Synthesis of Reversible Multiplexers

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Abstract— The advantages of reversible logic espically power reduction have drawn up a significant interest in this field and it finds its application in various fields including quantum computing, optical computing, nanotechnology, computer graphic, cryptography, digital signal processing and many more. In this paper 2:1 and 4:1 conventional and reversible multiplexer have been compared in terms of power dissipation. The circuit has been simulated using Xilinx 8.2i. Transistor implementation and power dissipation is measured using design architect. The results of reversible logic have been shown and compared with irreversible mux.

Index Terms— Basic reversible gates, reversible multiplexer, irreversible multiplexer, garbage output, constant input,technology, select lines

1 Introduction

INterest in reversible logic arises from the ability of this logic to reduce the power dissipation in the circuit. The reversible logic technique can be applied to both combinational and sequential circuits. In the irreversible logic for the loss of each bit of information KT ln 2 of power dissipation occurs [1]. This amount of heat dissipation is negligible in large circuit but it becomes considerable in large circuits. It was stated by Bennett that if certain computation is carried out in reversible manner, the power dissipation due to bit loss can be avoided [2].In reversible logic number of inputs and outputs are equal. In this paper conventional and reversible mux have been simulated on Xilinx 8.2i to obtain the RTL view and then implemented using Mentor Graphics to obtain the power dissipation of the circuit. The conventional and reversible mux is then compared in terms of number of inputs and outputs and power dissipation.

The topic has been introduced in the section 1. Section 2 in this paper explains some of the basic reversible gates depicting the input and output values and truth table is shown for each gate.. Section 3 describes the circuit diagram of the reversible as well as irreversible multiplexer. The simulation results and the power comparison have been shown in section 4. The topic is concluded in section 5

2 Reversible Gates

Reversible gates are the gates in which the number of inputs and outputs are equal.Various reversible gates along with their truth tables have been presented. With the help of gates described below, design of reversible multiplexer has been done. In conventional gates, number of inputs and outputs differ as a result of which loss of information and hence power dissipation is there. Moreover backward computation is not possible in traditional gates. But in the reversible logic input can be uniquely determined from the outputs i.e there is a specific output for each specific input.

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Garbage outputs are the outputs that are needed in the circuit so as to equalize number of inputs and outputs condition. Special consideration should be given to reduce the number of garbage outputs as these add up to make the quantum cost of the circuit more. Sometimes certain constant input either logic 1 or logic 0 is also used to make the circuit work properly. These constants inputs must be kept as minimum as possible. The reversible logic finds its application in various fields. The new generation computers will be based on this logic only. The various reversible gates along with their truth table have been described below:

2.1 Feynman Gate

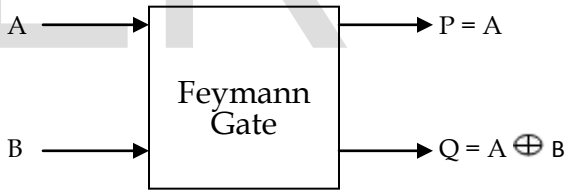

Figure 1: Feynmann Gate

This gate is also called as Copying gate [3]. The truth table is described below.

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of FeynmannGate

2.2 Fredkin Gate

Fredkin gate comprises of three inputs and three outputs [4]. The value of output is shown in the Figure2.

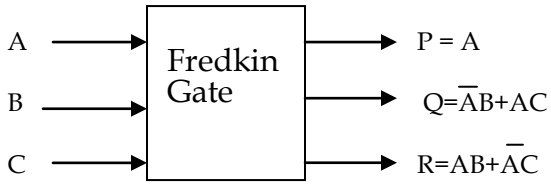

Figure 2: Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	1

Table 2: Truth table of Fredkin Gate

2.3 Peres Gate

Peres gate is also a three input and three output gate [5].

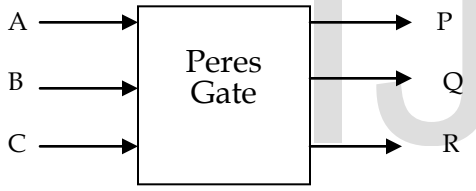

Figure 3: Peres Gate

Here P = A, Q=A$\oplus$ B, R= AB $\oplus$ C. The truth table of Peres Gate is given below:

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Table 3: Truth table of Peres Gate

2.4 Toffoli Gate

It has A, B, C as three inputs and P, Q, R as three outputs [6]. The outputs can be expressed as

$$P = A\ ,\ Q = B\ ,\ R = AB \oplus C$$

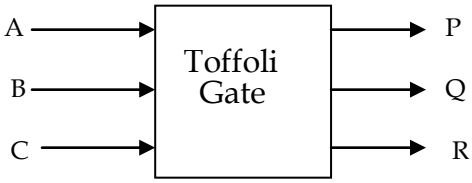

Figure 4: Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 4: Truth table of Toffoli gate

2.5 BJN Gate

BJN Gate has three inputs A, B, C and P, Q, R are three outputs [7]. The figure 5 shows the block diagram of BJN gate.

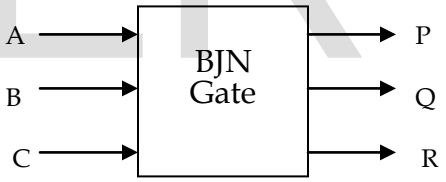

Figure 5: BJN Gate

Here P = A, Q = B and R = (A+B) $\oplus$ C. The truth table of above mentioned gate is depicted in table 5.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

Table 5: Truth table of BJN Gate

2.6 New Gate

New gate [8] described here is 3*3 reversible gate. The output P = A, Q = AB ⊕ C, R = A C ⊕ B.

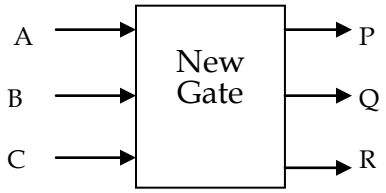

Figure 6: New Gate

The truth table of New gate is shown below in table 7.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	1	0
1	1	1	1	0	0

Table 6: Truth table of New Gate

3 Sections

Multiplexer is a combinational device that selects one output from number of inputs depending upon the value of select line. The basic multiplexer is in the form of 2 to 1 mux, 4 to 1, 8 to 1 mux. 2 to 1 mux refers that two inputs are used and one output. The number of select line is 1 in 2:1 multiplexer, whereas in case of 4:1 mux, number of select lines are 2. In general the multiplexer is of the form 2n to 1, where 'n' number of select lines.

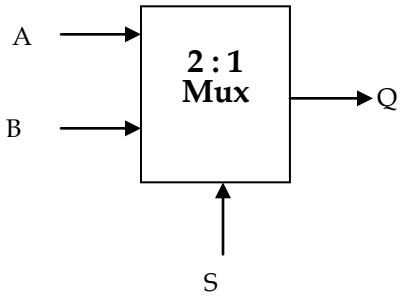

Figure 7: 2 to 1 multiplexer

In figure 7, A and B are two inputs , S is the select line and Q is the output. When value of S is low,the output Q = A, whereas when S = 1, the output Q = B. This 2 to 1 multiplexer can be implemented using reversible gate too. The fredkin gate is used for implementation of this mux [9]. The output Q of the Fredkin gate realizes the equation of multiplexer.

The 4 to 1 reversible mux can be realized using Fredkin gate, Feynman gate, Peres gate and BJN gate. All the said gates have been explained above in section 2. The circuit diagram for 4 to 1 reversible gate is shown below in the figure 8. Here s1 and s0 are two select lines used. The outputs from g1 to g10 represent the garbage outputs. I0, I1, I2, I3 represents the inputs used.

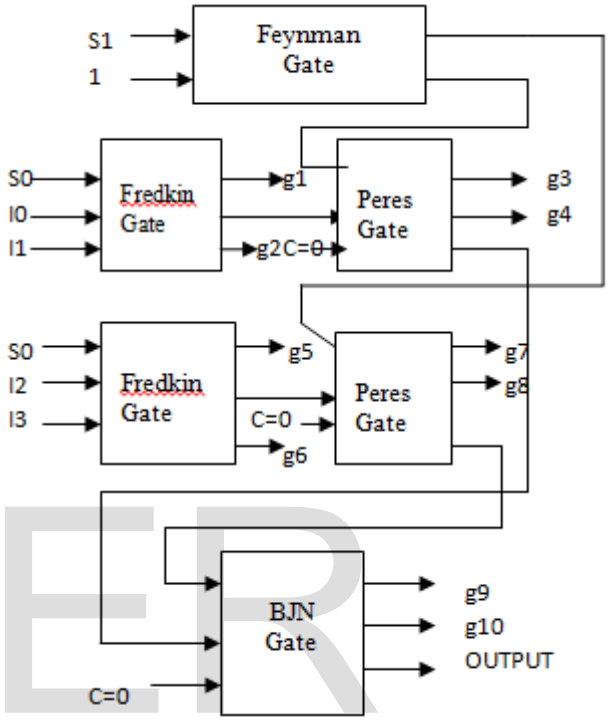

Figure 8: Reversible 4 to 1 mux

Number of constant inputs in the reversible multiplexer is 4 and number of garbage outputs is 10.

4 Simulation Results

The reversible and conventional 2 to 1mutiplexer has been realized in Mentor Graphics. ELDO and EZ Waves are used for obtaining the power consumption and the waveforms. The technology used is 180 nanometer. The results show considerable reduction in power dissipation while using the reversible logic in comparison to conventional multiplexer. So it can be analysed that the higher order reversible multiplexer too will dissipate less power as compared to conventional multiplexer.

Figure 9 depicts the circuit diagram of 2 to 1 conventional multiplexer. The blocks presented in the figure have already been simulated in another window of Design Architect. Here S represents the select line and d1 and d2 are two inputs. Out is the output. Figure 10 shows the output waveforms of the multiplexer.

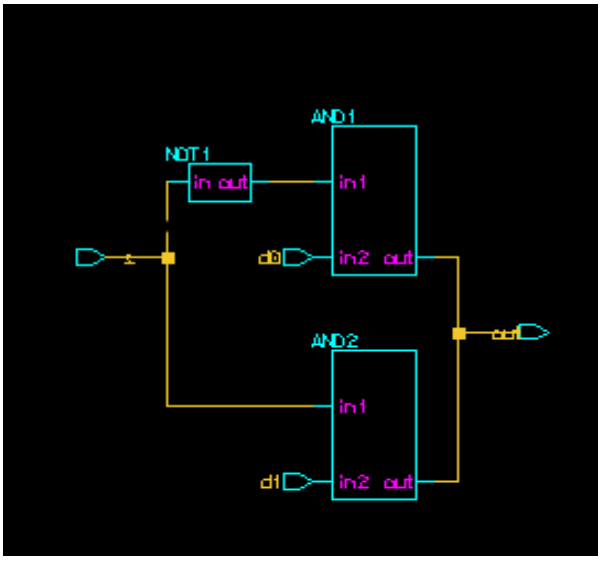

Figure 9: Conventional 2 to 1 Mux

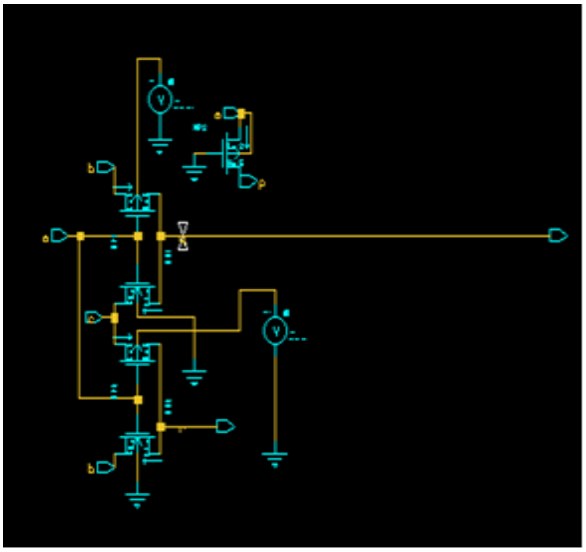

Figure 11: Reversible 2 to 1 Mux

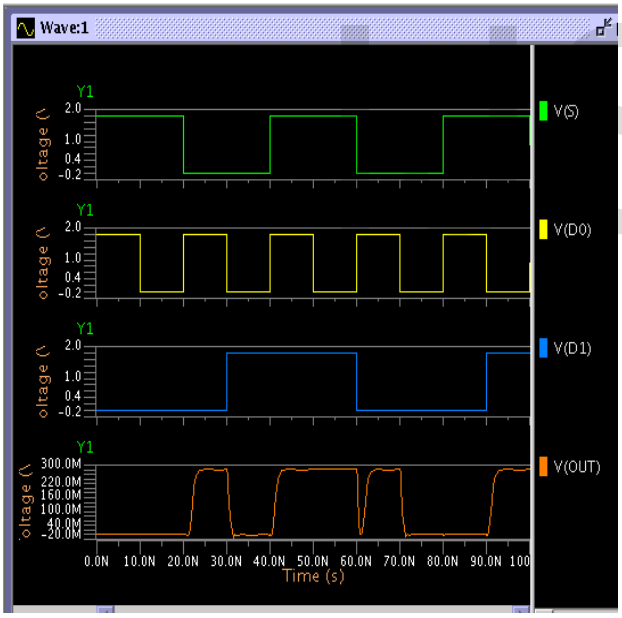

Figure 10: Waveforms for Conventional Mux

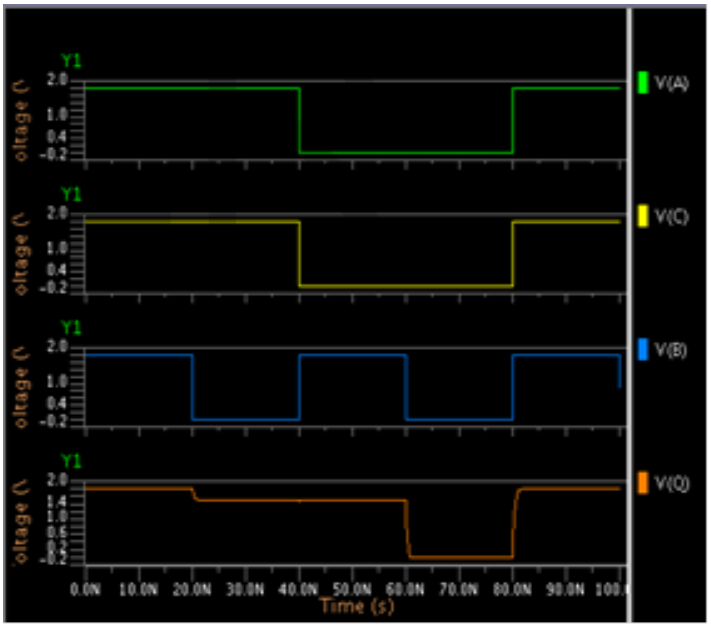

Figure 12: Waveforms for Reversible Mux

The reversible multiplexer is shown in figure 11 and its output waveforms in figure 12. The reversible multiplexer consists of two PMOS and two NMOS gates. A single PMOS is connected which act as a buffer. The drain terminal of buffer gate is connected to input 'a'. And the PMOS gate is always on as its gate terminal is connected to zero. The substrate of PMOS is connected to supply voltage of 1.8 Volt and the substrate of NMOS is connected to ground. Table 7 compares the power consumption of both these multiplexers. Here A and B are two inputs and C act as constant input. Q is the output of the reversible 2 to 1 multiplexer.

The table depicting power consumption of reversible and conventional 2 to 1 multiplexer is shown below.

Reversible mux	Conventional mux
13.0320 p Watt	55.1609 p Watt

Table 7: Power comparison

The table 7 clearly shows that the power of reversible multiplexer is quite less as compared to the conventional multiplexer. Here 'p' refers to pico .The reversible 4 to 1 mux has been implemented in Xilinx 8.2i. The RTL view of this 4 to 1 reversible multiplexer has also been shown in figure 13.

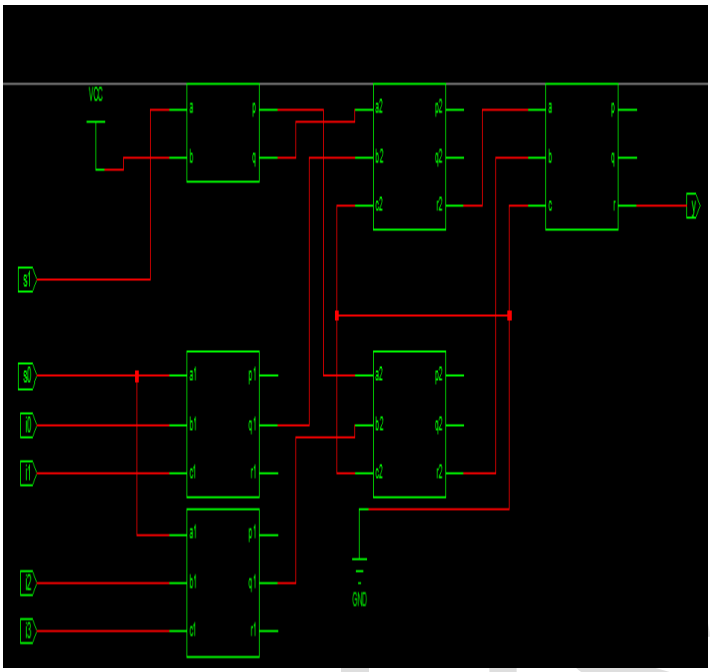

Figure 13: RTL View of 4 to 1 Reversible Mux

Here S0 and S1 are two select lines. I0, I1, I2, I3 are three inputs and Y is the output. Four constant inputs are used. The output waveform of 4 to 1 multiplexer is shown in figure 14. The circuit has been simulated for 100 ns.

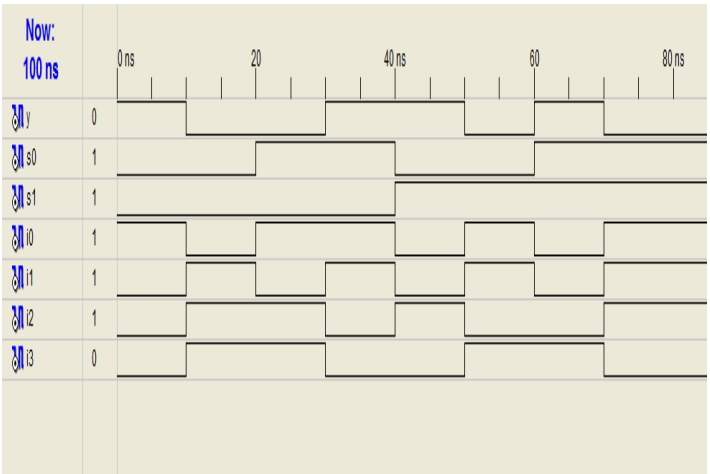

Figure 14: Waveforms of 4 to 1 Reversible Mux

5 Conclusion

In this paper reversible logic has been discussed for power reduction in multiplexers. The multiplexers are used in telephone switches. It has been seen that the power gets reduced when the circuit is implemented using reversible logic. The circuit is simulated on Mentor Graphics. 4 to 1 multiplexer has been implemented on Xilinx 8.2i. This circuit can be implemented using other reversible gates also.

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