Study and Experimental Validation on Total Harmonic Distortion Reduction by Increasing Arm Inductance for Modular Multilevel Converter

Abd Almula Gebreel

Abstract—This paper presents the effect of changing arm inductor for the modular multilevel converter (MMC) behavior in order to analyze the change in Total Harmonics Distortion (THD) for all MMC quantities including circulating current, upper arm current and voltage, lower arm current and voltage, and AC output voltage and current. The Operation principle, Circuit operation, and Converter equations are discussed first. Second, the multilevel modulation process for MMC is explained. Third, analysis of the Balancing of the submodule voltages based on sorting is carried out in this paper. For the reason that increasing arm inductor size could reduce the THD of MMC, this effect will be investigated in this paper. A new method to implement the submodule selection, which is the key technique for MMC for a wide range of a number of submodules per arm, is proposed and verified by the simulations. Analysis of the arm inductance value effect on MMC is carried out from many simulation results in this paper. Finally, the hardware design and software design of the prototype is presented to verify the arm inductor value effect on MMC experimentally. The experimental results are also documented in this paper.

Index Terms—Arm inductance effect on MMC.

1 INTRODUCTION

One of the important parts of MMC is the arm inductor. The inductor (Larm) for MMC is connected in the way of the DC transmission and in series with the converter as in Figure 1 for single phase. Arm inductor is placed to use its inductance in the electric circuit to surprise circulating current ripple to reduce higher harmonics as will be seen by simulation and experimentally. MMC was first presented as AC to AC and DC to AC converters, for high-power experimental prototypes [6]. MMC was presented as a cascaded converter based on cascading identical submodules [7]. The selection submodules have to be inserted or bypassed for each arm of the converter while maintaining each submodule capacitor voltage around its reference voltage, and phase arm modulation is an important aspect in the operation of the converter. The submodule, the heart of an MMC, has had its operation and circuit configuration explained before [1], [12], [13]. [12] simplifies the MMC by considering the sum of capacitor voltages in each arm instead of individual capacitor voltage. Different control approaches with various modifications were presented in [25] and [26] to investigate dynamic and required voltage balance of MMC topology. A number of applications such as voltage source converter-based HVDC transmission and back-to-back converter had been studied based on the use of MMC [21] and [27]. Also, in [28] and [29], high-voltage super-grids provided the possibility of using MMC in the configuration for multi-terminal HVDC. The modular topologies classification, presented in [7], does not rate the converter as a topology with many useful submodules for a DC system that can transmit up to 2200 KV. Power losses for both the converter and its submodules were evaluated in [30] and in [31], submodules losses were evaluated by utilizing different configurations for MMC. The effect of sampling frequency on total harmonics distortion in the operation of the converter was analyzed in [32]. Also, the effect of dead time in the submodule of the converter was considered in [33], [34] presented minimization method of DC-link ripple, a mathematical model for the capacitor voltage variations, and improved voltage balancing control system for MMC in the converter topology [35]. Arm inductance and submodule capacitance can be calculated in different methods as in [37], [38], and [39]. Also, smoothing reactor for HVDC systems has been evaluated exactly [40] and approximated [41]. Transmitting power 10,000 MW and distance up to 3000 km with ±1100 kV DC is considered economic, efficient, mature technology [6] and [42]. The DC bus voltage of UHVDC transmission system determines the number of submodules per arm. Therefore, with 2200 KVDC ([6], [42], [43]), each converter arm consists of a large number of submodules. The ripple shall be within limits up to 10% of the direct current value [36]. Arm inductor can be with value of inductance up to 1.5 H, While for back-to-back systems values is varying from high of 200mH to a low of 12mH [37], [39]. Also, it can smooth the circulating current by reducing the ripple in the direct current in order to prevent the current becoming discontinuous at light load. Moreover, it can be used to decrease harmonic output voltages and current in the MMC system. More importantly, the decreasing THD becomes the major concern for sensitive industry and HVDC applications. The importance of this paper that offering for industry applications either medium or high voltages two choices to reduce THD either by a large number of submodules per arm or increasing arm inductance instead.

2 OPERATION PRINCIPLES AND CONVERTER EQUATIONS

Figure 1 illustrates a final single-phase MMC circuit with its submodule. Since the capacitors are not guaranteed to provide constant voltage when connected to a circuit, this brings some problems. If a capacitor is inserted in the arm, its voltage varies according to the direction of the current. The simplest and accurate solution is to use the effect that charges and discharges the capacitors actively in the converter modulation.
itself through a specific algorithm to be explained in detail later in this paper. However, capacitor voltages are still inconstant, something which could cause current transient due to unequal voltages between the legs. For this reason, inductances are also placed in each arm. The heart of the MMC is the submodule and its basic half-bridge scheme appears in Figure 1.

![Figure 1. Single-phase MMC circuit and its submodule ((a) Positive and (b) negative current flow inside an MMC submodule](image)

Table 1 shows switching states for the submodule. In the latter situation and based on the proposed algorithm, the capacitor maintains its state of charge and its voltage remains unchanged. Using switching states in Table 1, it is possible to control each of the submodules separately.

<table>
<thead>
<tr>
<th>TABLE 1</th>
<th>SWITCHING STATES FOR EACH SUBMODULE</th>
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<tbody>
<tr>
<td>T1</td>
<td>T2</td>
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<tr>
<td>OFF</td>
<td>ON</td>
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<td>OFF</td>
<td>OFF</td>
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<td>OFF</td>
<td>OFF</td>
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<tr>
<td>ON</td>
<td>OFF</td>
</tr>
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</table>

To explain how the proposed PWM algorithm works for MMC circuit, a specific example will show how to generate a voltage waveform. In this example, the number of submodules per each leg will be 4; the converter will convert DC to AC with the 5-level waveform (n=N+1; where n number of output voltage level), which will be explained in detail. The voltage across each capacitor can be given as in (1):

$$V_C = \frac{V_{dc}}{N} = \frac{V_{dc}}{4} \ V.$$  \hspace{1cm} (1)$$

$V_{dc}$ is DC bus voltage, and assuming the submodule selection process is effective, the submodule capacitors within a converter arm can be assumed to be equally charged. This is possible with a switching frequency high enough to allow the modulator to act even on very small disturbances in this balance. It will be proven later that these assumptions can apply for a small number of submodules. Figure 1 shows an equivalent electrical circuit for one phase leg of MMC and Table 2 shows MMC parameters definitions.

Let the converter consist of N submodules per arm. In general, each arm is controlled by an insertion index $x$, which is defined such that $x = 0$ means that all N submodules in the arm are bypassed, while $x = 1$ means that all N submodules in the arm are inserted. In the former case, the current is flowing through the arm will not pass through any capacitor, so the equivalent capacitive arm impedance is zero. In the latter case, the arm current will meet N capacitors connected in series, making the equivalent capacitance of the arm C/N. If each submodule capacitor has capacitance $C$, the effective capacitance of the one arm is given by (2):

$$C_{arm} = \frac{C}{N \cdot x}.$$  \hspace{1cm} (2)$$

Naming the upper and lower arm currents $I_{up}$ and $I_{lo}$ respectively, and defining their polarities as illustrated on Figure 1, the output phase current is calculated as their sum in (3).

$$I_{out} = I_{up} - I_{lo}.$$  \hspace{1cm} (3)$$

The output phase current is assumed to be equally shared by both upper and lower arm. However, and as mentioned in previous paragraphs, there is a deviation from this ideal condition since part of the current passes through the series-connected arms and the DC source. Let this circulating current be called $I_{cir}$ as in (4).
In a three-phase system, \( I_{\text{cir}} = \frac{1}{3} I_{dC} \) and in a single phase system, \( I_{\text{cir}} = I_{dC} \).

Defining \( x_U \) and \( x_L \) as the insertion indices of the upper and the lower arm respectively, the following equation is derived:

\[
V_{\text{out}} = x_U V_{C,U,\text{arm(t)}} - x_U V_{C,U,\text{arm(t)}} - \frac{R_{\text{arm}}}{2} I_L - \frac{1}{\tau_{\text{arm}}} \frac{dI_L}{dt} \quad (5)
\]

Where \( V_{\text{out}} \) is the output phase voltage, by solving the last two equations, the equivalent voltage for the external load connected to the AC terminal becomes, and \( V_{C,U,\text{arm}(t)} \) and \( V_{C,L,\text{arm}(t)} \) are total upper arm capacitor and total lower arm capacitor respectively.

It is obvious from (4) that upper arm current generates the positive half cycle of the output AC current while lower arm current generates its negative half cycle. Also, from (5), it is obvious that upper arm voltage generates the negative half cycle of output AC voltage while lower arm voltage generates its positive half cycle of the output AC voltage as will be proved by computer simulation and experimental prototype.

3 PROPOSED PWM ALGORITHM

3.1 Reference arm voltage for \( N \) submodules

The proposed PWM algorithm of MMC is based on the equalization of the inserted submodules for one arm with the bypassed submodules for the other arm. First, the operation of MMC as \( n (N+1) \) level converter is discussed. The principle is that in each instant, \( N \) submodules are inserted and \( N \) submodules bypassed for the whole leg. Let \( N_U \) be the number of submodules inserted in the upper arm and \( N_L \) the number of submodules inserted in the lower arm. Accordingly, the AC terminal can take \( N+1 \) different potentials when the number of inserted modules varies between 0 and \( N \). A sinusoidal reference is applied to the modulator, which is then converted into a varying insertion index for each arm as defined by (6), where \( \omega N \) is the angular frequency of the output voltage.

\[
m(t) = N \cdot \overline{m} \cos(\omega_N t) \quad (6)
\]

\( m \) is the maximum value for modulation index, which is 1.

The main target from this process getting a number of inserted submodules for both arms with keeping the condition of this method mentioned above. Therefore, equation (6) will split into two equations (7), leading to (8) and (9):

\[
\begin{align*}
N_U &= N - N_{L,\text{bypassed}} = N_{L,\text{inserted}} \\
N_L &= N + N_{L,\text{bypassed}} = N_{L,\text{inserted}}
\end{align*}
\]

\[
N_U = \frac{N - m(t)}{2} \quad (0 < N_U \leq N) \quad (8)
\]

\[
N_L = \frac{N + m(t)}{2} \quad (0 < N_L \leq N) \quad (9)
\]

This step is considered a starting point for indirect PWM as can be seen later. Figure 2 (a) shows \( m(t) \) and a number of inserted submodules for both upper and lower arms in a sinusoidal waveform.

3.2 Flooring arms voltages references

Since the numbers of inserted or bypassed submodules for both arms are real, positive integers, flooring both sine waves of upper and lower arms is necessary. Flooring value (a) is choosing (a) to the nearest integer in the direction of negative infinity, while ceiling value (a) is choosing (a) to the nearest integer in the direction of positive infinity. For example, flooring value for 0.5 is 0 and flooring value for 1.99 is 1. Figure 2 (b) shows inserted submodules for both arms after flooring (green signal is \( N \) before flooring and red signal is \( N \) after flooring).

3.3 References arms voltages and carrier signals modulator

At the same time as the last step, the reference signals for both upper and lower arms are modulated with a carrier signal and a switching frequency for the switches as seen in Figure 2(c). The modulator will modulate both signals to the waveform in Figure 2(d) for both upper and lower arms respectively in a process which aims to create a signal which matches an assigned reference, by averaging the number of inserted submodules between a floor and a ceiling number in every sampling period. This process determines the inserted submodules for both upper and lower arms and the exact instants of the switching actions. Figure 2(d) shows inserted submodules for both upper and lower arms at the same time, with the number of inserted submodules in one arm equal to the number of bypassed submodules (\( N - N_{L,\text{inserted}} \)) in the other arm, which achieves balancing voltages between the upper arm and lower arm across the AC terminal.

A sinusoidal waveform in the output can, therefore, be achieved by varying the number of the submodules in the upper and lower arm with a sinusoidal manner. Since the voltage of each arm is not continuous but varies with the switching of the submodules, the selection of the submodules and PWM method applied to the converter affects its operation and output waveforms. The two arms that comprise the phase-leg of the converter can be modulated either simultaneously or independently.

The number of submodules to insert or bypass was found by comparing voltage reference with carrier waves. The next step, the selection of submodules, can be based on their capacitor voltage measurements. When the multivalue current direction is known, it can be predicted whether the capacitor will charge or discharge when inserted. This information is used to insert or bypass submodules closest to the range limits.
3.4 Submodules selection

To maintain the individual voltage of each submodule around its reference voltage takes an active balancing method. The voltage of each individual submodule together with the arm current needs to be measured and available in the voltage-balancing algorithm. The voltage-balancing algorithm selects the submodules in each of the arms of the converter based on the relative voltage values of all the arm submodules and direction of the arm current. Ascending or descending capacitor voltages are required to be used for balancing algorithm. The next submodule that switches in the arm is selected based on the direction of the current and the sorted voltages so that

When the arm current is positive (iarm > 0) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is not connected to be inserted into the arm.

If the arm current is positive (iarm > 0) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is connected to the arm to be bypassed and removed from the arm.

If the arm current is negative (iarm > 0) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is not connected to the arm to be inserted to the arm.

If the arm current is negative (iarm < 0) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is connected to the arm to be bypassed and removed from the arm.

The capacitor voltage of the submodule will not change when the submodule is not connected to the arm of the converter; it will remain at the level it was before it was removed from the arm. The capacitor voltage of the submodule will not change when the submodule is not connected to the arm of the converter; it will remain at the level it was before it was removed from the arm of the converter. The voltage balancing algorithm uses the data coming from the modulation process, upper and lower arms currents, and upper and lower arms sorting voltages. Figure 3 shows the proposed PWM algorithm sorting both arms voltages. The main aim of the selection process is to maintain the voltages of the capacitors close to the reference values. This is accomplished during the whole cycle of the waveform and the capacitors’ actual voltages drift from their reference value within this cycle due to the load current coming from upper and lower arms currents. Moreover, the algorithm considers the actual values for capacitor voltages coming from voltages measurements after sorting them in the selection of the submodules, but their relative voltage relates to the remaining submodules in the arm. In some cases, the submodule selected to be inserted into the arm of the converter according to the logic of the algorithm will further deviate from the reference voltage. The balancing of the submodule is not an instantaneous process and balancing around the reference occurs over the fundamental period.

Figure 2 PWM signal and its generated number of submodules

a. Reference voltage, the number of inserted submodules for both arms in continuous mode.

b. Number of upper and lower submodules after flooring.

c. Reference signals for both upper and lower arms across carrier signal.

d. Number of inserted submodules for upper and lower arms.
4. SIMULATION RESULTS

Since increasing the arm inductor is used to suppress the circulating current to be stable. The stability of circulating current tends to stability of submodule voltage in the arm. Upper arm voltage and lower arm voltage will have less THD when the fluctuation of the capacitor voltage is going to be less and less. 50-level MMC had been chosen to analyze the behavior of MMC with different values of arm inductors. Table 2 shows figures 4(d) and 5(d).

![Figure 3. Proposed PWM algorithm with sorting voltage for MMC](image)

**TABLE 3**

<table>
<thead>
<tr>
<th>Inductor size (mH)</th>
<th>Output Voltage</th>
<th>Output Current</th>
<th>THD%</th>
<th>DC component (A)</th>
<th>THD%</th>
<th>DC component (A)</th>
<th>Voltage ripple</th>
<th>DC component (A)</th>
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<tr>
<td>13.1</td>
<td>5.05</td>
<td>2.41</td>
<td>15.5</td>
<td>15.19</td>
<td>5.15</td>
<td>15.21</td>
<td>8.8</td>
<td>207.1</td>
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<td>15</td>
<td>4.92</td>
<td>2.41</td>
<td>57</td>
<td>13</td>
<td>21.5</td>
<td>13</td>
<td>8.5</td>
<td>206.1</td>
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<tr>
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<td>4.61</td>
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<td>59</td>
<td>9.41</td>
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<td>9.41</td>
<td>7.63</td>
<td>205.9</td>
</tr>
<tr>
<td>25</td>
<td>4.34</td>
<td>2.35</td>
<td>32</td>
<td>7.42</td>
<td>20.6</td>
<td>7.42</td>
<td>7.8</td>
<td>205.97</td>
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<td>4.1</td>
<td>2.33</td>
<td>52</td>
<td>6.2</td>
<td>20.1</td>
<td>6.2</td>
<td>7.4</td>
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<tr>
<td>35</td>
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<td>2.3</td>
<td>57</td>
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<tr>
<td>45</td>
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<td>18.65</td>
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<td>3.4</td>
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<td>7.1</td>
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</tr>
<tr>
<td>65</td>
<td>3.1</td>
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<td>30</td>
<td>2.9</td>
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<td>6.9</td>
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<tr>
<td>85</td>
<td>2.8</td>
<td>1.99</td>
<td>26</td>
<td>2.3</td>
<td>14.84</td>
<td>2.3</td>
<td>6.5</td>
<td>205.79</td>
</tr>
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</table>

The simulation results for MMC 50-level at different values of arm inductor with the same DC bus and all parameters compared with calculated value(13.1mH). As can be seen from figure 4(a) and 5(a) output voltage and current for MMC at 85mH is smoother that at 13.1mH and as values from Table 2 the THD was reduced almost 90% from 5.05% to 2.8%. Moreover, it is obvious that the circulating current ripple has been suppressed from 63.96% to 14.84% and this difference is very clear from circulating current waveforms as can be seen in figures 4(a) to 4(d).
MMC 50-level at calculated value of the arm inductor 13.1mH, \( V_{dc} = 5000 \text{ V} \), arm resistor = 0.5ohm, load inductor = 25mH, load resistor = 25, ohm, power factor =0.9540, and submodule capacitor= 0.0185 F.

Figure 4. Simulation results for AC for 25-level MMC at arm inductor 13.1 mH

- a. the output voltage and current
- b. upper and lower arms currents
- c. intermediate capacitors upper and lower arms and
- d. circulating current

Figures 5(a) to 5(b) show the simulation results for MMC 50-level at eight times of inductance value of the arm inductor (40mH) without change for other parameters.

Figure 5. Simulation results for AC for 25-level MMC at arm inductor 85 mH

- a. The output voltage and current
- b. upper and lower arms currents
- c. intermediate capacitors upper and lower arms and
- d. circulating current

Figure 6(a) shows the relationship between arm inductor and output voltage THD, figure 6(b) shows the relationship
between arm inductor and maximum output voltage, and figure 6(c) shows the relationship between arm inductor and circulating current ripple. As expected and can be seen from Table 2, THD for output voltage and current, THD for upper and lower arms current, circulating current ripple can be reduced by increasing the value of arm inductor.

5. EXPERIMENTAL RESULTS

The proposed modulation for the MMC is also verified on a phase-leg experimental prototype with two submodules per arm. The specifications of the laboratory prototype are given in Table 3. The results, which are given below, correspond to single-phase operation with 3kHz switching frequency. Figure 7(a) shows the output voltage of the 3-level modulation concept and output phase current. Figure 7(b) shows upper and lower arm current generating output current and Figure 7(c) shows upper and lower arm voltages generating output voltage.

Since the change in output voltage with increasing arm induct-
tance is invisible experimentally with small number of output voltage level. Therefore, circulating current waveforms with 10 ms period were recorded at different values of arm inductance. Figures 8(a) to 8(d) show the suppression of circulating current with increasing arm inductor up to four times. It is obvious that circulating current is going to be flat more with increasing arm inductance.

6. CONCLUSION

This paper described the effectiveness of arm inductor on MMC THD for all quantities including maximum output voltage and current, circulating current and capacitor voltage ripples. Also, the study presented THD deduction by increasing arm inductance instead of increasing number of submodules per arm offering more options to reduce the cost. The relationships of arm inductor with THD output voltage, maximum output voltage, circulating current ripple and submodule capacitor voltage ripple were presented. It is obvious that increasing the arm inductance leads to stabilize the circulating current and capacitor voltage which leads to reduce THD for the output voltage and current. The proposed PWM control comes to fulfill the requirements of UHVDC bus voltage in this paper with many contributions. Since there will be demand for UHVDC in the next years. The proposed method works with low switching frequency for UHVDC systems, which will decrease converter losses. Moreover, for MMC itself the proposed method offers simple numerical algorithm for MMC topology that can be used with large or small number of submodules per arm either experimentally or by simulation. Selection process for inserting or bypassing submodules guarantees capacitors voltages around the reference voltage (Vdc/N) with voltage ripple less than 7% even for large number of submodules per arm. More converter stability can be achieved by equal sharing of currents from both arms to the load. Overall, the proposed PWM allows MMC to be used with large scale of power transmission either HVDC systems or large scale of solar energy and also can be used for large motors control. In this paper, the prototype hardware, the implementation and experimental results of the effectiveness of arm inductor on MMC behavior is discussed and evaluated in order to bring agreement with simulation results.
REFERENCES


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