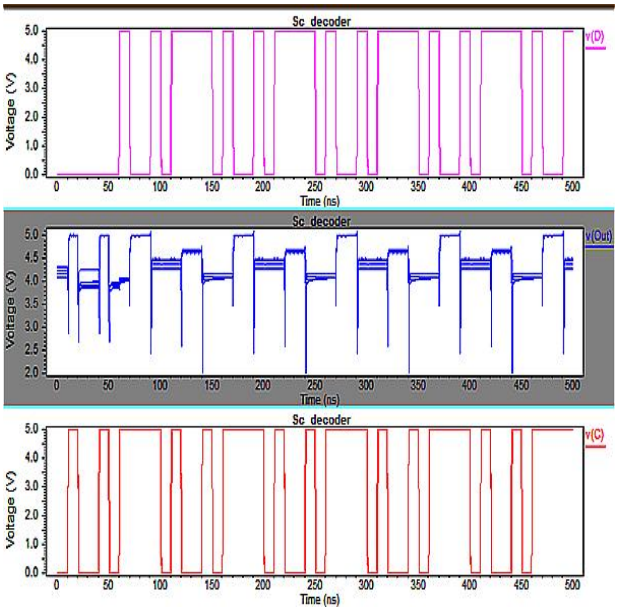

Average power consumed=4.449798e-004 watts at V_{DD}=5V

Fig 30. Simulation output of Reversible 2to 4 decoder Using SC Gate

From the Figure 30 of Reversible 2to 4 decoder is Proven because that only one Output is high for various input means that Reversible 2to4 decoder is verified and give precise output on Tanner 14 EDA platform.

Table 9 Comparision Result of Reversible decoder 2to4 decoder

Reversible decoder	Transistor Count	Garbage Output	Power dissipaton at V_{DD}=1.8V
Fredkin Gate 2to 4 decoder	14	4	7.561475e-005 watt
SC Gate 2 to4 decoder	8	5	2.105985e-007 watts

7 CONCLUSION

In this Paper we have show an epitome design for reversible decoder. Decoder are more often used for Digital display, digital to analog converter and for memory addressing etc, In Reversible decoder comprise of that in schematization of Quantum cost as canvas to fredkin gate. In 2 to 4 decoder has Quantum cost 15 and single fredkin gate has 5. Future works is promoting improvement in Decoration of Reversible decoder to minimize the Garbage output and total logic calculation.

Acknowledgment

The authors acknowledge Research Cum Teaching Fellowship through TEQIP-II provide by World Bank.

References

[1] Landauer, R., "Irreversibility and heat generation in the computing process", IBM. Research and Development, 5(3): pp. 183-191, 1961.

[2] P. Gupta, A. Agrawal, and N. K. Jha, "An algorithm for synthesis of reversible logic circuits," IEEE Transactions on Computer- Aided Design of Integrated Circuits and Systems, vol. 25, no. 11, pp. 2317–2330, 2006.

[3] V. V. Shende, A. K. Prasad, I. L. Markov, and J. P. Hayes, "Reversible logic circuit synthesis," in IEEE/ACM International Conference on Computer Aided Design (ICCAD '02), pp. 353–360, San Jose, Calif, USA, November 2002.

[4] Rashmi S.B "Transitror implementation fo reversible PRT Gates" International Journal of Engineering Science and Technology (IJEST) Vol. 3 No. 3 March 2011.

[5] Arvind Kumar "Synthesis of 4 to 16 Reversible Decoder "ITSI Transactions on Electrical and Electronics Engineering (ITSI-TEEE) Volume -1, Issue -5, 2013

[6] Bahram Dehghan "Survey the inverse property of Quantum Gates for Concurrent error detection" Journal of Basic and applied Scientific Research 2013.

[7] Mohammad Assarian "Delay Reduction in optimized Reversible Multiplier Circuit" Research Journal of Applied Science,Engineering and Technology Jan 2012.

[8] Aakash Gupta "An Improved Structure of Reversible Adder and Substractor" International Journal of Electronics and Computer Science Engineering IJECSE Volume2 number2.

[9] Devendra Goyal "VHDL Implementation of Reversible Logic Gates" International Journal of Technology & Engineering Research IJATER Volume 2 Issue 3 may 20

[1] Mashina Basha "Transistor Implementation of Reversible Comparator Low Technique" Internation Journal of Computer Science and Information Technologies vol 3(3) 2012.

[1] Azad Khan Md. M., 2002. "Design of full adder with reversible gate" International Conference on Computer and Information Technology, Dhaka, Bangladesh, pp. 515-519.

[12] Bruce, J.W., M.A. Thornton, L. shivakuamaraiah, P.S. kokate and X. Li, "Efficient adder circuits based on a conservative reversible logic gate", IEEE computer society Annual symposium on VLSI, Pittsburgh, Pennsylvania, and pp: 83-88, 2000.

[13] T Toffoli, "*Reversible Computing*", Technical Memo MIT/LCS/TM-151, MIT Lab for Computer Science, 1980.

[14] Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B, "Low Power Reversible Parallel Binary adder/Subtractor", international Journal of VLSI design and communication Systems (VLSICS), Vol.1 no.3,Sept 2010.

[15] Thapliyal H, M. B.Sshrinivas." A New Reversible TSG Gate and Its Application for Designing Efficient Adder Circuits". Centre for VLSI and Embedded System Technologies International Institute of Information Technology, Hyderabad, 500019, India.

[16] Sk. N. Mahammad and K. Veezhinathan. "Constructing online testable circuits using reversible logic" IEEE Transactions on Instrumentation and Measurement, 59(1): pp:101-109, January 2010.

[17] Dmitri Maslov and Mehdi Saeedi. "Reversible circuit optimization via leaving the boolean domain" IEEE Transactions on CAD of Integrated Circuits and Systems, 30(6): pp: 806-816, 2011.

[18] Neeraj Kumar Misra, Subodh Wairya, Vinod Kumar Singh "An Inventive Design Of 4*4 Bit Reversible NS Gate" IEEE International Conference on Recent Advances and Innovation in Engineering (ICRAIE-2014), 2014.