Oscillation Based Testing for Low Voltage Two Stage Operational Transconductance Amplifier

Maninder kaur, Jasdeep Kaur

Abstract— The paper describes the design for testability (DFT) of low voltage two stage operational transconductance amplifiers based on oscillation based testing (OBT). The oscillation-test strategy is a low cost and robust test method for mixed-signal integrated circuits. Being a vectorless test method, it allows one to eliminate the analog test vector generator. Circuit under test is transformed to oscillators using very simple techniques. The tolerance band of the oscillation frequency is determined by a Monte Carlo analysis taking into account the nominal tolerance of all circuit under test components. Seventeen bridging faults and nine open faults have been analyzed in proposed work. Simulation results for two stage operational transconductance amplifier using a 0.18μm CMOS technology show that the proposed oscillation-based test strategy has more than 92% fault coverage and, with a minimum number of extra components, requires a negligible area overhead.

Index Terms—Circuit under test (CUT), Faults, Fault Injection Transistor (FIT), Operational Transconductance Amplifier (OTA), OBT, Monte Carlo Simulation.

1 Introduction

IN the last fifteen years or so, tremendous progress has been made in integrated analogue operational transcoductance amplifier research and development, however, testability of analog OTA is still rather unstructured since testability is not yet a precisely defined term in the analogue world. Consumer electronic systems often require design for testability (DFT) techniques, including built-in self-test structure for analogue and mixed-signal ICs [1]. DFT for analogue circuits is one of the most challenging tasks in mixed-signal ASIC design due to the sensitivity of the circuit parameters to component variations and process technologies [2],[3]. Hence, we need to explore and investigate some cost effective, robust test method without any additional signal generation circuit. The DFT of analog circuits can be generally divided into two categories; the first deals with controllability and observability of the internal nodes and the second is to convert the circuit under test (CUT) function and generate an output signal which contains the CUT performance to determine its malfunction[4],[5][6].

In this paper, we present an easily implemented and low cost test approach to improve the fault diagnosis and testability of typical two-stage CMOS operational transconductance amplifier using DFT based oscillation test methodology [7]. The proposed test method is simple and provides good fault coverage with little circuit modification. The OTM is a low cost and robust test method for mixed signal integrated circuit and has been very effective in detecting physical defects such as open, shorts and bridging defects. Being vector-less technique, it allows one to eliminate the analog test vector generator [8], [9]. In this test methodology, complete circuit is divided into small functional blocks like amplifier, comparator, filter etc and each block is transformed to a circuit which oscillates. The oscillation frequency of the CUT is compared with nominal frequency of fault free circuit. Faulty behavior is then indicated by deviations in the frequency of oscillations with respect the frequency under fault-free conditions. The tolerance band of the oscillation frequency is determined by a Monte Carlo analysis taking into account the nominal tolerance of all CUT components [10]. The testability has also been enhanced in the testing procedure using a simple fault-injection technique. The approach is attractive for its simplicity and robustness.

The format of this paper is as follows; two stage operational transconductance amplifier and analog fault modeling are discussed in Section 2 and section 3 respectively. Section 4 introduces OTA to oscillator conversion schemes. Test simulation results are given in Section 5 and Section 6 contains conclusions.

2 Two Stage Operational Transconductance Amplifier

Operational transconductance amplifier is voltage controlled current source. It is an amplifier whose differential input voltage produces an output current [11]. There is usually an additional input for a current to control the amplifier transconductance. It replaces operational amplifier because of its high bandwidth, high voltage swing, high SNR even at low voltages and also due to its unique characteristic suited for applications such s gain control, multiplexing, comparator, analog modulation, active-c filter, oscillator etc [12]. Thus OTA constitute as a major building block in the analog designing. In OTA the output current is linear function of differential input voltage as shown in equation 1.

$$I_{OUT} = (V_{in+} - V_{IN-}) \times G_m \qquad (1)$$

The basic circuit diagram of two stage OTA is shown in fig 1 with differential amplifier and current mirror as first stage

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which convert differential input to single –ended output. The input devices of the differential pair are formed by P-channel MOSFETs M1 and M2 and current mirror circuit formed by an N-channel MOSFETs, M3 and M4. The transistor M6 serves as P-channel common source amplifier which is the second stage of op-amp. The current Ibias of the op-amp circuit goes through current mirrors formed by P-channel MOSFETS, M8, M5 and M7. It is designed to produce a current of 113µA.

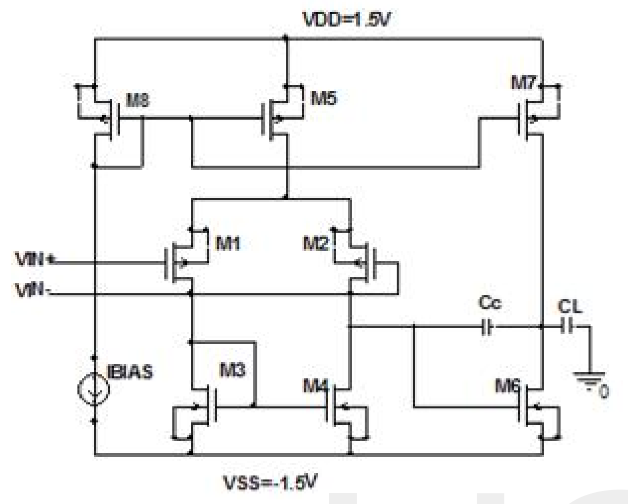

Fig. 1. Circuit Diagram of Two Stage CMOS OTA

3 FAULT MODELING

3.1 Fault Types

A fault in the analog or mixed- signal integrated circuit under test may be categorized as [13]:

1. Catastrophic (hard) faults: Catastrophic faults are the faults which are due to random defects causing failure in various component of the circuit. These hard faults include open, short or large variation in design parameter causes complete failure of the circuit.
2. Parametric (soft) faults: Parametric faults are faults due to statistical fluctuation in the manufacturing process, causing small deviation of CUT parameters from its tolerance band.

The faults considered in this study comprise catastrophic faults which includes open and bridging faults.

3.2 Fault Injection Transistor (FIT)

Fault injection transistor (FIT) basically n-MOS transistor is used for inducing bridging faults in the system to measure the fault tolerance or robustness of the system. Activating the fault injection transistor activates the fault in the CUT. The use of a fault injection transistor for the fault simulation prevents per--manent damage to the CUT by introduction of a physical met al short. This enables the operation of the CUT without any performance degradation in the normal mode. CUT works in modes: when FIT is inactive, it operates in normal mode and when FIT is activated it work as test mode without affecting the overall operation of the circuit.

3.3 Monte Carlo Simulation:

The tolerance band of nominal frequency of the CUT is determined by Monte-Carlo simulation [14]. The tolerance of 10% and 15% has been considered for resistance R1, R2 and C1, Cc respectively for the oscillator circuit. Monte Carlo analysis output is shown in fig 2.The oscillation frequency of the oscillatory CUT is measured and is compared with the nominal oscillation frequency of the fault free circuit. If the oscillation frequency lies close to the nominal frequency range, the CUT is accepted to be fault-free. The observability of a fault in parameter can be termed as the sensitivity of the oscillation frequency with respect to the variations of the parameter. In order to increase the observability of a defect in a component (or the fault in a parameter), the oscillator architecture is chosen so as to ensure the maximum possible CUT component contribution in determining the oscillation frequency [15].

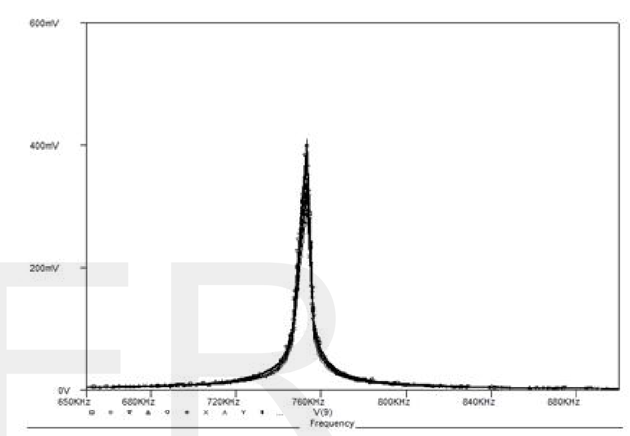

Fig. 2. Monte–Carlo analysis of CUT using Gaussian distribution

4 CUT INTO OSCILLATOR

The two-stage operational Transconductance amplifier (CUT) is transformed to oscillator by adding feedback circuit whose oscillation frequency can be expressed either as function of the CUT components or its important parameters. The feedback loop elements are adjusted in such a way that oscillations condition (Barkhausen criterion) of oscillator is maintained in its transfer function with no attenuation and no phase shift [16]. The transfer function of the oscillator is given by equation (2):

$$f_{osc} = \frac{f_{CUT}}{1 - f_{CUT}\, f_H} \quad (2)$$

Where f_{CUT} and f_H represents the transfer function of the CUT and feedback element respectively. The oscillation frequency f_{osc} and oscillation condition are obtained from equations (3), (4) and (5)

$$f_{CUT}(j\omega)\, f_H(j\omega) = 1 \quad (3)$$

Or equivalently

$$Re(f_{CUT} (j\omega) f_H (j\omega)) = 1 \qquad (4)$$

$$\text{Im}(f_{CUT} (j\omega) f_H (j\omega)) = 1 \qquad (5)$$

This condition is known as Barkhausen criterion which states that the signal must transverse the loop with no attenuation and no phase shift at the oscillation frequency [17].

In this work, CUT is converted into oscillator by using Wien bridge network [18]. The Wien bridge network is connected to the positive terminal of the CMOS OTA as shown the fig.3. The component values that we have used here are R1 = R3 = 10KΩ, R2 = 3 KΩ, R4 = 1KΩ, C3 = C1 = 16nF for simulation to achieve self-sustained oscillation.

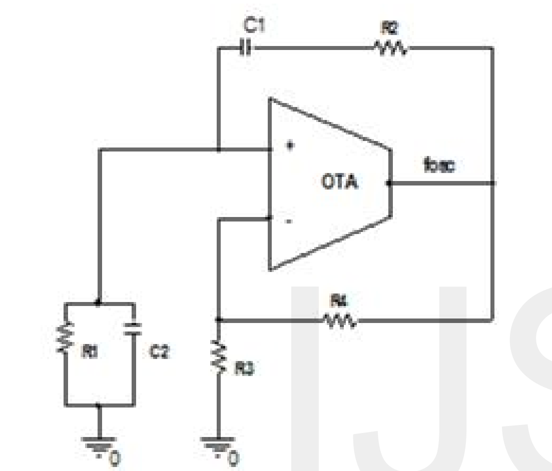

Fig. 3. Block diagram of CMOS OTA as an oscillator

Natural oscillation frequency is determined by the Fast Fourier Transform (FFT) analysis of oscillatory circuit. The schematic diagram of OTA as an oscillator is shown in fig.4.

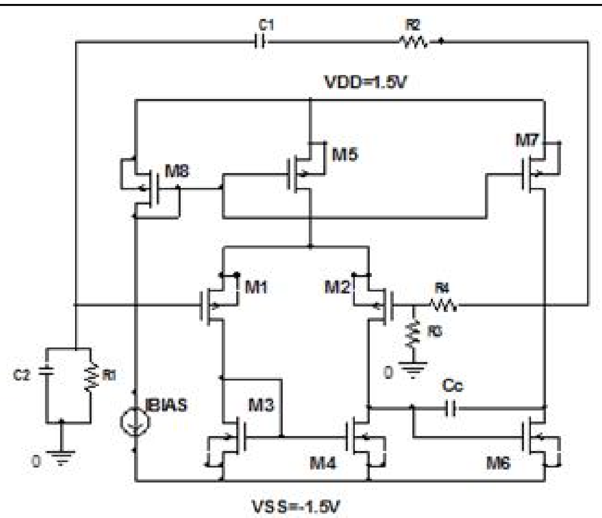

Fig. 4. Schematic Diagram of OTA as an oscillator

5 SIMULATION RESULTS

The testable OTA in fig.2 were simulated using PSPICE level 7 models 0.18µm CMOS technology for verification of the proposed OBT structures. The aim of this work is to show that oscillation-test strategy is able to detect the catastrophic faults as well as parametric faults. For the test purposes, OTA is converted into to an oscillator using quite simple technique which has nominal oscillation frequency of 752KHZ. Fig.5 shows time domain oscillation response of CUT, time domain oscillation response of the converted corresponding oscillator and the frequency response of the circuit under test. The fault-free oscillation frequency observed to be 750KHZ which was slightly shifted from the cut-off frequency of the circuit [18], [19].

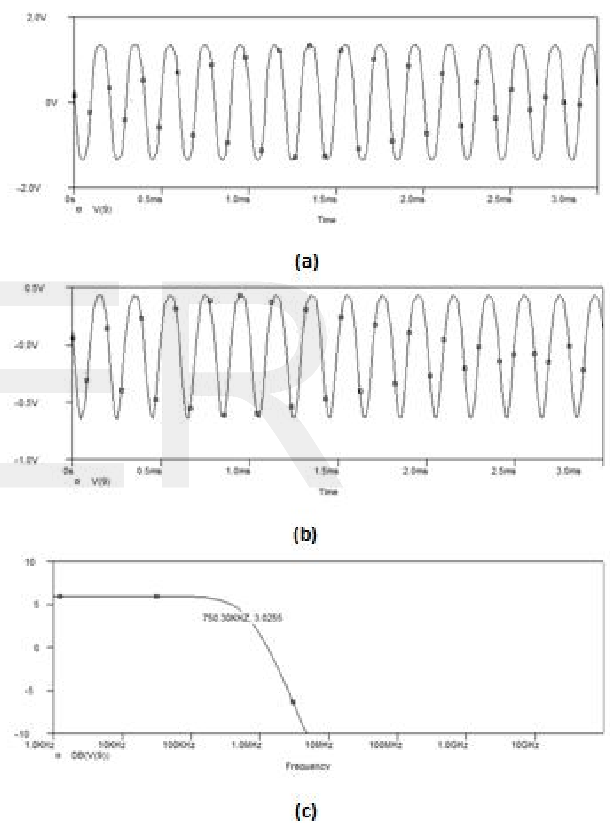

Fig. 5. (a) Output frequency of CUT, (b) Oscillation frequency of CUT as an oscillation (c) Cut-off frequency of CUT

To quantify the fault coverage and efficiency of the OBT strategy, a number of different faults were injected into the circuit under test according to the methodology described. To determine the undetectable tolerance band for the frequency, a Monte Carlo analysis was performed. The Fast Fourier Transform (FFT) of the output signal shows that the oscillation signal has lower and upper frequency deviation bounds of -4.25% and +5.05% respectively. The faults which produced oscillation frequency deviation outside this tolerance band were considered detectable.

In the present work, total twenty six faults which include sev-

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enteen short faults and nine open faults have been introduced in CUT oscillator. The value of W / L of FIT is taken as 1 / 0.5. It is observed that the twenty faults out of twenty six fault deviate from nominal oscillation frequency range whereas four faults resulted in loss of oscillation, thus twenty four faults have been detected with fault coverage of 92%.the results also show that two faults could not be detected, since the deviation observed in oscillation frequency with respect to nominal frequency was within the tolerance limit. Tables 1 present the effects of the injected faults on the oscillation frequencies and percentage deviations from the fault-free frequency.

TABLE 1
INJECTED FAUTS IN THE CUT

Component	ΔC/C	Δfosc/fosc	ΔC/C	Δfosc/fosc	ΔC/C	Δfosc/fosc
M1	GDS	20%	DSS	-9.93%	OPEN	NO%
M2	GDS	-10%	DSS	-9.3%	OPEN	-6.91%
M3	GDS	3%	DSS	-25%	OPEN	-35.77%
M4	GDS	NO	DSS	2%	OPEN	180%
M5	GDS	32.18%	DSS	6.38%	OPEN	23%
M6	GDS	-30.5%	DSS	-10.33%	OPEN	NO
M7	GDS	6.38%	DSS	NO%	OPEN	110%
M8	GDS	-30%	DSS	12.5%	OPEN	-20.8%
Cc	SSF	12.5%	-	-	OPEN	-10.39%

ΔC / C: Percentage of the faults injected into component C, Δfosc / fosc: Variation of the oscillation frequency from its nominal value, NO: No oscillation, GDS: Gate – Drain Short, DSS: Drain - Source Short, SSF: Struck Short Fault

The obtained results, presented in table1 show that both short and open faults can be detected with high fault coverage. Table 2 summarizes the fault coverage obtained by oscillation testing in terms of short and open faults injected.It can be seen from the table 2 that the overall fault coverage obtained for all falts injected was 92%.

TABLE 2
SIMULATED FAULT COVERAGE OF OSCILLATION TESTING

FAULT TYPE	TOTAL FAULTS INJECTED	FAULTS DETECTED (WITH OSCILLATION)	FAULTS DETECTED (WITHOUT OSCILLATION)	FAULTS UNDETECTED (WITH OSCILLATION)	FAULT COVERAGE
SHORT	17	13	2	2	88.23%
OPEN	9	7	2	0	100%
TOTAL	26	20	4	2	92.3%

6 CONCLUSION

In this paper, we have proposed a vectorless, dynamic DFT technique for low voltage two stage operational transconductance amplifiers, based on converting the circuit into an oscillator using wein-bridge oscillator. The OBT technique needs only measurement of the frequency deviation to detect faults. Hence requires short test times and has good immunity to noise. The design is easily implemented with little area overhead and has negligible impact on circuit performance. Fault simulation results show that the proposed oscillation-based test technique provides high fault coverage of 92% and is capable of simultaneously detecting single and multiple faults. The advantage of the proposed solution is that they require only minor circuit changes and is a vector-less solution for fault detection.

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