Design of Temperature Sensor Using Ring Oscillator

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Abstract- This paper presents the design of a low cost temperature sensor based on ring oscillator. It exploits the frequency of the ring oscillator that is proportional to temperature which is displayed in the form of a digital output. The proposed CMOS temperature sensor comprises a ring oscillator, a voltage level shifter, a 10-bit counter, and a 10-bit register. The designed ring oscillator is frequency-tunable and the voltage level shifter provides the output to full-scale to make sure that the number of its rising edge is counted by the counter. The register saves the counted output.

Index Terms— Charge Recycling, Noise Shaping, Ring Oscillator, Temperature Sensor.

1. INTRODUCTION

THE block diagram representation of a CMOS temperature sensor is shown in Fig. 1. Proposed ring oscillator generates a clock signal which is proportional to the change in temperature. A current-starved inverter with 4-digit tunable inputs makes the ring oscillator frequency-tunable. The voltage level shifter makes sure that the number of its rising edge is counted by the counter. The register saves the counter output at every positive edge of the external clock. The difference between two successive outputs of the register indicates the temperature [1][2][3].

2. EXISTING RING VCO

A ring oscillator consists of odd number of delay stages with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and must have unity voltage gain at the frequency of oscillation. The total delay is equally divided among all stages. So each delay provides a phase shift of π /N, where N is the number of delay stages.

The remaining π phase shift is provided by a DC inversion. The most basic ring oscillator is simply a chain of single ended digital inverters. This circuit is shown in Fig. 2. To provide the DC inversion, an odd number of stages must be used. To see why this circuit will oscillate, assume that the output of the first inverter is a '0'. Therefore, the output of the Nth inverter, where N is odd, must also be '0'. However, this output is also the input to the first inverter, so the first inverter's output must switch to a '1'. By the same logic, the output of the last inverter will eventually switch to a '1', switching the output of the first inverter back to '0'. This process will repeat indefinitely, resulting in the voltage at each node oscillating.

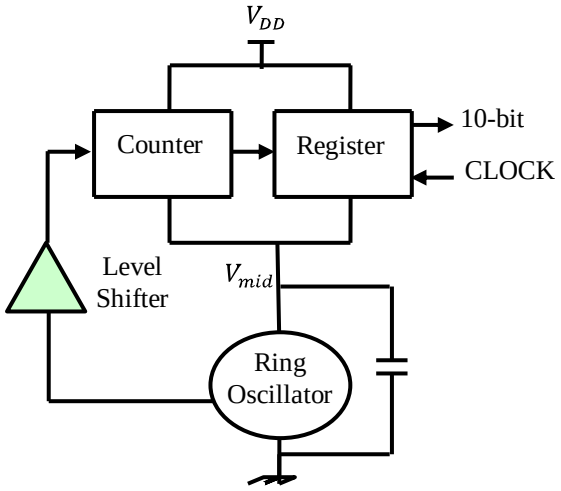

Fig.1. Schematic of proposed temperature sensor

To determine the frequency at which this circuit will oscillate, the delay provided by each inverter cell is $2\tau_d$. The signal must go through N inverters, each with the delay τ_d, for a total time of $N\tau_d$, to obtain the first 2π phase shift. Then, the signal must go through each stage a second time to obtain the remaining π phase shift, resulting in a total period of $2N\tau_d$. The frequency is the reciprocal of the period, resulting in the frequency as

$$f = \frac{1}{2*N*t_d} \quad (1)$$

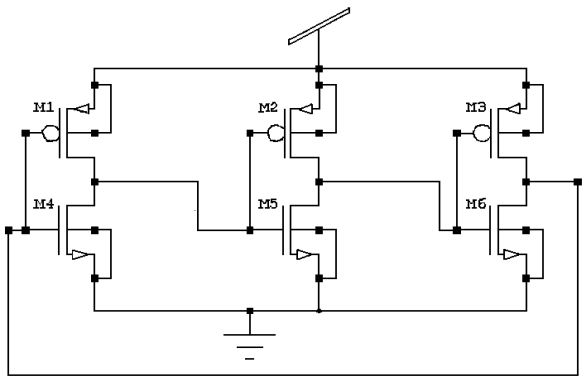

Fig 2. Existing Ring Oscillator

Fig. 2 shows the existing ring oscillator employing three delay stages. Each inverter consists of an $nMOS$ transistor and a $pMOS$. This basic structure has oscillation frequency f_{osc} mainly limited by the transit response of the $pMOS$, whose mobility is two to three times lower than its $nMOS$ counterpart. A very simple way, namely negative skew, has been proposed [5] to improve its frequency performance. It consists of introducing a negative delay element to boost the high-to-low transition and thus to compensate $pMOS$ devices' performance. Tuning is possible only if auxiliary devices are added to implement a current starved inverter, which will also lead to the increase of power dissipation and phase noise.

Fig. 3 shows the waveform of an existing ring oscillator. Table I give the frequency of oscillation for different bias voltages.
To make this circuit useful, the oscillation frequency must be controllable.

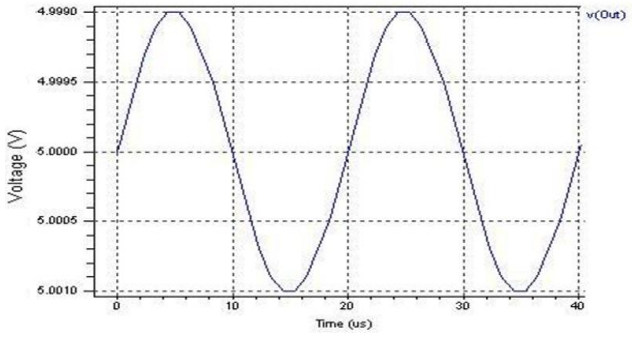

Fig. 3. Waveform of Existing Ring Oscillator

FREQUENCY OF OSCILLATION OF EXISTING RING OSCILLATOR WITH RESPECT TO DC BIAS VOLTAGE

DC bias voltage (Volts)	Peak to peak voltage(Volts)	Time Period(μs)	Frequency of oscillation(kHz)
5.0	0.0243 to 4.97	14.5	11.49
4.5	0.0265 to 4.97	14.58	11.43
4.0	0.0290 to 4.97	15.58	10.69
3.5	0.0306 to 4.98	16.01	10.41
3.0	0.0258 to 4.98	16.09	10.35
2.5	0.0205 to 4.98	16.5	10.1
2.0	0.0397 to 4.97	16.58	10.05
1.5	0.0425 to 4.97	16.8	9.92
1	0.0482 to 4.99	16.88	9.87
0	4.990 to 5.010	17	9.8

3 .PROPOSED RING VCO

The proposed schematic 3-stage voltage controlled ring oscillator ($VCRO$) is shown in Fig. 4. The circuit was simulated using 0.35μm $CMOS$ technology. Both $nMOS$ and $pMOS$ transistors of the inverters are of the same size. The proposed oscillator (with a 3V gate voltage bias for M4) exhibits an oscillation frequency of 27.36 MHz against 10.35 kHz for the existing one. It corresponds to a considerable increase in the frequency of oscillation and the bandwidth also increases as compared to existing one. The oscillation frequency of the proposed oscillator can be tuned through gate control of M3.

The proposed Ring Oscillators in both parts are constructed with a chain of current-starved inverter stages, while the bias current generators are of different structures. The bias current generator in the upper part provides the ring oscillator with a proper bias current to allow its oscillation period to be proportional to temperature (Fig. 4).

The input voltage is varied from 0 to 5V, in steps of 0.5V and then time period at different values of voltages from the waveform (Fig.5) can be obtained. After that frequency is calculated by taking inverse of the time period. Table II shows values of time periods and frequencies for different values of voltages.

TABLE I

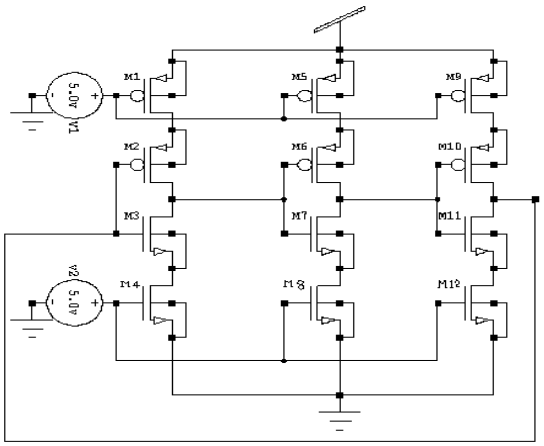

Fig.4. Structure of proposed CMOS ring oscillator with current-starved inverter stages

TABLE II.
VARIATION OF FREQUENCY WITH VARIATION IN INPUT VOLTAGE OF PROPOSED RING VCO

DC bias voltage(Volts)	Peak to peak voltage(Volts)	Time period(ns)	Frequency of oscillation(MHz)
5.0	0.0243 to 4.97	30.51	54.62
4.5	0.0265 to 4.97	31.47	52.96
4.0	0.0290 to 4.97	33.12	50.32
3.5	0.0306 to 4.98	36.8	45.28
3.0	0.0258 to 4.98	43.8	38.05
2.5	0.0205 to 4.98	53.28	31.28
2.0	0.0397 to 4.97	54.61	30.51
1.5	0.0425 to 4.97	54.92	30.34
1.0	0.0482 to 4.99	59.03	28.23
0.0	4.990 to 5.010	59.09	28.20

A layout (a geometric representation) of the circuits is done using the previous design which is showing better performance among all designs, and simulate the design again after layout. In this way we included 2nd order effects that take place in real life and can better estimate our design performance. We do LVS (Layout versus Schematic) checks to make sure that their layout design corresponds to the same behavior as our simulated design. Basically, without layout, the design will never work properly in real life.

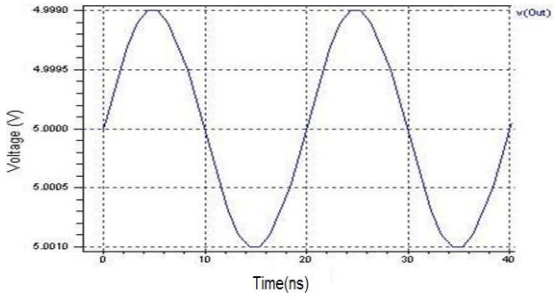

Fig.5. Output Waveform of proposed Ring VCO

Fig. 6 shows the layout diagram of Proposed Ring VCO and Fig. 7 shows the corresponding waveform.

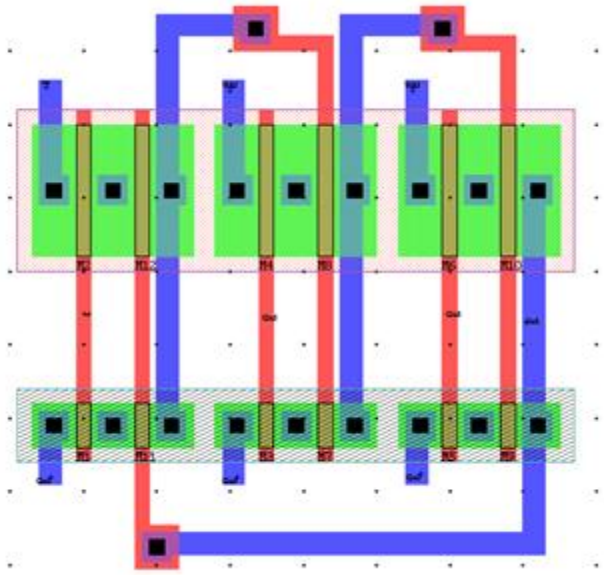

Fig.6. Layout Diagram of proposed ring VCO

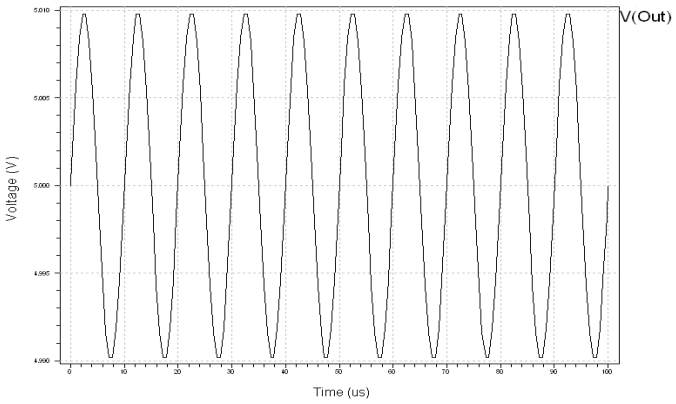

Fig.7. Output Waveform of proposed Ring VCO

4. WORKING PRINCIPLE

The high-to-low and low-to-high propagation time for a CMOS NOT gate can be expressed as;

$$t_{PHL} = \frac{2C_L V_{tn}}{k_n(V_{DD}-V_{tn})^2} + \frac{C_L}{k_n(V_{DD}-V_{tn})} ln\left[\frac{1.5V_{DD}-2V_{tn}}{0.5V_{DD}}\right] \quad (1)$$

$$t_{PLH} = \frac{-2C_L V_{tp}}{k_p(V_{DD}+V_{tp})^2} + \frac{C_L}{k_p(V_{DD}+V_{tp})} ln\left[\frac{1.5V_{DD}+2V_{tp}}{0.5V_{DD}}\right] \quad (2)$$

$where\ k_n = \mu_n C_{OX}\left(\frac{W}{L}\right)_n\ and\ k_p = \mu_p C_{OX}\left(\frac{W}{L}\right)_p$ and $C_L =$ load capacitance

$$t_p = \frac{t_{PHL}+t_{PLH}}{2} = \frac{C_L}{k(V_{DD}-V_t)} ln\left[\frac{1.5V_{DD}-2V_t}{0.5V_{DD}}\right] = \frac{C_L}{\mu C_{OX}(V_{DD}-V_t)}\frac{L}{W} ln\left[\frac{1.5V_{DD}-2V_t}{0.5V_{DD}}\right] \quad (3)$$

$$\mu = \mu_o\left(\frac{T}{T_o}\right)^m, where\ m = -1.2\ to\ -2.0$$

Fig.4 shows the structure of the proposed ring oscillator for the temperature sensor, which is composed of an odd number of current-starved inverter stages with a bias current generator. The rise and fall delays of a single inverter stage in the oscillator are determined by the inverter bias current I_{Source} (I_{Sink}), the load capacitance C_{load}, and the inverter trip voltageV_{tp}.

$$t_{rise} = \frac{C_{load}*V_{trip}}{I_{source}} \quad (4)$$

$$t_{fall} = \frac{C_{load}*(V_{DD}-V_{trip})}{I_{source}} \quad (5)$$

$where\ V_{rtip} = 50\%\ V_{out}$

Now, the oscillation frequency of the ring oscillator, composed of N current-starved inverter stages, can be represented as

$$f_{osc} = \frac{1}{N*(t_{rise}+t_{fall})} = \frac{I_{source}}{N*C_{load}*V_{DD}} \quad (6)$$

The Eq. (6) indicates that the oscillation frequency of the ring oscillator is linearly dependent on the inverter bias current. Namely, if the amount of current provided by the bias current generator has a positive coefficient to temperature, the oscillation frequency will also have a positive coefficient. If the current provided by the bias current generator is constant irrespective of temperature variation, the oscillation frequency will also be temperature independent.

5. CHARGE RECYCLING

Due to the need of DC to DC converter, low supply voltage such as 0.3V for sub threshold operation is not practical when the sensor is designed as a part of a system. In addition, simply increasing the supply voltage cannot be a smart solution, because when the supply voltage is increased N times, power consumption is multiplied by N^2. Taking into account the increased frequency of ring oscillator in accordance with the increased supply voltage, further increase in power consumption is inevitable [7]. Since there is no voltage regulator to source or sink charge from the intermediate node, V_{mid} is self-determined by the inherent charge balance between the top and bottom circuits [8].

Another feature of the proposed circuit based on the increment of V_{mid} as temperature increases. That is because when temperature increases, power consumption of the top circuits increases more rapidly than the bottom circuits, triggering the charge balancing action to make V_{mid} higher to decrease the power consumption of the top circuits and increase the power consumption of the bottom circuits, finally equalizing them [9]. This property has a positive effect on the resolution, since higher V_{mid} leads to higher ring oscillator frequency, and in turn higher frequency-to-temperature gain of the oscillator. Also, lowest power consumption can be achieved by adjusting V_{mid} at the lowest target temperature to become the lowest voltage headroom for the bottom circuits through balancing the top and bottom circuits. Although it is not essential, placing a decoupling capacitor between intermediate node and ground also has a positive effect on the sensor because it stabilizes V_{mid}.

6. NOISE SHAPING

Since the counter is free-running without any reset signal, the current quantization noise is correlated with the previous one. As a result, just as the conventional VCO-based ADC which consists of a VCO and a counter, the proposed temperature sensor has the first-order noise shaping property [10]. In this case, the noise transfer function (NTF) is given by

$$NTF(z) = 1 - z^{-1} \quad (7)$$

This Eq. (7) is high-pass whereas the signal transfer function (STF) is all-pass. The counter output is saved in the register at every rising edge of the clock signal. The current register output is subtracted by the previous one and several outputs are added to produce a single value representing the temperature. The number of outputs used for adding directly affects the resolution.

Therefore, when the perfect linearity of the temperature sensor is assumed, the resolution can be expressed as

$$Resolution = \frac{T_{max}-T_{min}}{O_{max}-O_{min}}\frac{1}{N} \quad (8)$$

where T_{max} and T_{min} is the maximum and minimum temperature in the target range, respectively, O_{max} and O_{min} is the maximum and minimum output value before adding and N is the number of added outputs.

7. VOLTAGE LEVEL SHIFTER

The voltage level shifter which is used in the proposed temperature sensor circuit extends the reduced voltage level of the ring oscillator output to full-scale to make sure that the number of its rising edge is counted by the counter as shown in Fig. 8.

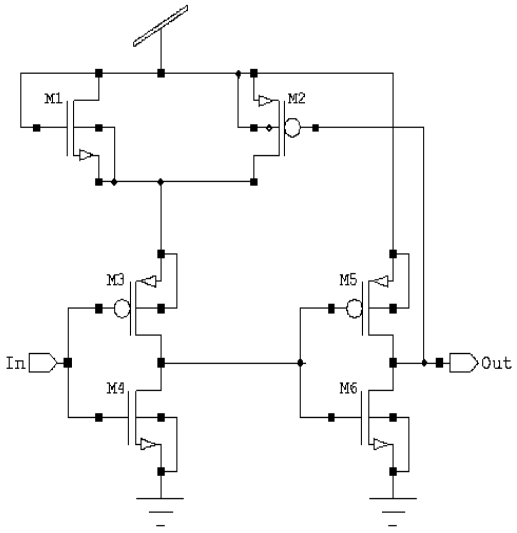

Fig.8. Circuit diagram of voltage level shifter

The level shifter in an integrated circuit translates a binary input signal having a low voltage level to a binary output signal having a different voltage level. The level shifter includes an input stage that receives the input signal (Fig. 9) and provides control signals (Fig. 10) to a low state voltage translation circuit and a high state voltage translation circuit. The low state voltage translation circuit controls the level shifter when the input signal is low and provides a bias signal to a bipolar device adapted to pull the external output signal low. The high state voltage translation circuit controls the level shifter when the input signal is high and includes a voltage reducing circuit operating as a current mirror with a pull-up $pMOS$ transistor to couple an internal high voltage power supply to the output node (V_{out}).

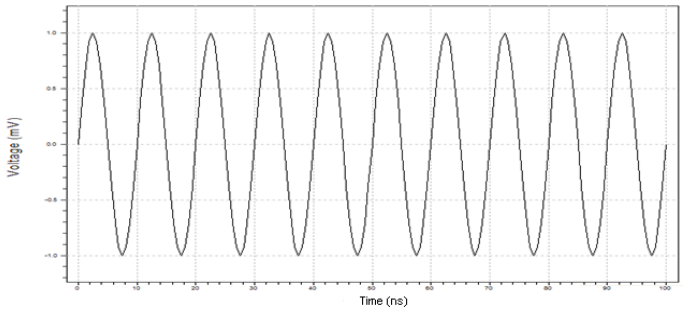

Fig.9. Input Waveform of voltage level shifter

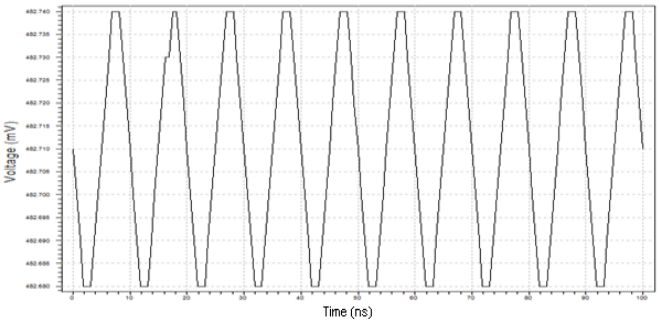

Fig.10. Output Waveform of voltage level shifter

Buffer circuits or level shifters for converting a signal having an input voltage level into a signal having a different predetermined voltage level are commonly used as input buffers in semiconductor devices and have been designed to interface between circuitry of two different voltage levels.

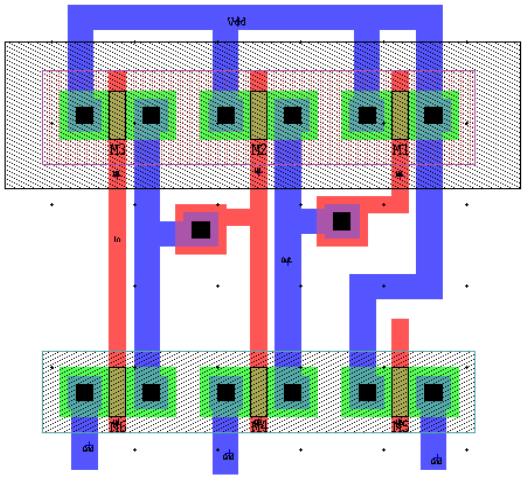

Fig.11. Layout Diagram of voltage level shifter

The layout diagram of voltage level shifter is drawn using W-edit as given in Fig.11. and corresponding output waveform corresponding to the layout is given in Fig.12.

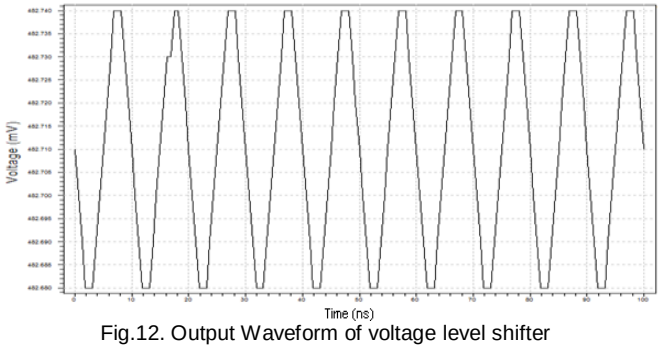

Fig.12. Output Waveform of voltage level shifter

8. COUNTERS AND REGISTER

The counter and register is designed using D Flip-Flop as shown in Fig. 13 and the output waveform of the corresponding D Flip-Flop is shown in Fig. 15.

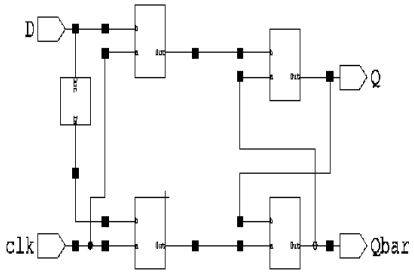

Fig.13. Schematic Diagram of D Flip- Flop

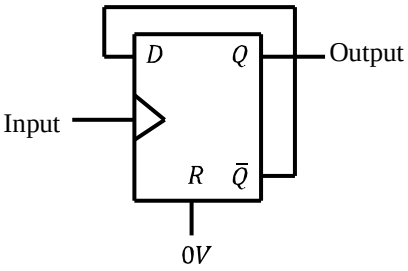

Fig.14. Block diagram of 1-bit counter

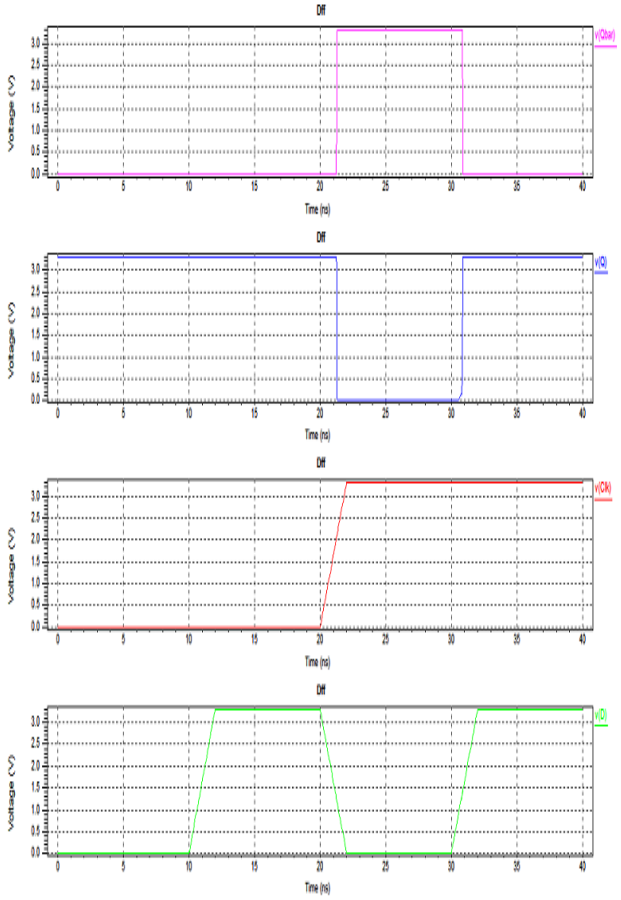

Fig.15. Waveform for D Flip-Flop

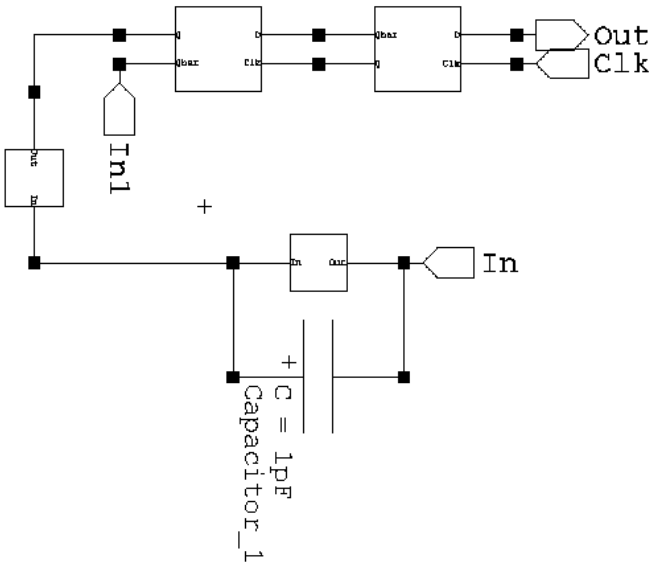

Fig.16. Schematic Diagram of Proposed Temperature Sensor

Fig.16 is the schematic view of proposed temperature sensor and Fig.17 shows the Temperature variation with respect to Oscillation Frequency.

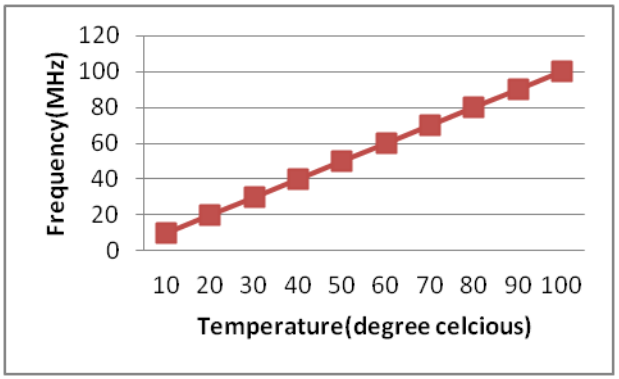

Fig.17. Temperature Characteristic of Ring Oscillator showing Frequency of Oscillation Linear to Temperature

9. CONCLUSION

A low power ring oscillator-based $CMOS$ temperature sensor has been presented. The proposed temperature sensor occupies smaller silicon area with higher resolution than the conventional temperature sensor based on band gap reference. Extremely low power consumption is achieved through charge recycling, which is to stack circuits and make each circuit to actually operate within $0.3\sim0.5V$ voltage headroom, although the supply voltage is $0.8V$. Ring oscillator and counter in the sensor composed first-order noise shaping property just like the VCO-based$ADCs$. Simple structure allowed the proposed temperature sensor to feature low power and small chip area while having high resolution.
Ring oscillators are basic building blocks of complex integrated circuits. They are mainly used as clock generating circuits. The proposed $VCRO$ has full range voltage controllability along with a wide tuning range and is most suitable for low-voltage operation due to its full range voltage controllability.

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