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Design and Simulation of DLL with Double Edge Synchronization in 0.13µm CMOS Technology

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Abstract— This paper describes a wide-range, low-power and low-jitter delay-locked loop (DLL) with double edge synchronization which is mainly used in clock alignment process. Double edge synchronization method has its own advantages and disadvantages. Using two PFDs, two CPs and two loop filters in double edge DLLs increases the jitter and power consumption. In order to overcome these challenges, in this article proper blocks were used for the proposed DLL circuit. Therefore, the results of the most important items of proposed double edge DLL are as well as the results of the single edge DLLs in most articles. All the simulation results are based on 0.13µm CMOS technology with 1.2v supply voltage. The HSPICE simulation results show that the proposed DLL circuit generates clock signals ranging from 750MHZ to 1GHZ. The maximum power consumption of the DLL circuit at 1GHZ is 3.1mW. The maximum and minimum of rms jitters are 17.5 and 2.5ps and the maximum and minimum of peak-to-peak jitters are 125.3 and 19.7ps, respectively. The locking time of proposed DLL is less than 60ns within the operating frequency band. Another feature of this architecture is that it has good duty-cycle correction capability (50±1%).

Index Terms— Delay-Locked Loops (DLLs), PLL, locking time, jitter, multistage clock buffer, voltage-controlled delay line

1. INTRODUCTION

IN the high-speed generation and high-integration density systems, the synchronous adjustment between the systems is very important. Asynchronous clock which were caused by the phase error would be a serious threat to the correctness of the operation of the whole circuit. The phase-looked loop (PLL) and delay-locked loop (DLL) are the most commonly adapted to the most commonly adopted to the purpose of clock synchronization [1], and they have been widely used in high-speed applications, such as memory ICs, communication ICs, microprocessors, network processors, etc.

Ordinarily, if there is no frequency multiplication, using DLL for signal synchronization would be the better choice than PLL. Because DLL is a first order control system, it's more stable and easier to design. Moreover, PLL suffers from a later locking time and jitter accumulation due to the closed loop voltage-controlled oscillator (VCO). On the other hand, the DLL using the voltage-controlled delay line (VCDL) instead of the VCO does not accumulate over many clock cycles, therefore, DLL exhibits better jitter performance than PLL. In addition, DLL have smaller area and faster locking time than the PLL [1]. Low power, wide lock range, short locking time, and low jitter are the focuses of DLL design. In order to achieve low jitter operation, DLL designs require delay stage design with low supply and substrate noise sensitivity and good matching between the up/down CP currents [2].

In this work, a DLL structure with double edge synchronization with clock alignment capability of both rising and falling edges is proposed. In the rest of the paper, section 2 of the paper describes architecture of DLL with clock alignment capability of both rising and falling output pulse edges. Section 3 concentrates on implementation of proposed structure. Section 4 includes simulation results by HSPICE simulation, and conclusions are given in section 5.

2. ARCHITECTURE OF PROPOSED DLL

The building block of a conventional analog delay loop with double edge synchronization is shown in Fig. 1. This structure of DLL circuit has clock alignment capability of both leading and trailing output pulse edges. A clock aligner's task is to phase-align a chip internal clock with a reference clock, effectively removing the variable buffer delay and reducing uncertainty in clock phase between communicating VLSI IC constituents [3].

Constituents of Fig. 1 are: a voltage controlled delay line, VCDL, two differential charge- pumps, CP1 and CP2, two first order low-pass filters, LPF1 and LPF2, and a multistage clock buffer (MCB). The reference clock, CLK-ref, is propagated through VCDL and MCB. The output signal, CLK-out, is compared through with the reference input. If the delay difference from integer multiples of clock period is detected, the closed loop will automatically correct it by changing the delay time of the VCDL [4].

According to Fig. 1, in first stage two PFDs are shown. Their function is to compare phase-frequency of rising or falling edges between the input (CLK-ref) and output (CLK-out). Note that the phase-frequency detector 1 (PFD1) is sensitive to a rising and phase-frequency detector 2 (PFD2) is sensitive to a falling pulse edge. These PFDs have high-speed and small dead-zone. Hence, the DLL circuit has very fast lock feature

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compared to other dynamic PDs [3, 5]. In the next stage, two ideal charge-pumps and two low-pass filters sketched in Fig. 1. UP1 and UP2 pulses cause Ip to add charge to the capacitors of LPF1 and LPF2, while DN1 and DN2 function is to discharge the capacitors. The output of CP1 and CP2 are Vctrl1 and Vctrl2, and they are connected to the VCDL control input (Vbn and Vbp). In the last stage of this figure, VCDL and MCB blocks are shown. The control input voltages of VCDL (Vbn and Vbp) can regulate the rising or falling clock pulse edge.

3. CIRCUIT STRUCTURE

3.1 Phase-Frequency Detector (PFD)

The PD function is to detect the phase difference between the reference clock signal and the feedback clock. PD can detect the skew of the clock, and it can be analog or digital as well. Nowadays digital phase detectors have become more popular. As its name indicates, PDs are sensitive to the phase difference between two signals, but they are not sensitive to frequency. Practically phase detector can work as frequency detector but with limited range. Thus, it is preferred to replace the phase detector with phase-frequency detector. On the other hand, many PFDs have a large dead-zone. As we know, dead-zone occurs when the loop does not respond to small phase errors. Each width of the dead-zone directly feeds to jitter in the DLL and should be avoided. Hence, this kind of PFDs cannot be used at high frequencies.

To overcome the speed limitation and reduce the dead-zone, we proposed high-speed PFDs which are sketched in Fig. 2. These schematics have fast-lock loop feature. In this work, PFD1 [6] is used to detect a rising pulse edge. We needed another PFD for falling edge, therefore, we proposed new phase-frequency detector (PFD2) to detect a falling pulse edge. Hence, PFD1 (Fig. 2 (a)) is sensitive to rising clock pulse edge, while PFD2 (Fig. 2 (b)) is sensitive to the falling edge. The width of UP and DN signals are proportional to the phase-frequency of the input signals [7]. PFD1 and PFD2 have three states. As shown in Fig. 3(a), (b) and 4(a), (b) both reference and output have the same frequency but with phase differences, while in Fig. 5(a), (b) and 6(a), (b) both signals have different frequencies and phases. There is another state, which is when both signals have the same frequency and phase (Fig. 7).

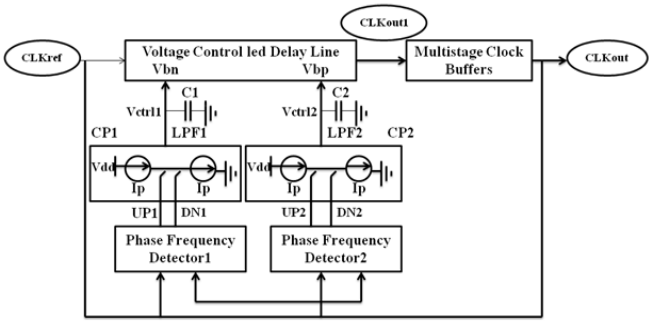


Fig. 1. DLL's structure with double edges synchronization.

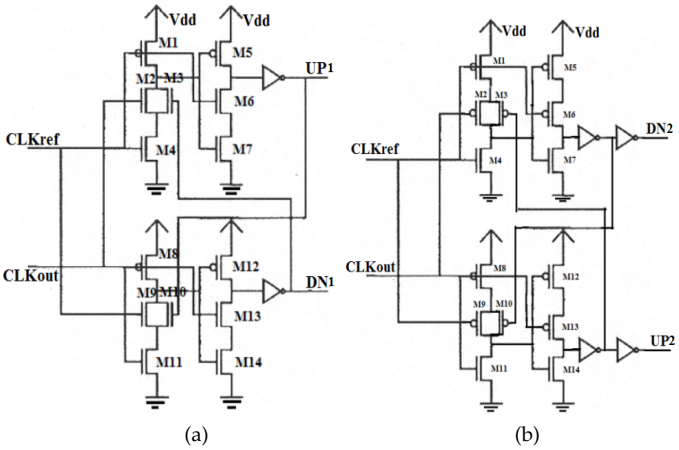


Fig. 2. Phase-frequency detectors for (a) raising and (b) falling edges.

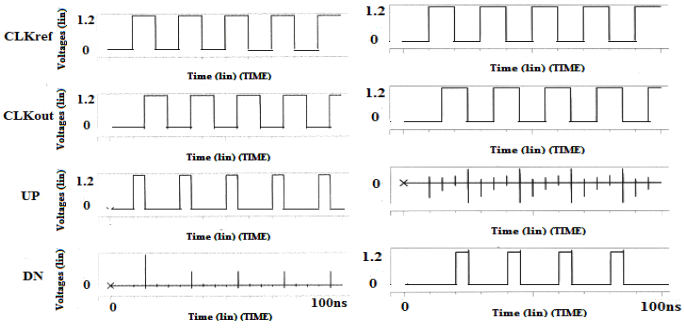


Fig. 3. Behavior of (a) PFD1 and (b) PFD2 with same frequency (CLK-ref leads).

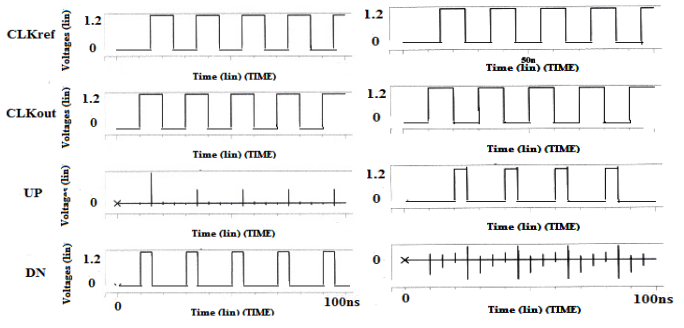
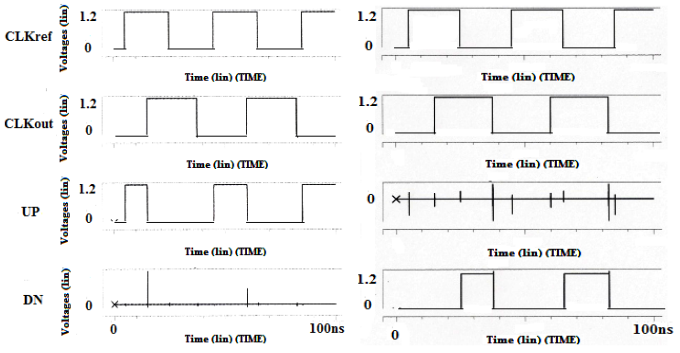
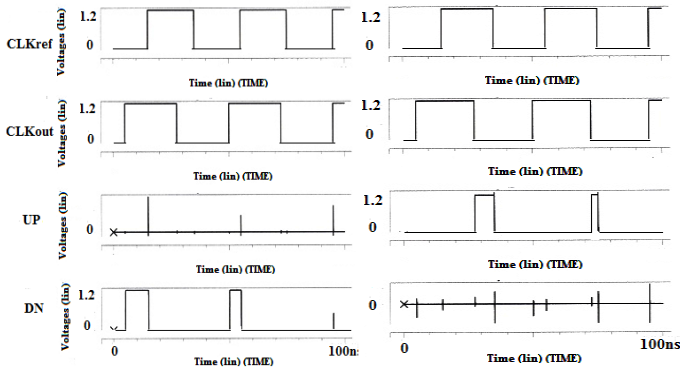


Fig. 4. Behavior of (a) PFD1 and (b) PFD2 with same frequency (CLK-ref lags).



(a) (b)

Fig. 5. Behavior of (a) PFD1 and (b) PFD2 with different frequencies (CLK-ref leads).



(a) (b)

Fig. 6. Behavior of (a) PFD1 and (b) PFD2 with different frequencies (CLK-ref lags).

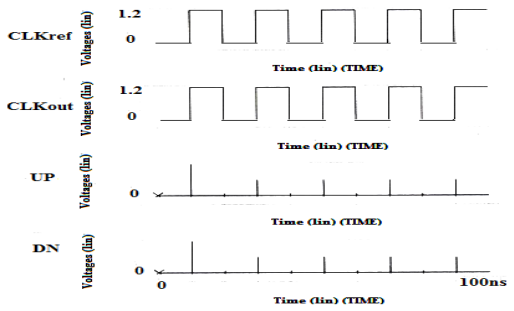
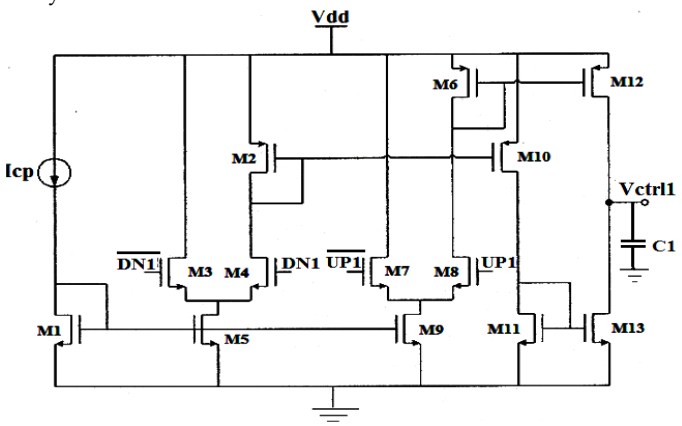


Fig. 7. Behavior of PFD1/PFD2 with same frequency and phase.

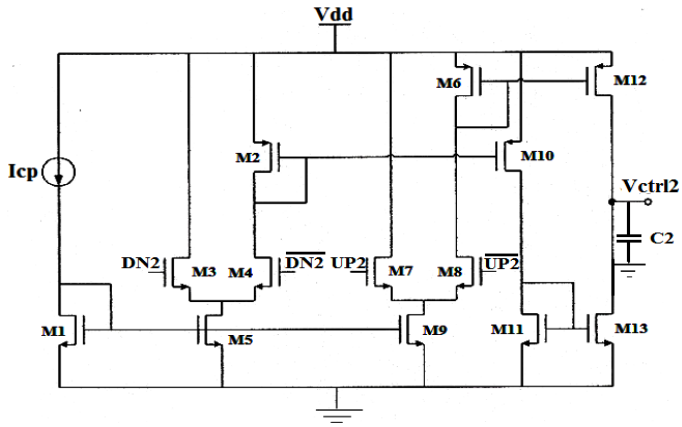
3.2 Charge-Pump and Loop Filter (CP and LPF)

Charge-pump design is one of the most complicated parts of the DLL structure. The charge-pump controls the charging/discharging current by UP/DN signal from PFD, and uses the phase difference between the up and down signals from the PFD to convert the phase error into current. Then, loop filter converts the current into the control voltage, by charging or discharging the capacitor and sending it to Vctrl to set the VCDL delay. Two differential charge pumps (CP1 and CP2) are used, because in this work, they seem more proper choice and the advantage of these structures is that switching time is improved by using the current steering switches. CP1 is depicted in Fig. 8(a). This charge-pump can be used for rising edge [8]. Therefore, we needed another charge-pump for falling edge, and we proposed CP2 (Fig. 8(b)) to detect falling pulse edge.

One of the possible filters is a RC low-pass filter, like the filter mentioned in [9]. But in this work two simple capacitors are used as low-pass filters, and they are adjusted to be C1=C2=2pF. As we can seen in Fig. 1, the equivalent model of the charge-pump and low-pass filter consists of a source current, a sink current and two switches controlled by PFD output. When the output phase of the DLL circuit leads the reference phase, the current source switch opens and the current sink switch closes. Thus, the voltage in the capacitor decreases. The voltage in the capacitor increases if the reference phase leads the output phase. In this work, we adjusted source current and sink current to be ICP-up=ICP-down=100μa. Each charge-pump can charges or discharges their filter capacitors. Vctrl1 and Vctrl2 (Vbn and Vbp) are the voltages on capacitors C1 and C2 respectively, and sets the VCDL stage propagation delay.



(a)



(b)

Fig. 8. Implementation of charge-pump for (a) raising and (b) falling edges.

3.3 Voltage controlled Delay Line (VCDL)

The most critical component in the performance of DLL is VCDL. A VCDL can influence DLL action. Therefore, VCDL can influence DLL stability and jitter performances. The implementation of a VCDL is composed of several variable delay elements connected in series. There are several examples of buffer elements [10], such as cascade delay cell, differential delay cell, shunt capacitor delay cell, etc.

The VCDL used in this work (Fig. 9) is a modified current starved delay element. In our approach, both Vbn and Vbp, directly drive gates of M3 and M4 MOS transistors, respectively. Transistors M5 and M6 act as symmetric loads and are used for two purposes: (a) to make linear a voltage-to-delay transfer function of the normal current starved delay element and (b) provides correct initial condition for DLL operation even in a case when both control voltages Vbn and Vbp are out-of-regulation limits (for example, M3 and M4 are switched off).

In high-speed design a multistage clock buffer implemented with a long inverter chain is often needed to drive a heavy capacitive load. For these designs, as well as for applications in which the timing of both edges of the clock is critical, it is difficult to keep the clock duty-cycle at its ideal value of 50%, primarily due to various asymmetries in signal paths and unbalances of the p and n transistors in the long buffer. As a consequence the clock duty-cycle will deteriorate from 50%, and in the worst case, the clock pulse may disappear inside the clock buffer, as the pulse width becomes too narrow or too wide [3]. As can be seen in Fig. 1 the output of VCDL (CLK-out1), is an input for MCB and the output of MCB (CLK-out), interns to PFD1 and PFD2. The VCDL and MCB were implemented as a chain of ten delay elements (five VCDL and five MCB).

Time delay variation of the leading and trailing pulse edge term of control voltage Vctrl (Vbn and Vbp) is presented in Fig. 10. If the control voltage Vctrl, decreases, the time delay of the trailing edge increases and time delay of leading edge decreases and vice versa.

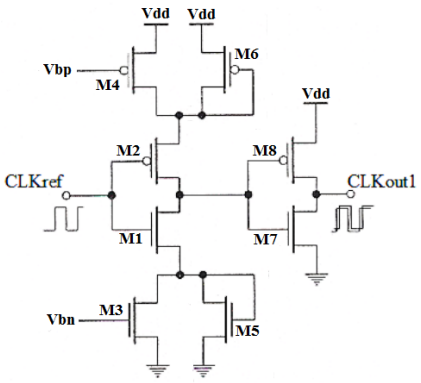


Fig. 9. Modified current starved element.

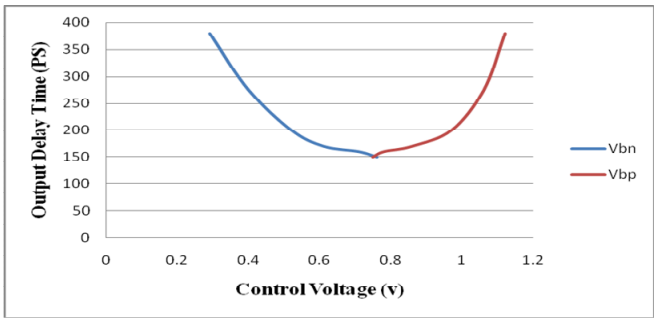


Fig. 10. Output rising and falling edge delay versus frequency.

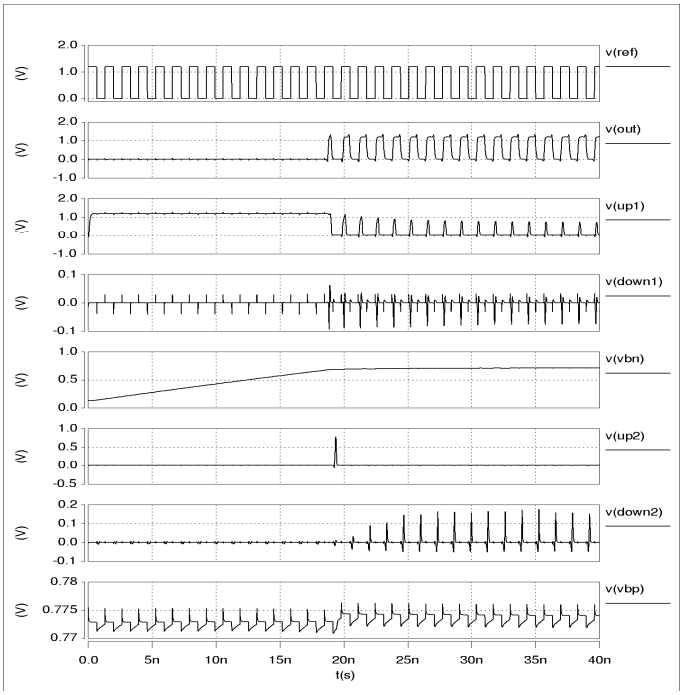
4. SIMULATION RESULTS

The proposed DLL structure with double edge synchronization is implemented in 0.13µm CMOS technology, with the supply voltage of 1.2V. The operational frequency range is from 750MHZ to 1GHZ. Fig. 11 shows the result of DLL operation at (a) 750 MHZ and (b) 1 GHZ. In Fig. 11 illustrates the behavior of CLK-ref and CLK-out, and waveforms of UP1 (UP2), DN1 (DN2). Also, this figure shows the behavior of charge-pump's output (Vctrl1 and Vctrl2). As can be seen from UP1 and DN1 (UP2 and DN2) signals define the control voltages Vctrl1 (Vctrl2). The locked time of DLL is less than 60ns within the operating frequency band. This circuit also has good duty-cycle correction capability. As shown in Fig. 12, within the full operating range, the duty cycle error is less than ±1%. Fig. 13 and Fig. 14 show output rms jitter and peak-to-peak jitter versus operation frequency. As can be seen, in low frequencies until the middle frequency range (875MHZ), both jitters are increasing. But when frequency becomes bigger than 875MHZ, both jitters are decreasing. Fig. 15 shows power consumption variation during the frequency range of DLL. Unlike rms and peak-to-peak jitter, power consumption increases proportional to frequency in whole of operation range. The maximum and minimum power consumption at 750MHZ and 1GHZ are 1.8mW and 3.1mW, respectively.

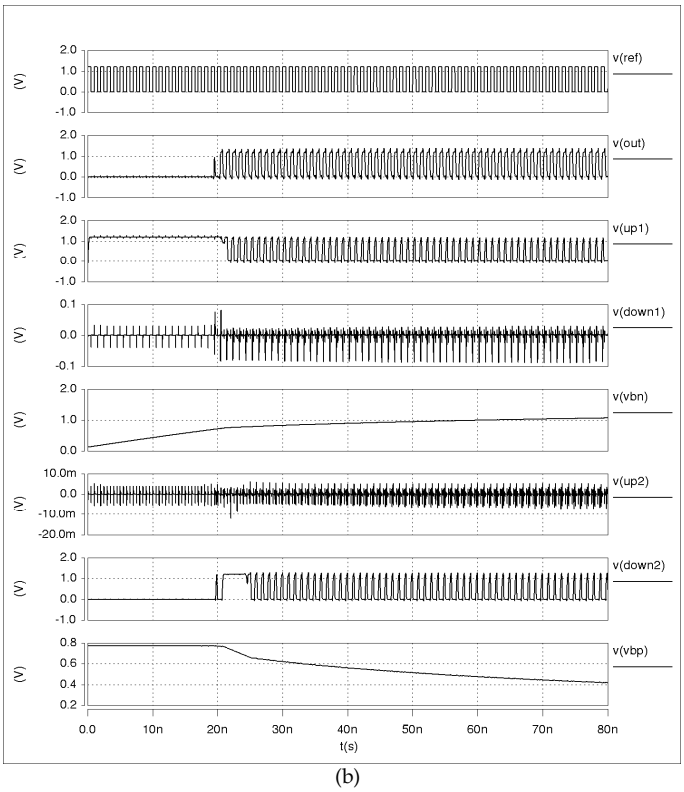
Table 1, gives the performance summary of the proposed PWCL and the characteristics of other published PWCLs. As it can be seen, reference [3] is also double edge synchronization DLL. In this work, approximate architecture proposed in this reference is used, but with more proper blocks and different process to improve important items of DLL. Therefore, compare to this reference, different technology is used, locking time is faster, wider range of frequency is achieved. On the other hand, rms jitter, peak-to-peak jitter and power consumption were computed, which did not mention in reference [3] at all. It can obtain that in this work, good jitter performance and low power consumption are achieved too. In the rest of the table, our work is compared with other references [7, 11, 12, 13].

It must also be pointed out that the reported information for this work are extracted from the simulation results, whereas some of those previously reported works are from the experi-

mental results. So some problems such as parasitic elements, impedance mismatch and calibration errors have been ignored, which could influence the performance of proposed system for future fabrication and test setup.



(a)



(b)

Fig. 11. Simulation of DLL with double edge synchronization at (a) 750MHZ (b) 1GHZ.

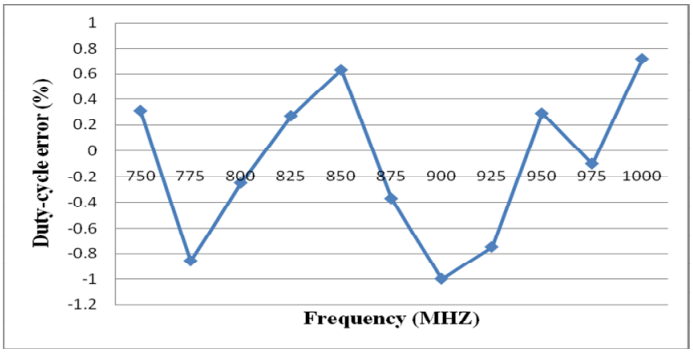


Fig. 12. Duty-cycle error versus frequency.

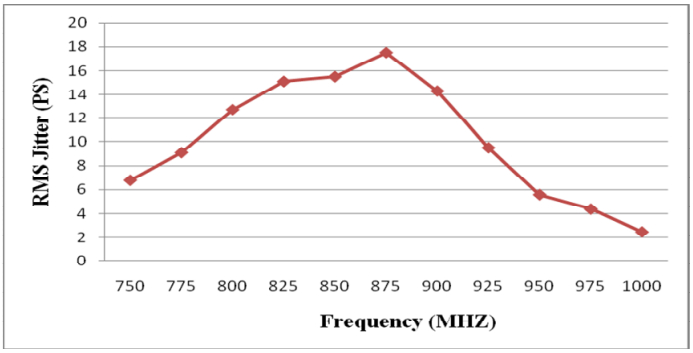


Fig. 13. RMS Jitter versus frequency.

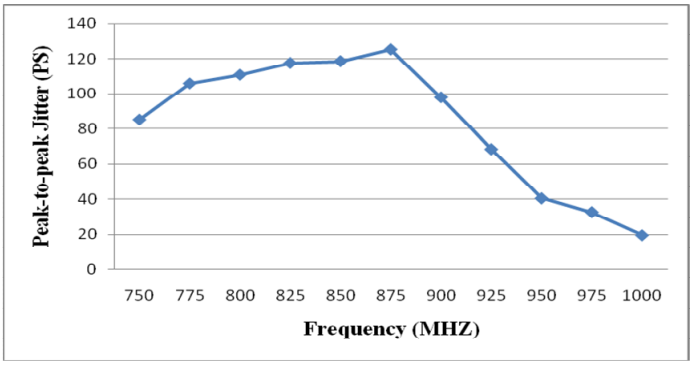


Fig. 14. Peak-to-peak Jitter versus frequency.

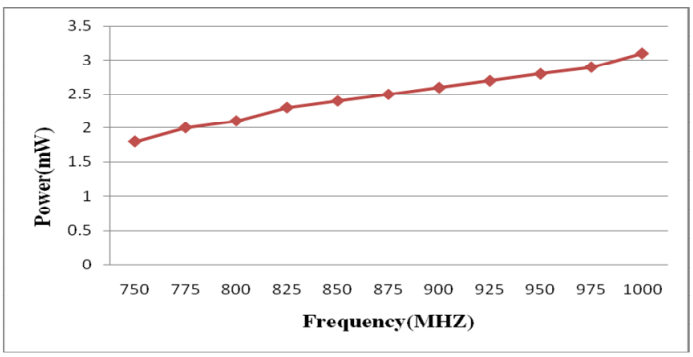


Fig. 15. Power consumption versus frequency.

TABLE I PERFORMANCE COMPARISONS OF PWCLS

References	This work	[3]	[7]	[11]	[12]	[13]
CMOS Process	0.13µm	1.2*m*	0.13*m*	0.13*m*	0.18*m*	0.18*m*
Supply Voltage	1.2V	5V	1.2V	N.A.	1.8V	0.6V
Operational Frequency	0.75-1GHZ	55-166MHZ	0.77-1.05GHZ	15-600MHZ	150-400MHZ	85-550MHZ
Locked Time	<60ns	<200ns	<40ns	N.A.	13 cycles	N.A.
Duty-cycle error	±1%	±8%	N.A.	N.A.	N.A.	N.A.
RMS Jitter	6.8ps@750MHZ 2.5ps@1GHZ	N.A.	N.A.	9ps@600MHZ	25ps@400MHZ	3.8ps @550 MHZ
Peak-to-Peak Jitter	85.2ps@750MHZ 19.7ps@1GHZ	N.A.	1ps@1GHZ	N.A.	N.A.	25.6ps @550 MHZ
Power consump-tion	1.8mW @750MHZ 3.1mW @1GHZ	N.A.	4.38mW@1GHZ	20mW @600MHZ	N.A.	2.4-4.2mW
Singel/Double edge Correction	Double	Double	Single	Single	Single	Single

5. CONCLUSION

In this paper, DLL architecture with double edge synchronization based on 0.13µm CMOS technology at 1.2V power supply is proposed. Operating frequency range is from 750MHZ to 1GHZ. Fast-lock double edge synchronization DLL (maximum 60ns) is achieved by using high-speed double edge phase-frequency detectors (PFD1 and PFD2). Proposed PFDs also have small dead-zone. Also, differential charge pumps (CP1 and CP2) are used; because in this work, they seem more proper choice and the advantage of these charge pumps is that switching time is improved by using the current steering switches. Another feature of this structure is that it has good duty-cycle correction capability (50±1%). On the other hand, double edge synchronization method leads to more power consumption and it can increase rms and peak-to-peak jitter, because of using two PFDs, two CPs and two loop filters instead of one, therefore, in this work analysis of rms jitter, peak-to-peak jitter and power consumption is also implemented. The maximum power consumption of the DLL circuit at 1GHZ is 3.1mW. The maximum and minimum of rms jitters are 17.5 and 2.5ps and the maximum and minimum of peak-to-peak jitters are 125.3 and 19.7ps, respectively. Therefore, double edge synchronization method in DLLs can be used without jitter performance or power consumption challenges.

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