Design and Performance Analysis of a Phase Locked Loop using Differential Voltage Controlled Oscillator

Sudatta Mohanty, Madhusmita Panda, Dr Ashis kumar Mal

Abstract—This paper is based on Phase locked-loop (PLL) using Differential Ring VCO in 350 nm CMOS Technology and illustrates the design process of various blocks of the PLL. The PLL is a closed loop system that compares the phase of an output signal with an input reference signal. PLLs are widely used in order to generate well-timed on-chip clocks to be used in high-performance digital systems. The entire circuit is implemented and simulated using Spice File and the tuning characteristics of the VCO was also verified from which the gain of the VCO was calculated. The estimated lock time of the PLL was found to be 10.02ns and the locking frequency was found to be 693 MHz and the gain of the VCO was estimated to be 120.5 MHz/V.

Index Terms—Phase Locked Loop, Phase Frequency Detector, Charge Pump, Voltage Controlled Oscillator, Loop Filter, Locked State, Unlocked State.

1 INTRODUCTION

A Phase locked loop (PLL) is a closed loop frequency system that locks the phase of the output signal to the reference signal. The term ‘lock’ refers to a constant or zero phase difference between two signals. The basic block diagram of the PLL is shown in the Figure 1. It is a closed loop control system in which the output signal is synchronized with the input signal in terms of frequency and phase. The signal from the feedback path is compared with the input reference signal, until the two signals are locked. If there happens to be a phase difference, then it is called the unlocked state, and the signal is sent to each component in the loop to correct the phase difference.

2 PLL ARCHITECTURE

The major components of the PLL are: (1) The Phase Frequency Detector (PFD), (2) The Charge Pump (CP), (3) The Loop Filter (LPF), and (4) The Voltage controlled Oscillator (VCO). The input to the PLL is a reference signal whose value depends upon the user. The Phase Frequency Detector (PFD), compares the reference signal, and the feedback path, and generates an error signal.

2.1 Phase Frequency Detector

A phase frequency detector (PFD), is a device which compares the phase of two input signals and provides a signal in the form of phase error. It has two inputs which correspond to two different input signals, usually one from a Differential Ring voltage controlled oscillator and other is a reference source. It has two outputs which instruct the subsequent circuitry on how to adjust to lock onto the phase [1].

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The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock.

### 2.2 Charge Pump

The Charge Pump produces a charge which is proportional to the error signal. The function of the charge pump is to take the digital Up and Down pulses from the PFD and convert them into an analog control voltage [2].

The Charge Pump shown in Fig. 3 has only one output, so it is termed as a "single-ended Charge Pump". This Charge Pump consists of a current source, and two switches with inputs directly connected to the outputs of the PFD. The switches control the current from the Charge Pump (Icp) where it is sourced in proportion to the input phase error. The current is sourced through S1 which is controlled by the 'Up' output of the PFD which is therefore termed as the "Up current" (I_{UP}) with S1 being termed as the ‘Up switch’. The current then passes through switch S2 which is controlled by the "Down" output of the PFD [3]. This sink current is thereby termed as the 'Down current' (I_{DN}) with S2 acting as the ‘Down switch’. The Up and Down currents are respectively defined by a current source and current sink to make them constant in order to achieve a desirable loop performance. The combination of S1 and its current source is termed as the ‘Up network’ and the combination of S2 and its current sink is termed the ‘Down network’.

### 2.3 Loop Filter

Loop filter is an important component in PLL, as it affects and determines the loop stability. It also provides the necessary control voltage that is required to adjust the frequency of the VCO. The Figure below shows the RC network, which includes a resistor in series with the filter capacitor. Each time the charge pump drives the R and C1 combination, a current is injected into the filter, and the control voltage experiences a jump.[2] To suppress this effect, a second capacitor (C2) is added in parallel with the resistor.
Figure 8 shows the output of the charge pump/LPF when the up signal is produced. When the up signal is produced from the PFD, then the control voltage of the VCO keeps on increasing and when the down signal is produced, then the control voltage of the VCO keeps on decreasing and when there is no phase difference, then the control voltage remains constant.

### 2.4 Voltage Controlled Oscillator

The voltage controlled oscillator is one of the most important building blocks of the PLL. There are many different implementations of VCOs. One of them is a ring oscillator based VCO. The proposed design for VCO in PLL is based on the Ring VCO, which is used in the clock generation subsystem. The main reason of using the ring oscillator is its ability to integrate easily and due to this integrated nature, the ring oscillator is used in clock recovery data process for serial circuit communication [5].

A ring oscillator comprises of a number of delay stages, with the output of the last stage fed back as the input to the first. To achieve oscillation, the ring oscillator must provide a phase shift of \(2\pi\) and it should have a unity voltage gain at the oscillation frequency. Each delay stage must provide a phase shift of \(\pi/N\).

Where \(N\) is the no of delay stages.

The delay cell is a differential pair with loading and bias controls. The self biased techniques are used to reduce jitter and process variations. This arrangement for extended frequency range VCO results in a large gain of the VCO. The above negative feedback scheme combined with advanced delay cell generates a wide frequency range and low phase noise VCO.

An ideal VCO is a circuit whose output frequency is linear function of its control voltage and this output frequency is represented by the following equation [10] pg 510:

\[
\omega_{\text{out}} = \omega_o + K_{\text{vco}} V_{\text{cont}} \quad (1)
\]

Where \(\omega_o\) represents the intercept corresponding to \(V_{\text{cont}} = 0\) and \(K_{\text{vco}}\) denotes the gain or sensitivity of the circuit which is expressed in rad/s/V.

The tunable range of the VCO can be determined from the characteristics curve shown below:

\[
\text{Tuning range} = \omega_2 - \omega_1 \quad (2)
\]

Where \(\omega_2 = \) Maximum Frequency and \(\omega_1 = \) Minimum Frequency

and Gain of the VCO is given as:

\[
K_{\text{VCO}} \geq \frac{\omega_2 - \omega_1}{V_2 - V_1} \quad (3)
\]

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The output of the above circuit should be differential in nature. As the differential circuits do not yield rail-to-rail outputs, so the differential output has to be converted into a single-ended output.

The output in the above figure shows the oscillations of the VCO. It can be noted from the figure that, when the input is constant, the output frequency is also constant and when there are variations in the input signal, then the output frequency also varies.

2.5 Frequency Divider

It is one of the most important blocks of the PLL circuit. It is normally used for scaling purposes. It divides the VCO frequency in order to generate a frequency which is comparable with reference frequency. It scales down the frequency of the VCO output signal [5]. The output of the VCO is fed back to the input of the PFD via the frequency divider circuit. A simple D flip flop can act as a frequency divider circuit. The figure of a simple DFF based divide by 2 frequency divider circuit is shown below[5].

<table>
<thead>
<tr>
<th>Clk</th>
<th>D</th>
<th>Q</th>
<th>QBar</th>
</tr>
</thead>
<tbody>
<tr>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>1</td>
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</table>
From the output given in figure 17, it can be clearly noted that, the output is yielded significantly as per the truth table given in Table 1.

The combined PLL circuit is shown in the figure below.

The combined circuit of the PLL shown in figure 18 is simulated using Tanner EDA tool whose output in the locked condition is shown in figure 19.

The above figure shows the combined output of the PLL circuit in the Locked state after its complete simulation. As stated above, the locked condition means, there is zero phase difference between the reference and the input frequency signals thus yielding in a constant charge pump output [10].

The Performance Analysis of the entire PLL circuit is shown in Table 2 below:

Table 2 shows the simulated results of the combined PLL circuit where the locking frequency, lock time, and gain of the VCO are listed for better analysis.
3 CONCLUSION

The presented work describes the operation of the PLL and its different components. The simulation studies revealed the behavior of the individual components which were found to be as expected. In this paper, a better lock time was presented. The lock time of the PLL was found to be 10.01ns. The lock time of the PLL mainly depends on the PFD architecture used along with the parameters of the charge pump and the loop filter. So, by properly choosing the PFD architecture and adjusting the charge pump current and loop filter component values, a better lock time can be achieved.

4 REFERENCES