A Study on Carbon Nano-Tube Field Effect Transistor (CNTFETs): A Promising Technology for future ICs

Ritambhara, Yazusha Sharma, Nishi Agarwal, Sandeep Vyas

Abstract—Presently, the low power and high efficiency are imperishable problem in technological gadgets. With the emergence of technologies like 5G and others, it has become requisite to meet the challenge before they are compiled. In this paper we entrust FinFETs, and CNTFETs technologies which are found to be upbeat field of research. The paper presents the performance enhancements of CNTFETs at 14 nm node and discusses the important areas of their applications and future scope.

Index Terms—CMOS, FinFETs, CNTFETs, Simulation, Permittivity, Device Modeling, Device Scalability, MOSFET, Scaling.

1 Introduction

As Gordon Moore predicted, over the last three decades number of transistors in a single chip has been increased from thousand to billion and suggested it doubles every year [1]. International Technology Roadmap for semiconductor in 2015 predicted and stated that in next five years CMOS technology will stop shrinking because industry will not be able to scale CMOS resulting to death impart to Moore’s law [2]. Si-MOSFET based technology has its own limitations like high power density, high leakage current, and decreased gate control resulting them to be inappropriate for ultra-high speed and low power applications. The limitations forced scientists and research to explore other alternatives, FinFETs and CNTFETs has emerged as most promising due to the properties like higher scalability, better performance and higher carrier mobility with suppressed short channel effect. Among the two alternatives CNTFETs are more preferred over FinFETs due to heat dissipation problem, as heat easily gets escalated on the fins. The Carbon the primary constituent of will surpass the silicon the widely employed material in the designing Integrated, Carbon will be the material for future integrated circuits [3],[4]. The advancements in technologies have resulted in high speed multi-core processors, memory storage with greater size and low power devices. Yet, today’s devices based on robotics system, Artificial Intelligence and embedded systems demand higher speeds, much smaller sized IC’s that what is being offered by existing technologies to push boundaries of their performance. To aid the development of such systems, it is necessary for IC technology to scale down the size of transistors and enhance the speed and performance with low power requirements. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) enabled to develop advanced systems like day to day required gadgets like Smart Phones, Laptops, etc., which is prior to the 22 nm node. With 22 nm node technology, further scaling down of MOSFET is not possible due to increased Short Channel Effects (SCE) such as Drain Induced Barrier lowering (DIBL), Impact Ionization, velocity saturation, Channel length modulation, so most of the foundries introduced new type of transistor called Fin Field Effect Transistor (FinFETs), which has less SCE’s, and better control over the channel; this transistor structure is being used in 16 and 14 nm node also. The FinFETs based 14 nm node technology portrays some serious issues, which leads to the degraded performance of the ICs. The Technological advancements era had viewed other alternatives for MOSFET apart from FinFETs [5],[6] such as TFET[7], JLTFT[8] along with CNTFETs. Among all they will fail to compete with the CNTFET due to its advantages. As per the recommendation and credits by industry experts as well as researchers, CNTFET will be choice of next generation VLSI chips due to its small dimension and high performance [9],[10]. It has been reported that CNTFET based circuit are more efficient and 3 times faster than silicon based circuit at same power [11].

International Technology Roadmap for Semiconductors (ITRS) updates 2013 speaks that it is the future of transistors [12]. This paper is organized as follows; Section 2 presents FinFETs based device and their Issues and section 3 gives details about CNTFET technology and related issues. Sect 4 discusses the techniques for performance enhancement and various applications of CNTFETs are presented in section 5. The Section 6 covers the future scope with conclusion in last section.

2. FinFETs Device and their Issues:

In FinFETs both source and drain are connected with thin fin which forms the channel and the gate copes all around the channel to control current flow precisely; hence transistor entered into 3D form from the planar form [13]. Since more than one gate can be used to control the channel which in turn re-
which greatly reduces the scattering probability. It has the ability to minimize sub-threshold slope and hence SCE's. Different types of CNTFET’s are proposed since the invention of CNT’s; such as MOSFET like CNTFET, Schottky barrier type CNTFET, surrounding gate CNTFET, suspended CNTFET, vertical CNTFET, etc. MOSFET like CNTFET has the advantages of CMOS process compatibility, less variation to changing gate length, high ON current, etc. When laying the nano-tube down upon the source and drain electrode possess’ weak wander wall force for contact hence, the electrode were laid down on the top. In addition to carbon various other materials like Au, Ti, Co were used to improve the metal/ nano-tube contact during annealing process, it is still in the research phase because of its reliability issues [11]. Another suggested design is -Surrounded gate CNTFET offering the advantage of better controllability over the channel. The challenges for its realization needs to address the issues such as controlling band gap energy, gate dielectric deposition, low resistance contact formation, placing of nano-tubes, etc. The structure of CNTFETs with Drain, Source, Gate and CNTs is shown in Fig-2.

Since half a decade, major advancements have been made in the fabrication of CNTFET’s such as fabrication of carbon nano-tube computer with 178 transistors [9]. The standard parameters of the same are given in the Table-1 below.

Table-1 IRTS 2013 Standard Parameters for 22nm & 14nm Mode Technology

<table>
<thead>
<tr>
<th>Device parameter Taken for simulation</th>
<th>Technology Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>22nm</td>
</tr>
<tr>
<td>Channel Thickness (Lg) (nm)</td>
<td>22[20-25]</td>
</tr>
<tr>
<td>Oxide Thickness (Tox) (nm)</td>
<td>1</td>
</tr>
<tr>
<td>Fin Thickness (Tfin) (nm)</td>
<td>10[10-12]</td>
</tr>
<tr>
<td>Fin Height (Hfin) (nm)</td>
<td>40[30-50]</td>
</tr>
<tr>
<td>Source drain Doping concentration</td>
<td>10(^{10})</td>
</tr>
<tr>
<td>Channel doping concentration</td>
<td>10(^{20})</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>0.95</td>
</tr>
</tbody>
</table>

3. CNTFETs Devices and Their Issues.

The first carbon nano-tube field effect transistor was reported in 1998. These were simple devices fabricated by depositing single wall CNTs the electrode serve as source and drain and connected via nano-tube channels and the doped Si substrate served as the Gate. CNTFETs are promising and emerging nano-scale device for implementing very dense, low power and highly efficient circuits. CNTFETs uses semi-conducting material carbon in the form of carbon nano-tube as the channel [16]. The technology permits to have both n-channel and P-channel devices from nano-tubes. In earlier developed CNTFETs were P-type with hole is the major carrier and carried the nomenclature Hole conductor CNTFETs. Unlike FinFET’s, CNTFET’s are ballistic devices which uses carbon instead of silicon with high mobility Carbon nano-tube (CNT) as channel. Ballistic regime is because of owing one dimension...
Our research work primarily focused on enhancing the performance of the FinFETs, using different techniques. We have completed the simulation in techniques suggested by ITRS update 2013. These techniques are described below:

**DIFFERENT MODEL FOR CHANNEL**

Silicon (Si) has less carrier mobility as compared to that of Germanium (Ge), Indium Gallium Arsenide (InGaAs). As we know that the current in the device and carrier mobility are directly proportional to each other hence, it provides better performance. Ge is better option for channel but still have some issue in manufacturing. Hence, SiGe good candidate as channel.

**HIGH K- MATERIAL AS INSULATOR**

The concept of using high K dielectric material is already implemented in CMOS process. So the same concept of using high K- dielectric material is used here which enhance the performance of FinFETs [11].

**IMPLEMENTATION OF GATE ALL AROUND STRUCTURE**

Tri gate FinFETs are used to make ICs in many of the industry but when scaling them below 14nm their performance degrades because of increase in SCEs. Therefore ITRS 2013 update depicts that Implementation of gate all around is a solution of that using Si02 and Hf02 as gate dielectric.

**4. RELATED WORK**

As a device is scaled to their nano-size, it is quite difficult to model the device due to Quantum mechanics effect. Classical approach such as drift diffusion methods fail here. According to ITRS 13 update it is very difficult to model a device using Quantum Mechanical Approach using parameters at 14 nm technology or beyond. Firstly the simulation will be carried out for 22-nm node and then the same simulation process is again repeated for 14-nm node. Figure 3 shows the V-I characteristics of gate all around for both technology nodes. It was observed that FinFETs will give more OFF current in 14-nm node without any additional performance enhancement technique. The increased OFF current of FinFETs in 14-nm can be easily inferred from the graph. ON current (ION), OFF current (IOFF) and ION/IOFF ratio of the FinFETs in all simulations are listed in Si and SiGe as the channel.

Table-2 : Comparison of FinFETs and CNTFETs with different Dielectric materials.

<table>
<thead>
<tr>
<th>14nm Mode Technology</th>
<th>I+I/OFF ratio FinFETs</th>
<th>I+I/OFF ratio CNTFETs</th>
</tr>
</thead>
<tbody>
<tr>
<td>With low K dielectric material (Si02)</td>
<td>1.00E+03</td>
<td>5.25E+04</td>
</tr>
<tr>
<td>With high K dielectric material (Hf02)</td>
<td>4.40E+05</td>
<td>2.28E+06</td>
</tr>
</tbody>
</table>

**Fig. 3** V-I characteristics of FinFETs for 22-nm and 14-nm node [13]

V-I characteristics obtained from CNTFET simulation described in earlier section are shown in Fig. 4 for both 22-nm and 14-nm node. It is clearly indicated in the figure that CNTFET shows less variation in the performance as result of scaling. In this case use of High-k material (HfO2) dielectric will increase the ION/IOFF ratio. Finally results of FinFETs and CNTFETs simulation with different gate dielectrics are tabulated in the Table 2. It is clear from the table that CNTFETs shows better performance in comparison to that of FinFETs.

**Fig. 4:** V-I characteristics of CNTFETs in 22-nm and 14-nm [13]
6. Application of CNTFETs

As per literature survey, there are extensive applications of CNTFETs in varied fields. CNTFETs can be used as emerging candidates in numerous applications where MOSFETs are currently used. Hence, Carbon is considered to surpass silicon in Integrated Circuits (ICs). CNTFETs device depict the similar intrinsic properties that of Si-based MOSFET nano-tube (CNTs) are recently considered an emerging block for future nano-electronics industry. Some of possible application is listed below.

6.1. Communication Engineering

The linear relationship between applied voltage and drain current, CNTFETs finds its suitability for mobile communication system for incorporating several Complex Modulation Scheme [18].

6.2. RF and Microwave Applications:

RF and Microwave are used in wireless remote control security and scanning system to detect the image and location of buried object which compatible by wide variety of CNTFETs graphene FETs (GFETs) for the development of biosensor and Integrated on-chip security system with high sensitivity [4],[19],[20].

6.3. Bio-Medical Technology

Nowadays VLSI is widely used for implementing various biomedical applications to increase monitoring and diagnosis in healthcare. IoT based wearable devices and hearing aids, pacemakers are widely employed to improve the life span of human beings. These device Consist of various sensors based circuits which can be developed with Carbon nano-tube Field effect transistor (CNTFETs) instead of presently employed MOSFETs [21-25].

7. Future work.

It has been stated above that device modeling can be accurately done using quantum simulation; hence simulating the FinFETs and CNTFETs with quantum transport approach will lead to better and accurate results. Further, FinFETs variability analysis can also be done to understand the design issues in detail. Further, simulation for node less than 14-nm can also be performed for more research on FinFETs and CNTFET. Novel design methodologies with novel circuit are need of the hour to enhance the speed, reduce power consumption delay and area of CNTFETs with their fault tolerance detection at architectural level of design.


[22] CNTFET for biomedical sensing application. IEEE international conference on advances in engineering & technology research (ICAETR – 2014), August 01-02, Dr. Virendra Swarup Group of Institutions, Unnao, India; 1-4; 2014.

