AN FPGA IMPLEMENTATION BELIEF PROPAGATION DECODING ALGORITHM

M. M. Jadhav¹, Chetna N. Kharkar², Dr. A. M. Sapkal³

Abstract — Low Density Parity Check (LDPC) codes are one of the best error correcting codes that enable the future generations of wireless devices. In this paper we have presented an FPGA based self error checking & correction system with higher capability. We implemented the error correction algorithms such as belief propagation & bit flip algorithm. The number of error corrected is simulated using Xilinx High level Synthesis tool & Modelsim simulator. A complete self checking system is implemented on Xilinx Spartan 3E FPGA & synthesis is done using ISE13.2. The decoded codeword of the decoder is displayed on PC HyperTerminal using serial Rs232 interface. The system is capable of correcting large & different size of codeword. Self error detection & correction capability of the system is compared & verified in presence of noise.

Index Terms — LDPC codes, LDPC decoder, FPGA Implementation, bit flip decoding, Belief Propagation, log domain, soft decoding, hard decoding

1. INTRODUCTION

Low-density parity-check (LDPC) codes are forward error-correction codes [1], first proposed in the 1962 PhD thesis of Gallager at MIT[2]. The computational effort in implementing coder & encoder are more for these codes.LDPC codes is then rediscovered by Mackay and Neal [3]. These codes are decoded iteratively by Belief propagation decoding on their associated factor graph [4]. In the mean time the field of forward error correction was dominated by highly structured algebraic block and convolution codes.

Optimization results for various channels, such as the Additive White Gaussian Noise (AWGN) channel and the Binary Symmetric Channel (BSC) have produced specific degree distributions such that the corresponding codes come very close to capacity [5]. In fact, the state of art in the coding field is currently achieved by LDPC codes, which was accomplished by Chung et al. [6]. It was soon recognized that these block codes were in fact a rediscovery of the LDPC codes developed years earlier by Gallager. New generalizations of Gallager’s LDPC codes by a number of researchers produced new irregular LDPC codes. These codes easily outperform the best turbo codes, as well as offering certain practical advantages and cleaner setup for theoretical results. Today, design techniques for LDPC codes exist which enable the construction of codes which approach the Shannon’s capacity to within hundredths of a decibel. Low density parity check (LDPC) codes have been extensively adopted in next-generation forward error correction applications. They achieve very good performance using the iterative decoding approach of the belief-propagation (BP) [7].

1 M. M. Jadhav is presently perusing PHD from Government college of Engineering, Pune in the field of communication. He has guided graduates & more than ten Post graduates students, His area of Interest is communication system. Email- makj123@yahoo.com

2 Chetna N. Kharkar is currently Working as a Sr. Design Engineer at Qualitat systems, Pune (India). She has a 6+ years of experience in Embedded domain. Pursuing Master of Engineering from Sinhgad college of Engineering, Pune, India. Email- chetnakharkar@gmail.com

3 Dr. A. M. Sapkal is HOD of E&TC Department at government college of Engineering, Pune. He has 23 years of experience in teaching, 3 years Industrial & 14 years of Research experience. He has guided More than 100 post graduates students. Email - hod.extc@coep.ac.in
use for any length of code word (or) data word and also for any rate of code word. So the usage of this code leads to high performance. The above decoding algorithms can recover the original codeword in the presence of large amounts of noise. Decoding algorithms such as belief propagation & Bit flip algorithm are simulated, error detection and correction capability of both algorithms compared & verified.

2. DESIGN OF DECODING ALGORITHM FOR ERROR CHECKING

The decoding algorithm can be stated in three steps:

i. Initialization
The decoding algorithm is fed by the log-likelihood ratio as represented in equation (2).

\[ r_{0}[i] = \log \left( \frac{P(c_i = 0 \mid y_i)}{P(c_i = 1 \mid y_i)} \right) \quad \text{(1)} \]

ii. Syndrome Check
The code word simply multiplied by the transpose of \( H \). If the result is all zero vectors then the code word is valid.

\[ H^T \star Z = 0 \quad \text{(2)} \]

iii. The Iterative Decoding
The algorithms used to decode LDPC codes are the belief propagation algorithm or the sum-product algorithm, bit flipping algorithm.

2.1 Belief propagation decoding algorithm

Decoding algorithm consists of three steps computed iteratively
1. The data node process (data update) computes \( M_{j,i} \) messages from \( E_{j,i} \) messages and log-likelihood ratios. For each data node, \( i \) being the degree of the node and \( r_i \) is the log-likelihood ratio entering this node:

\[ M_{j,i} = \sum_{j' \in A_i, j' \neq j} E_{j',i} + r_i \]

2. The check node process (check update) computes \( E_{j,i} \) messages. For each check node \( j \) being the degree of the node:

\[ E_{j,i} = (\prod_{\alpha {j'}} g(\beta {j'}) ) \]

where \( \alpha_{j'} = \text{sign}(M_{j'}) \) and \( \beta_{j'} = |M_{j'}|' \)

3. Two math functions are used in step 2 for transposing the initial needed convolution in the log-Fourier domain. These functions are defined as,

\[ f(x) = \log \left[ \tanh \left( \frac{|x|}{2} \right) \right] \]

\[ g(x) = 2 \cdot \tanh^{-1} \left( \exp(x) \right) \]

4. The hard decision process that computes the estimated value of each symbol of the code. For each data node:

\[ L_{i} = r_{i} + \sum_{j} E_{j,i} \]

2.2 Bit flip Decoding Algorithm

Algorithm: Bit flipping Decoding

Procedure Decode(y)

\[ \text{for } i = 1 : n \text{ do} \]

\[ M_{i} = y_{i} \]

\[ \text{end for} \]

\[ \text{repeat} \]

\[ \text{for } j = 1 : m \text{ do} \]

\[ \text{for } i = 1 : n \text{ do} \]

\[ E_{j,i} = \sum_{i' \in B_j, i' \neq i} (M_{i'} \mod 2) \]

\[ \text{end for} \]

\[ \text{end for} \]

\[ \text{for } i = 1 : n \text{ do} \]

\[ \text{if the messages } E_{j,i} \text{ disagree with } y_{i} \text{ then} \]

\[ M_{i} = (r_{i} + 1 \mod 2) \]

\[ \text{end if} \]

\[ \text{end for} \]

\[ \text{for } j = 1 : m \text{ do} \]

\[ L_{j} = \sum_{i \in B_j} (M_{i} \mod 2) \]

\[ \text{end for} \]

\[ \text{if all } L_{j} = 0 \text{ or } I = I_{\text{max}} \text{ then Finished} \]

\[ I = I + 1 \]

\[ \text{end if} \]

\[ \text{until Finished} \]

\[ \text{end procedure} \]

3. EXPERIMENTAL SETUP

We have Implemented Bit flip decoder & belief propagation decoder algorithm on Xilinx Spartan 3E starter Board. The output of the decoder is shown on PC (computer) HyperTerminal. Figure 1 shows the experimental setup & figure 2 shows...
Decoder codeword on PC HyperTerminal the hardware for hardware implementation of the decoder algorithm. The results of bit flip decoder & belief propagation algorithm is compared in terms of number of error recovered. The results show that belief propagation algorithm has a better error correction capability than the bit flip decoder.

Figure 1: Experimental setup

Figure 2: Decoded codeword on serial Port HyperTerminal

4. FPGA IMPLEMENTATION OF ERROR CHECKING DECODER

FPGA implementation of the decoder is done for large H matrix & results are simulated using High level Simulator. The design is synthesized and implemented using Xilinx ISE 13.2. The Xilinx High level synthesis Tool converts the High level c language code into HDL. The synthesis is done using the High level synthesis & Xilinx ISE 13.2, built in synthesis tool. Table 1, shows synthesis report which gives information of the Slice flip flops, LUTs usage, device utilization constraint, timing summary. Figure 3, shows the simulation results which show the working of the decoder. The reset & clock activates the other signals, when reset is ‘1’, the decoder is in Idle condition, when reset ‘0’, decoder operation starts on the clock tick event. Figure 1 shows the H-matrix used for decoding & the output Z required decoded codeword.

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Figure 1: Experimental setup

Figure 2: Decoded codeword on serial Port HyperTerminal

Table 1: Xilinx device utilization summary

5. FPGA IMPLEMENTATION RESULT

The decoding performance of belief propagation and bit flip algorithms in recovering original codeword, shown in the table Table 2.

<table>
<thead>
<tr>
<th>MSG Bits</th>
<th>H Matrix</th>
<th>Codeword length</th>
<th>No. of errors recovered by BPD</th>
<th>No. of errors recovered by BFD</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>64X128</td>
<td>128</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>128</td>
<td>128X256</td>
<td>256</td>
<td>9</td>
<td>8</td>
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<tr>
<td>256</td>
<td>256X512</td>
<td>512</td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td>512</td>
<td>512X1024</td>
<td>1024</td>
<td>18</td>
<td>16</td>
</tr>
<tr>
<td>2048</td>
<td>2048X4096</td>
<td>4096</td>
<td>46</td>
<td>34</td>
</tr>
</tbody>
</table>

Table 2: Comparison of Number of errors recovered by Belief propagation & Bit flip Algorithm
6. CONCLUSION

The decoder was designed using High level Language & synthesized using Xilinx High level synthesis tool to Implemented on Hardware. The simulation results shows how the clock & reset signal controls the decoder operation. The implementation of self checking system on FPGA for belief propagation algorithm has resulted in correction & detection of errors on large size codeword. Belief propagation & bit flip algorithm results are compared & verified using Simulation & implementation. From the performance parameter it is concluded that Belief propagation decoding algorithm improves the performance of system in terms of error correction rate. Error recovery rate of belief propagation algorithm is better than bit flip decoding algorithm. The detailed decoder design and architecture are presented and the results are explained.

REFERENCES


