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FACULTY OF POWER AND ELECTRICAL ENGINEERING

Computerised Control of Electrical Technologies

KUSUMA PRIYA KROVI

(Student ID: 181AEM060)

"Research and Development of Step-Down Converter for Energy Storage Applications"

Master Thesis

Scientific Advisor:

Dr. Sc. Ing. Janis Zakis

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The Author of the Thesis:

Kusuma Priya, Krovi….....

(signature, date)

Scientific adviser

Dr. Sc. Ing. Janis Zakis….....

(signature, date)

The Master Thesis is recommended for defending:

Director of the Institute: **Dr.habil.sc.ing. L. Ribickis** ….....

(signature, date)

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State examination board chairman ….....

Members of the Board ….....

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Secretary of the Board ….....

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ANNOTATION

The main purpose of the thesis is to develop a control system for Step-Down DC-DC converter for an energy storage system where output voltage should be constant with variable input voltage and load. Converter PCB is designed and tested in buck mode where 341.1W power is achieved by using the SiC MOSFETs and Non-isolated DC/DC converter. The Software results and necessary data is provided. The analysis of MOSFET properties, Control Systems and research on EMI reduction is done.

Content: 89 Pages, 66 Figures, 7 Tables, 61 References

ANOTĀCIJA

Darba galvenais mērķis ir izstrādāt vadības sistēmu līdzstrāvas pazeminošajam pārveidotājam enerģijas uzkrāšanas sistēmai, kur izejas spriegumas ir nemainīgs, bet ieejas spriegums un slodze mainīga. Darbā ir veikta līdzstrāvas pārveidotāja spiestās plates projektēšana un pārbaude sprieguma pazeminošā režīmā ar jaudu 341 W.

Tāpat arī darbā iekļauts MOSFET tranzistoru apskats, vadības sistēmu izpēte, elektromagnētiskās savietojamības risinājumi un datorsimulāciju rezultāti.

Saturs: 89 lapas, 66 attēli, 7 tabulas, 61 atsauces

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ABBREVIATIONS

SCR	Silicon Controlled Thyristor
MCT	MOS Controlled Thyristor
PIV	Peak Inverse Voltage
BJT	Bipolar Junction Transistor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
CE	Common Emitter
CB	Common Base
CC	Common Collector
GTO	Gate Turn Off Thyristor
SITH/SIT	Static Induction Thyristor
ODF	Over Drive Factor
DMOS	Diffused Metal-Oxide Semiconductor
COMFET	Conductively Modulated Field Effect Transistor
GEM	Gate Modulated FET
MOSIGT	Metal-Oxide Semiconductor Insulated Gate Transistor
IGT	Insulated Gate Transistor
WBG	Wide Band Gap
UPS	Unregulated Power Supply/ Uninterrupted Power Supplies
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
PWM	Pulse Width Modulation
EMI	Electro-Magnetic Interference
HEV	Hybrid Electric Vehicle
HV	High Voltage
LV	Low Voltage
PCS	Power Conversion System
BESS	Battery Energy Storage System
DR	Distributed Resources
EPS	Electric Power Systems
PHEV	Plug-in Hybrid Electric Vehicle
PCB	Printed Circuit Board

EMC	Electro-Magnetic Compatibility
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZCT	Zero Current Transition
ZVT	Zero Voltage Transition
FFT	Fast Fourier Transform

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INTRODUCTION

Now a days, renewable energy resources mostly used for the generation of electric power which are environmentally friendly. Like solar, wind are the sources where there will be the fluctuations and sometimes cannot provide the required energy during peak demand. Due to this reason, need of energy storage systems (ESS) came into existence where there are different topologies like battery, hybrid and fuel energy systems for the storage. Whenever, there is the use of energy storage systems, there will be DC/DC converters. Similarly, balanced power should meet at grid where there is the need of DC/DC converters in order to step-up or step down the grid voltage to be balanced. So mostly used DC/DC converter is bi-directional converter which can be used in both buck and boost modes.

While using the DC/DC converters in energy storage systems, the converter should operate efficiently. So, in order to operate in that way, synchronous buck converters should be used which is replaced with the MOSFET instead of diode from basic buck converter circuit for low cost and less losses but if this synchronous DC/DC converter can also operate in both buck and boost modes by giving the appropriate gate signal and the high side MOSFET will conduct during buck mode and low side MOSFET will conduct during boost mode where this operation is almost similar to the bidirectional DC/DC converter with almost same circuit configuration. In order to control the gate of the MOSFET, closed loop is needed. In order to get the accurate desired output using current control mode method to give the pulse to the gate help to reduce the oscillations at the output.

Usually, there are different types of switches to use in converter but for medium power applications, MOSFETs are used widely which are voltage controlled. Also, there are different types of materials like Si, GaN and SiC. Until the existence of GaN, SiC there is the use of Si but due to less losses and high temperature operating reliability the wide bandgap semiconductor materials (GaN, SiC) are widely using now. Mostly SiC based non-isolated (where it has the DC path between its input and output) DC-DC converter are used because of its high frequency range, high temperature withstanding capability, low switching and conduction losses by having faster turn on. Actually, there are parasitic elements which give the electromagnetic interference(EMI) which leads to overall power reduction if the synchronous DC/DC converter is not designed accurately, thereby instead of using hard switching, soft switching or chaos control methods can be used for EMI reduction for desired results.

Thesis Objectives:

- Learning of basic principle of MOSFET's and its pros compared to other switches like BJT's, Diodes etc.
- To identify the different types of control systems to the step-down dc-dc converter providing simulation results for synchronous buck converter compared to basic buck converter using MATLAB software.
- To know the various topologies for energy storage systems.
- Research analysis to reduce the electromagnetic interference in step-down converter.
- Hardware implementation of DC/DC converter in buck mode by using driver mechanism method to drive the gate.

THESIS STRUCTURE

The structure of this thesis contains a general introduction, four chapters, a conclusion, and future work and a list of references. Every chapter have its basic introduction for further understanding. The general conclusion is given at the end of the thesis for the whole work.

Chapter 1: Fundamentals of Power Semiconductor Diodes and Transistors(switches)

This chapter deals with the basic introduction about the switches and its evolution, basic operation with pros and cons.

Chapter 2: Control of Step-down converter

This chapters explains about the different control strategies for a converter to maintain constant output by using MATLAB software for a synchronous buck converter which plays importance in energy storage applications by comparing to basic buck converter with simulation results.

Chapter 3: Energy Storage applications for step-down converter

This chapter deals with, how the topologies in the real time applications with the use of converter in buck-mode and introducing synchronous buck converter for those applications.

Chapter 4: EMI Reduction and PCB Design

This chapter research about how to reduce the EMI and what methods must use.

Chapter 5: Hardware Development of Converter in Buck Mode

In this, hardware development of converter in Buck-Mode with practical results.

conclusions and list of references are given.

1. Fundamentals of Power Semiconductor Diodes and Transistors

Silicon controlled rectifier (SCR) was first introduced in the year 1957. After that, several power semiconductor devices are introduced with different ratings. The classification of semiconductors is done based on turn on, turn off characteristics and gate signal [1] [2].

Diodes: These are uncontrolled switching devices where on and off operations are controlled by the power supply [1].

Thyristors: These have controlled gate signal during turn-n. Due to regenerative action, they remain latched-in on-state when thyristors are turned-on [1].

Controlled Switches: With the help of control signals the devices can be turned on and off. BJT, MOSFET, GTO, SITH, IGBT, SIT & MCT are the devices are the devices which behave as controllable switches [1].

Pulse gate signals are required are required for SCR, GTO, SITH & MCT to turn on them. Once the device is turned on gate pulse is removed and continuous signal is required for BJT, MOSFET, IGBT, & SIT to keep them in turn state [1].

Triac & RCT comes under bidirectional current capability whereas, unidirectional current devices are other remaining devices (Diode, SCR, GTO, BJT, MOSFET, IGBT, SIT, SITH, MCT) [1].

1.1 Types of Power Electronic Converters

A power electronic converter consists of one or more power electronic converters. It is made up of some power semiconductor devices and by using integrated circuits we controlled the devices. The switching characteristics permit a power electronic converter to shape the power from one form to other form where there is change from input power to output power. The function of power conversion is performed by static power converters very efficiently. Broadly speaking, the power electronic converters are of six types as below [1].

Diode rectifiers: It converts ac input voltage into a fixed dc voltage. The input voltage may be either single phase or three phase. Applications like electric traction, battery charging, electro plating, electro chemical processing, power supplies, welding and uninterruptable power supplies (UPS) systems where there is need of rectifiers [1].

AC to DC Converters (phase-controlled rectifiers): These devices convert constant ac voltage to variable dc output voltage. For commutation, these rectifiers use line voltage, as such the devices are also known as line-commutated or naturally commutated ac to dc

converters. Phase controlled converters may be fed from single phase or three phase source and are used in dc drives, metallurgical and chemical industries, excitation systems for synchronous machines etc. [1].

DC to DC Converters (DC Choppers): A dc chopper converts fixed dc input voltage to a variable dc output voltage and to turn off the thyristors we require forced or load commutation. The thyristors are replaced by transistors for low power circuits. Depending upon the type of commutation and on the direction of power flow the choppers circuits are classified and are widely used in dc drives, subway cars, trolley trucks and battery-driven vehicles etc. [1].

DC To AC Converters: The converter with fixed dc voltage to a variable ac voltage and output may be a with variable voltage and variable frequency mostly in inverters. To turn of the thyristors these converters use line, load or forced commutation. These inverters are wide employed in induction-motors and synchronous-motor drives, induction heating, UPS, HVDC transmission etc. Nowadays in high power application standard thyristors are being replaced by GTOs and by power transistors in low-power application [1].

AC To AC converters: These convert fastened ac input voltage into a variable ac output voltage. These are of two types:

Ac voltage controllers: These device circuits convert fastened ac voltage directly to a variable ac voltage at an equivalent frequency. These voltage regulators use a traic or two thyristors in opposed parallel. Each the devices area unit turned off with the assistance of line commutation. We can manage the output voltage by variable the firing angle delay. These devices area unit wide employed in lighting management, speed management of fans, pump etc. [1].

Cyclo converters: A cyclo converter may be a device that converts ac power at one frequency to output power at completely different frequency through one stage conversion. In these converters line commutation is additional common, though forced and cargo converters cyclo converters are also used. These are wide used for slow- speed large ac drives like rotary kiln etc. [1].

Static switches: The power semi-converter devices will operate as static switches or contactors. These switches possess many advantages over mechanical and electromechanical circuit breakers. The static switches are referred to as ac static switches or dc static switches depending upon the input supply [1]

1.2 Power Semi Converters Elements

A power diode and thyristor devices are most vital important in numerous power physical science topologies. Power semiconductor diodes are like lower power p-n junction diodes, referred to as signal diodes. Similarly, power transistors are identical with npn or pnp signal transistor. The main objective of this chapter is to describe power diodes, power transistors and MOS controlled thyristors (MCT) [1] [3].

1.2.1 Power Diode Characteristics:

Power diodes are made up of silicon pn junction formed by allowing, diffusing or epitaxial growth. Power diode may be a two-layer, two terminal, p-n semiconductor devise. There are two terminals one is anode, and another is cathode. The two vital characteristics of power diodes are described below [1].

1.2.1.1 Diode V-I Characteristics:

When anode is positive with respective to the cathode, the diode is in forward biased condition. Initially diode current is zero, with increase of the source voltage Vs from zero value i.e., Vs =0 to cut in voltage. The cut in voltage is additionally referred to as threshold voltage or turn on voltage, the forward diode current is very small. The diode is said to conduct when the diode current rises speedily beyond cut-in voltage. The cut in voltage is 0.7 for silicon diode where will be the forward voltage drop of 0.8 to 1V when diode starts conducting [1].

The diode is said to be reverse biased when anode is negative with respect to cathode. A small reverse current, known as leakage current, flows in the of microamperes or milli-amperes flows in the reverse biased condition of the diode. The leakage current increases slowly with respect to reverse voltage until breakdown or avalanche breakdown is reached. The diode is turned on in the reversed direction at this breakdown voltage. If the current is not limited by series resistance in the reversed direction, the current will we too high to destroy the diode. By operating the diode with below specific peak repetitive reverse voltage V_{RRM} the reverse avalanche breakdown of the diode is avoided. Fig 1.3 illustrates the diode characteristics where V_{RRM} and cut-in voltage is shown [1].

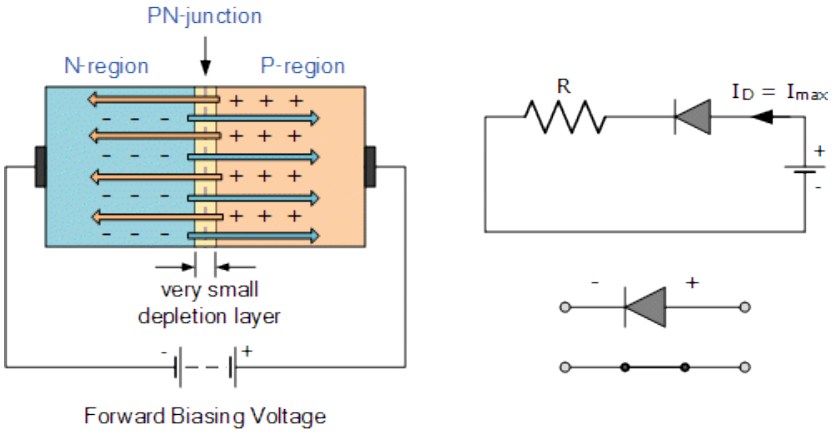


Figure 1. 1. Diode with Forward Bias [4].

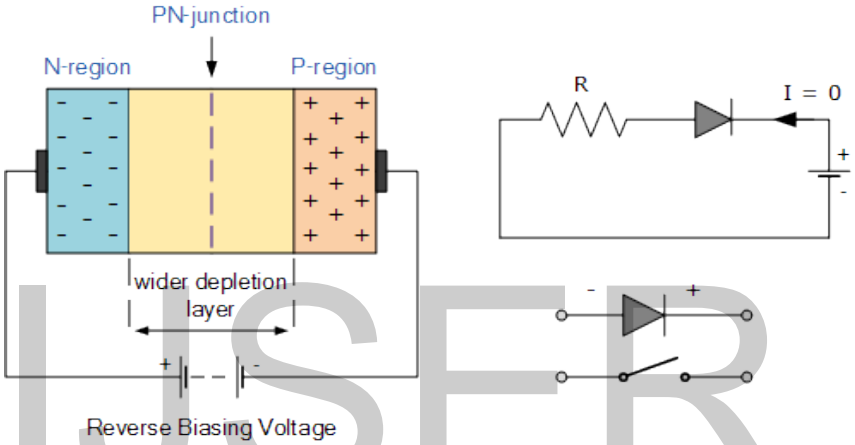


Figure 1. 2. Diode with Reverse Bias [4].

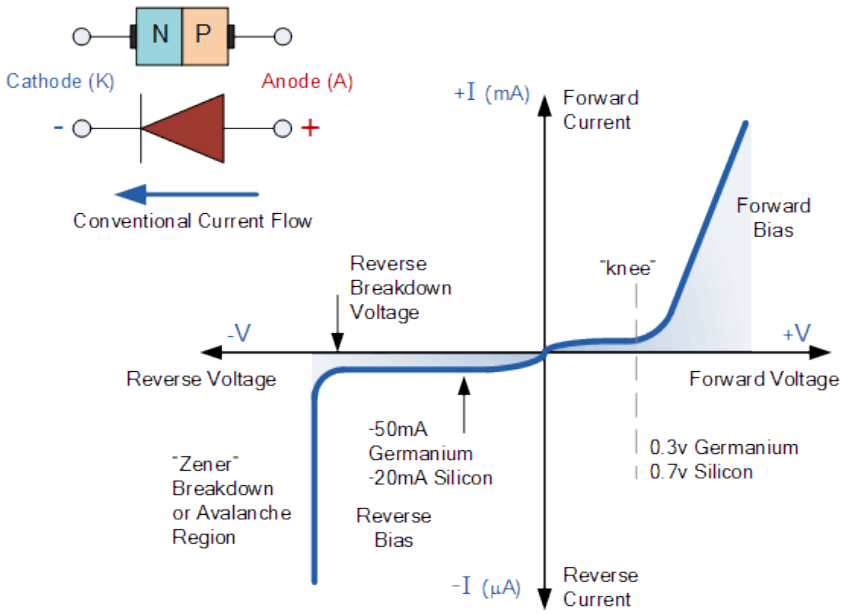


Figure 1. 3. Diode V-I characteristics [5].

The value of peak inverse voltage (PIV) of a diode is also indicated by the diode manufacturers. These are the largest reverse voltage to which a diode may be subjected during

its working. PIV is same as V_{RRM} [1].

The power diodes are now available with reverse voltage ratings of 50V to 3000V or more and with and with forward current ratings of 1A to many thousand amperes [1].

1.2.1.2 Diode Reverse Recovery Characteristics:

The diode continues to conduct in the reverse direction, after the forward current decays to zero because of the presence of stored charges in the two layers. Whenever the reverse recovery current decays to zero, the diode regains its blocking capability. The reverse current flows for a time called the reverse recovery time t_{rr}. The moment at which the forward diode current becomes zero and therefore the instant reverse recovery current decays 25% of its reverse peak value I_{RM} called as reverse time t_{rr} [1].

The reverse recovery time consists of two segments of time t_a and t_b, i.e., $t_{rr}=t_a+t_b$. where t_a is known to be the time between the zero crossing of forward current and peak reverse current I_{RM} and t_b is time that is measured from the instant of I_{RM} to the instant that is reached to 0.25 I_{RM}. The charge stored within the depletion region is removed during the time t_a and during t_b charge from the two layers is removed. The ratio of those two-time factors t_b/t_a is known as softness factor or S-factor. The stored charge or reverse recovery charge which is shown in figure 1.4(a) with representation of shaded area, where there should be removal of Q_R when diode is at reverse recovery time t_{rr}. The diode has large oscillatory over voltages when S-factor is small. If S-factor is one then it is termed as soft recovery diode or less than one is called snappy recovery diode or fast recovery in diode [1].

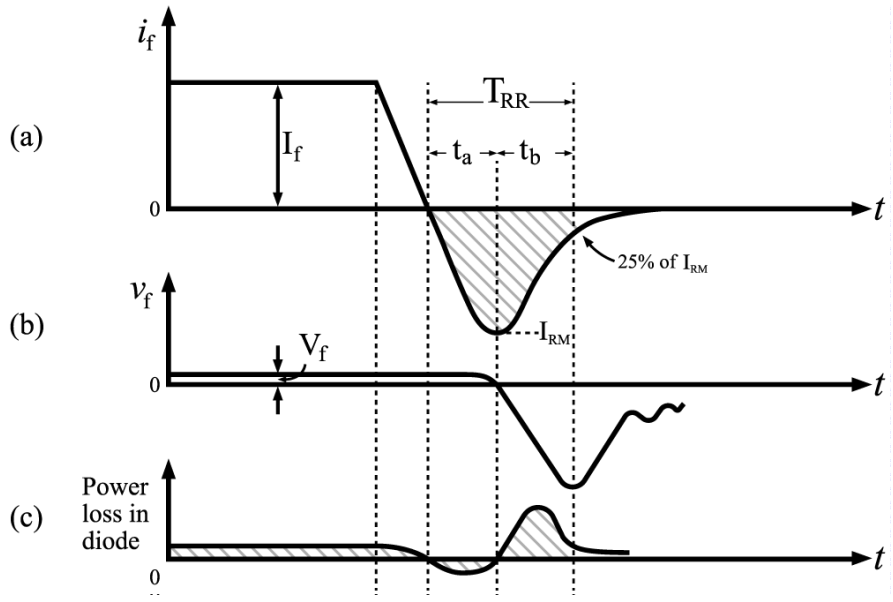


Figure 1. 4. Reverse recovery characteristics (a) variation of forward current i_f (b) forward voltage drop(v_f) and (c) power loss in a diode [1].

In figure 1.4(b), shown the waveform of forward voltage drop v_f across the diode. The product of v_f and i_f gives the power loss in a diode. The variation is shown in the figure 1.4(c). The total power loss is taken from the average value as $V_f i_f$ in a diode. Figure 1.4(c) reveals that major power loss in a diode occurs during the period t_b [1].

It is noticed from the figure 1.4(a) that peak inverse current I_{RM} can be expressed as

$$I_{RM} = ta * di/dt \quad (1.2.1)$$

Where di/dt = rate of change of reverse current.

The reverse recovery characteristics of figure 1.4(a) can be taken to be triangular. Under this assumption storage charge Q_R, from figure 1.4(a) is given by,

$$Q_{RM} = 1/2 * I_{RM} * t_{rr} \quad (1.2.2)$$

OR

$$I_{RM} = 2Q_r / t_{rr} \quad (1.2.3)$$

If $t_{rr} = t_a$, then from equation (1.2.1)

$$I_{RM} = t_{rr} * di/dt \quad (1.2.4)$$

From Equations (1.2.3) and (1.2.4), we get

$$T_{rr} * di/dt = 2\ Q_R/t_{rr} \quad (1.2.5)$$

$$T_{rr} = [2Q_R/ (di/dt)]^{1/2} \quad (1.2.6)$$

From Equation (1.2.1), with $t_a = t_{rr}$, we get

$$I_{RR} = t_{rr} * di/dt = [2Q_R/ (di/dt)]^{1/2}.di/dt$$

$$= [2Q_R (di/dt)]^{1/2} \quad (1.2.7)$$

It is seen from Equations (1.2.6) and (1.2.7) that reverse recovery time and peak inverse current are dependent on storage charge and rate of change of current *di/dt* where storage charge dependent on the forward diode current I_f. This shows that reverse recovery time and peak inverses current depend on forward field current [1].

1.3 Types of power diodes

The power diodes are classified into three types by the consideration of reverse recovery characteristics, [1]

1. General purpose diodes
2. Fast recovery diodes
3. Schottky diode

1. General purpose diodes:

These general-purpose diodes have high reverse recovery time. It will be within the range of 25µs. In this, current rating varies generally from 1A to several thousand amperes and the

voltage rating will be in between 50V to 5KV. Some of the applications of the general-purpose diodes are battery charging circuits, uninterruptible power Supplies (UPS) and electric traction etc. [1].

2. Fast recovery diodes:

As the name indicates, these diodes have very low reverse recovery time of about 5μs or less. They are mainly used in commutation circuits, choppers, switched mode power supplies, induction heating etc. The ratings of the diode are taken as, the current rating will be 1A to many thousand amperes and the voltage rating in the range from 50V to 3KV [1].

In this kind of diode,

For low voltage ratings (below 400V), the epitaxial process is employed for the diode fabrication.

For diodes having voltage rating above 400V, diffusion technique is employed for the fabrication of diodes [1].

3. Schottky Diodes:

In high frequency switching circuits like SMPS, the Schottky diodes are used (in those applications we cannot use the general-purpose diodes). In this type of diodes, instead of P-N junction metal to semiconductor junctions used. There will be very fast recovery time and low forward voltage drop in the Schottky diode. The flow of current only due to majority carriers. So, the time delay because to reverse recombination is avoided. The disadvantage with Schottky diode is that they have low voltage ratings around 100V and forward current ratings up-to 300A [1].

1.4 Power Transistors

Power diodes are uncontrolled devices because their turn-on turn-off characteristics are not under control. Power transistors, however, possess controlled characteristics. When a current signal is given to base then only turn on of transistors are possible. The transistor remains in the on-state until the control signal is present. The power transistor is turned off when the control signal is removed [1].

Power transistors are of three types,

- Bipolar junction transistors (BJTs)
- Metal-oxide-semiconductor field-effect transistors (MOSFETs)
- Insulated gate bipolar transistors (IGBTs)

These three types are described below.

- **Bipolar junction transistors:**

A bipolar transistor is a three-layer, two junctions NPN or PNP semiconductor unit. If P-type base is sandwiched which is thin and lightly doped between a heavily doped N-type emitter and N-type collector is known as NPN transistor , while doping with thin and lightly N-type base which is sandwiched between a heavily doped P-type emitter and collector is called as PNP transistor as shown in Figure 1.5 (a) and (b). The term bipolar denotes the current flow in the device is due to the movement of both electrons and holes. An emitter, base and collector are the terminal representation for BJT [1].

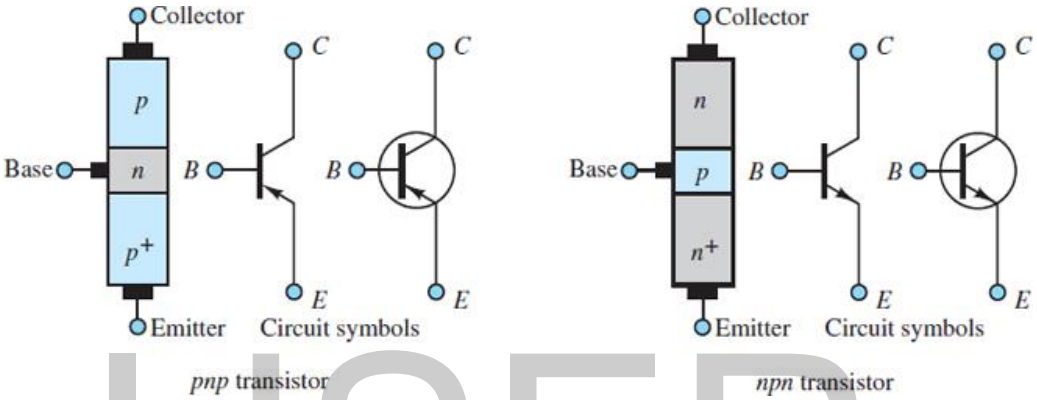


Figure 1. 5. Bipolar Junction Transistors (a) PNP type and (b) NPN type [6].

- **Steady state characteristics**

Depending on which of the three terminals is used as common terminal, there can be three possible configurations for the transistor:

- Common emitter (CE)
- Common base (CB)
- Common collector (CC)

Out of the three possible circuit configurations, common emitter arrangement is more common in switching applications. Therefore, NPN transistors will only be considered [1].

- **In-put characteristics**

The Emitter base junction of the common-emitter configuration can also be considered as a forward biased diode, the current-voltage characteristics is like that of diode. A graph between current I_B and base emitter voltage V_{BE} gives input characteristics as shown in Figure 1.6(b). When collector emitter voltage V_{CE2} is more than V_{CE1} base current decreases as shown in Figure 1.6(b) [1].

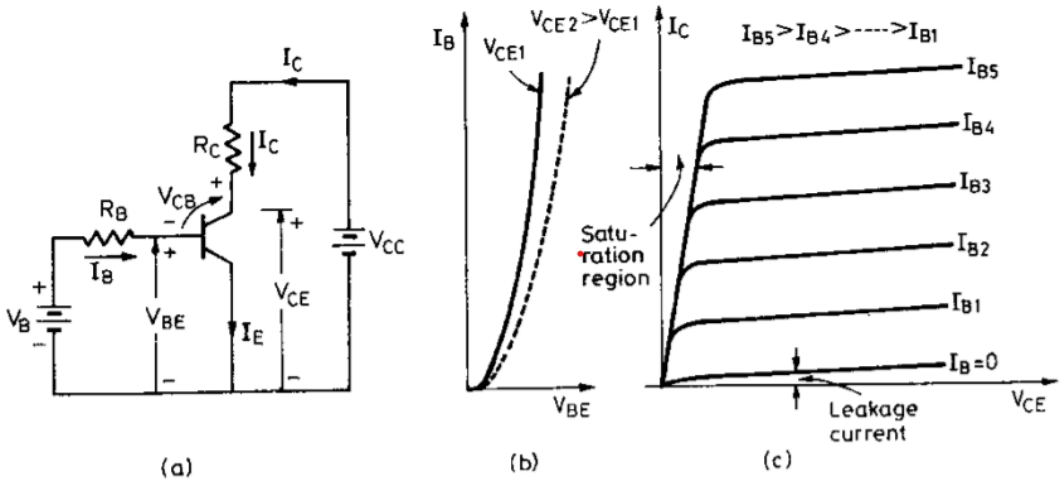


Figure 1. 6 (a) NPN transistor circuit characteristics, (b) input characteristics and (c) output characteristics. [1]

- **Output characteristics:**

A graph between collector current I_C and collector emitter voltage V_{CE} gives output characteristics of a transistor. At base current I_B=0 as V_{CE} increased a small leakage current flows as shown in Figure 1.6(c). As the base current increased from $I_B=0$, to I_{B1}, I_{B2} etc. The collector current also rises as shown in Figure 1.6(c) [1].

Figure 1.7(a) shows the output characteristic curves for I_B=0 and for $I_B\neq0$. The initial part of curve 2 (i.e. $I_B\neq0$) has low V_{CE} and this region called the saturation region. In curve-2 the flat part indicating almost constant I_C by increasing V_{CE} is the active region. The transistor acts like an amplifier, in this region the breakdown region is indicating by the vertically rising curve which must be avoided [1].

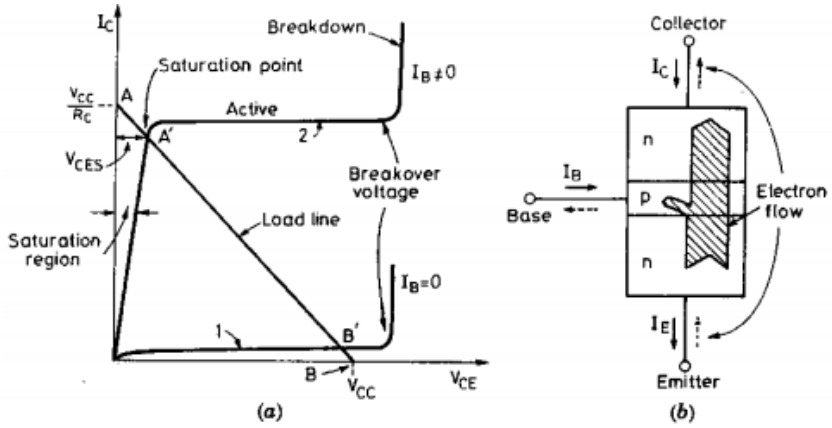


Figure 1. 7. a) output characteristics and load line for NPN transistors and (b) electron flow in

NPN transistor [1].

For load resistor R_C, Figure 1.6(a), the collector current I_C is given by

$$I_C = V_{CC}\text{-}V_{CE}/R_C \quad (1.4.1)$$

This is the equation of load line and it is shown by the line *AB* as shown in Figure 1.7(a). When the transistor is ON, V_{CE} is zero and collector current $I_C=V_{CC}/R_C$. The I_C is shown by point *A* on vertical axis. The V_{CC} appears across collector-emitter terminals when the transistor is off (or) in cut off region and there is no collector current. This value is indicated by point *B*. The line joining the points *A* and *B* called the load line [1].

- **Relation between α and β:**

Though the collector current I_C less than the emitter I_E. It is almost equal to I_E. The forward current gain is defined as the ratio of collector current to the emitter current and is indicated by α. i.e. [1]

$$\alpha = I_C/I_E \quad (1.4.2)$$

As $I_C < I_E$, value of α varies from 0.95 to 0.99.

In a transistor, the input current is the base current and the output current is the collector current. The ratio of collector current I_C to the base current I_B is known as the current gain β and is given by

$$\beta = I_C/I_B \quad (1.4.3)$$

Using KCL in Figure 1.6(a) gives

$$I_E = I_C + I_B \quad (1.4.4)$$

Remember that the emitter current is the largest of all the three currents, the collector current is almost equal to but less than emitter current. Base current has least value. Dividing both sides of Equation (2.8) by I_C we get

$$I_E/I_C = 1 + I_B/I_C \quad (1.4.5)$$

$$1/\alpha = 1+1/\beta \quad (1.4.6)$$

or

$$\beta = \alpha/1\text{-}\alpha \quad (1.4.7)$$

$$\alpha = \beta/\beta+1 \quad (1.4.8)$$

- **POWER MOSFETs:**

A power MOSFET is known as metal oxide semiconductor field effect transistor. In electronic circuits, it is a unipolar, voltage-controlled, high input impedance device which is an integral part. It is a three terminal device called drain, source and gate instead of collector, emitter and base for BJT. The circuit symbol is as shown in Figure 1.8(a). The arrow direction

represents the electron flow. Its operation depends upon the majority charge carriers. The base current (or) the control signal required for MOSFET is much less than that of BJT. In MOSFET the gate circuit impedance is extremely high of order of 10^9 Ω. The MOSFET gate is driven directly from microelectronic circuits because of the large impedance. Second break down of voltage occurs in BJT, whereas the MOSFET is free from this problem. The power MOSFETs are widely used in low power frequency converters [1].

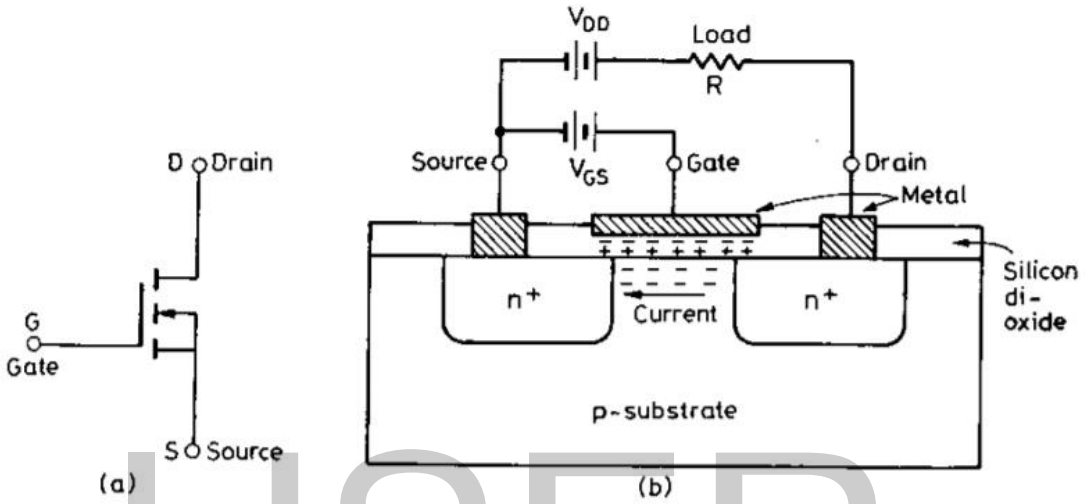


Figure 1. 8. N-channel enhancement power MOSFET (a) circuit symbol and (b) its basic structure [1].

There are 2 types of power MOSFETs,

- N-channel enhancement MOSFET and
- P-channel enhancement MOSFET

Out of these two because of higher mobility of electronics the N-channel enhancement MOSFET is more common [1].

A simplified structure of n-channel MOSFET of low power rating as shown in Figure 1.8(b). The N-channel region between source and drain forms the N-channel MOSFET. In this type of MOSFET, diffusion of two n^+ regions which are heavily doped on the P-substrate and the thin layer of silicon-di-oxide (SiO2) on the top of the substrate which works as insulation. In order to embed metallic source and drain terminals the insulating layer is engraved. From Figure 1.8(b), it is shown that the n^+ regions contact source and drain terminals. To form the gate terminal of MOSFET a layer of metal is also deposited on Sio_2 layer. [1] When gate circuit is open, then no current flows from drain to source and load because of one reverse-biased n^+-p junction. An electric field is established, when gate is made positive with respect to source as shown in Figure 1.8(b). Finally, in the p-substrate below Sio_2 layer induced negative charges are formed called as electrons. Hence form N-channel and current can flow

from drain to source shown by the arrow. If V_{GS} is more positive, n-channel becomes more and more current flows from drain to source. The current through the channel gets enhanced due to increase in gate voltage, hence the name enhancement MOSFET [1].

The main disadvantages of n-channel MOSFET is when n-channel is conducting a large ON-state resistance is present between drain and source where there will be high power dissipation in n-channel. This shows that MOSFET of Figure 1.8(b) is used only for low power MOSFET [1].

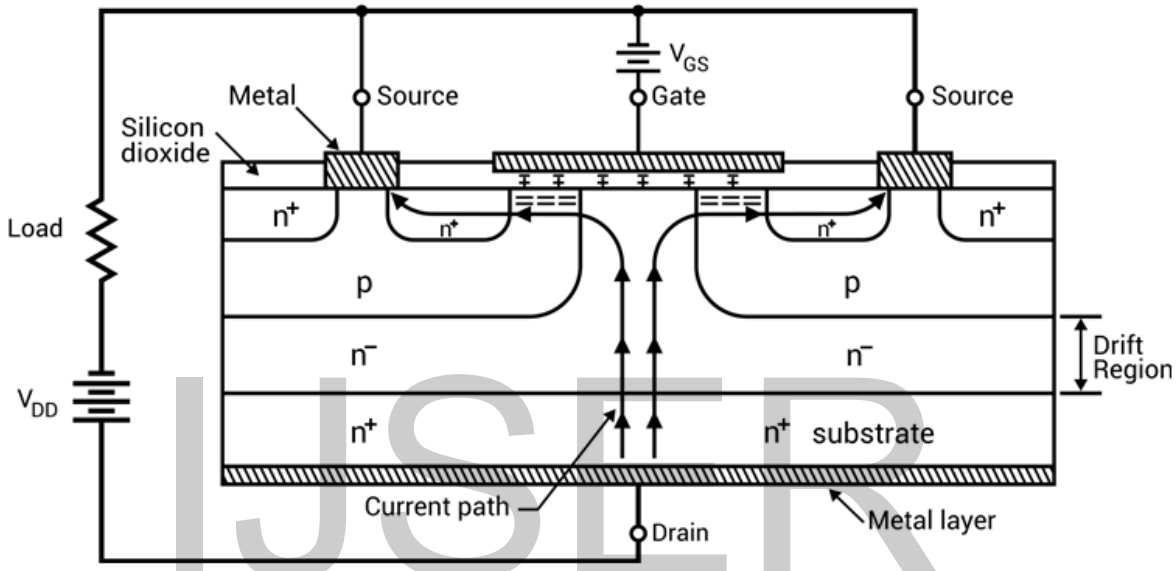


Figure 1. 9. basic structure of a n-channel DMOS power MOSFET [1].

The constructional details of high power MOSFET or illustrated in Figure 1.9. figure 1.9 shows a planer diffused metal oxide semiconductor (DMOS) structure for N-channel for power MOSFETs meanwhile there will be high resistivity n^- layer that is epitaxially grown on the n^+ substrate. Further, n^+ regions are diffused in p^- regions shown. As before, Sio_2 layer is added, which is then etched to fit metallic source and gate terminals. There will be thousands of parallel connections for a same single silicon chip for basic MOSFETs cells [1].

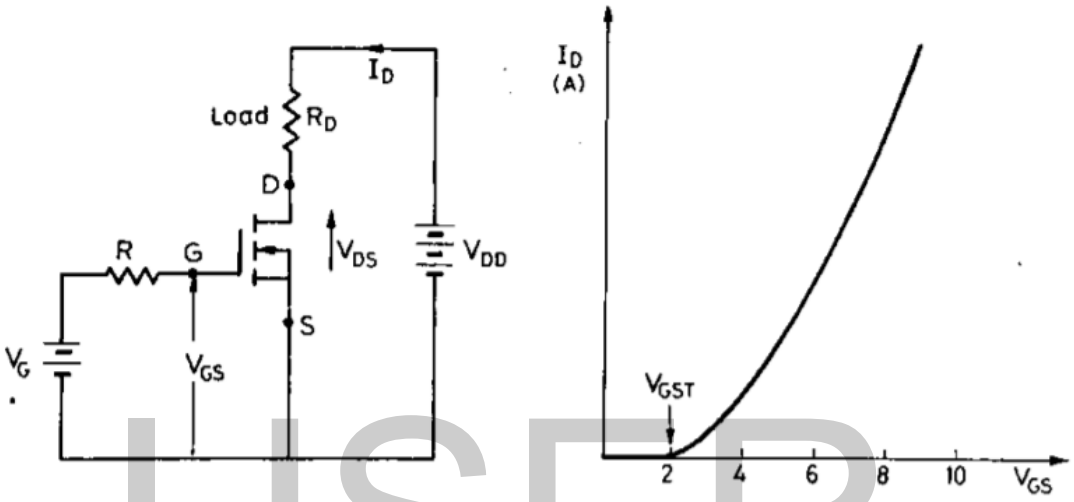
No current flows from drain to source thereby zero gate circuit voltage and n^- - p^- junctions are reverse biased when V_{DD} is there. When gate terminal is made positive with respect to source, an electric field is established and electrons form n-channel in p^- regions as shown. So, a current flow from drain to source as indicated by arrows. When gate voltage is increased drain current I_D also increased as expected. Control of n-channel length is only possible by lowering the ON-resistance where shorter channel length is used [1].

In power MOSFET, time delays caused by removal or recombination of minority carriers are eliminated because conduction is due to majority carriers. Switching frequencies

for power MOSFETs will be in the range of megahertz [1].

- **Transfer characteristics:**

Transfer characteristics shows the variation of drain current with respect to gate source voltage V_{GS}. The below transfer characteristic is drawn for n-channel power MOSFET as shown in Figure 1.10(b). From the fig is shown that there is threshold voltage V_{GST} below which the device is off. The V_{GST} will have the magnitude of 2 to 3V [1].



(a) (b)

Figure 1. 10. (a) N-channel power MOSFET circuit diagram and (b) its typical transfer characteristics [1].

- **Output characteristics:**

The output characteristics of a MOSFET are drawn between the drain current I_D and the drain source voltage V_{DS}. The characteristics curve is as shown in Figure 1.11 where the graph is almost linear by having low V_{DS} with constant on-resistance $R_{DS}=V_{DS}/I_D$. For given V_{GS}, when V_{DS} is increased, the drain current I_D should increase, but due to the applied V_{GS}, the drain current controlled at certain level. Therefore, the output drain current is controlled by the gate current. The load line intersects the output characteristics at *A* and *B*. Here, A indicates fully ON-condition and *B* indicates the off-state of power MOSFET. It acts like a switch either at point *A* or at *B* just of BJT [1].

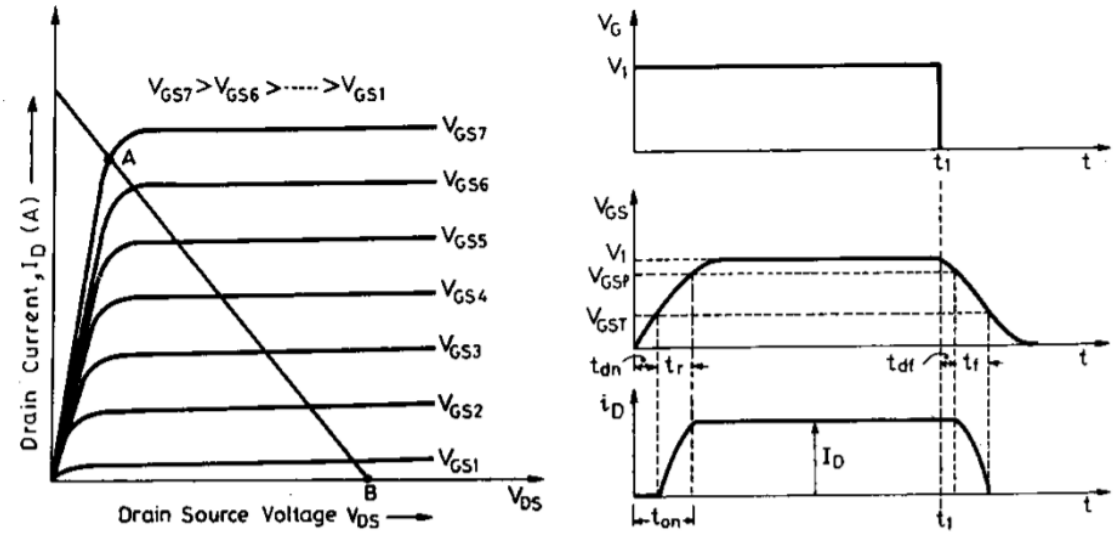


Figure 1. 11. Output characteristics and switching waveforms of a power MOSFET [1].

- **Insulated Gate Bipolar Transistor (IGBT):**

IGBT is a relatively new device in power electronics and before the advent of IGBT, power MOSFETs and power BJT were common in use in power electronic application. Both devices possessed some advantages and simultaneously some disadvantages. So, IGBT is the device which combines both the advantages of BJT and MOSFET. So, an IGBT has low on-state power loss as in a BJT and high input impedance like a MOSFET. The problem which faced on BJT with second breakdown will not present in IGBT. IGBT is known by various other names conductively modulated field effect transistor (COMFET) or Gain modulated FET (GEMFET), metal-oxide insulated gate transistor (MOSIGT). Initially it was known to be insulated gate transistor (IGT) [1].

Basic structure and working:

Figure 1.12 illustrates the basic structure of an IGBT. The structure of IGBT is very much like that of PMOSFET, except a major difference in the substrate. Substation of a p^+ layer substrate instead of the n^+ layer substrate in the IGBT named as collector. An IGBT has also contains thousands of basic structure cells collected appropriately on a single chip of silicon like that of power MOSFET [1].

When gate is made positive with respect to emitter and with gate-emitter voltage more than the threshold voltage of IGBT, an n-channel is formed in the p-regions as in a power MOSFET as shown in Figure 1.12. The n-channel short circuits the n^- region with n^+ emitter regions. There will be a substantial hole injection to the epitaxial n^- layer from P^+ substrate for electron movement of the n-channel. Hence, forward current is established eventually as shown in Figure 1.12 [1].

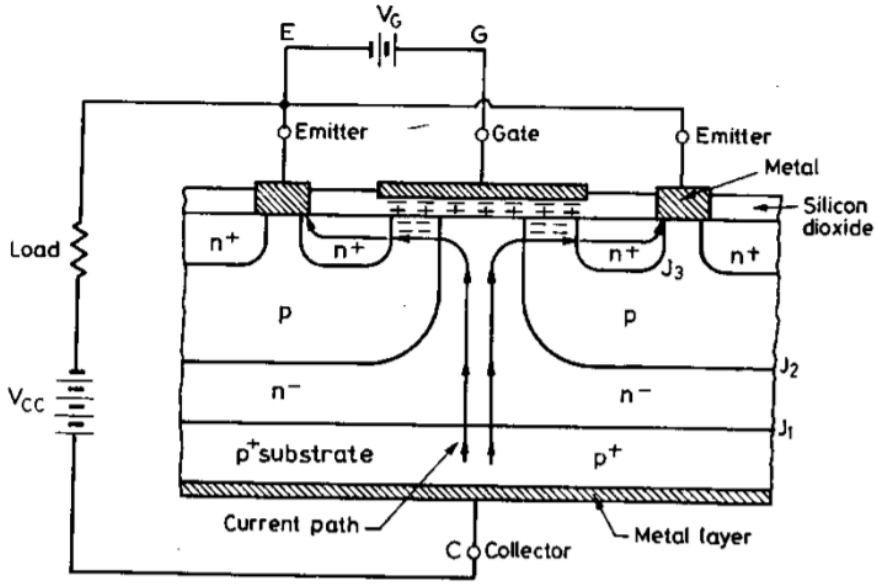
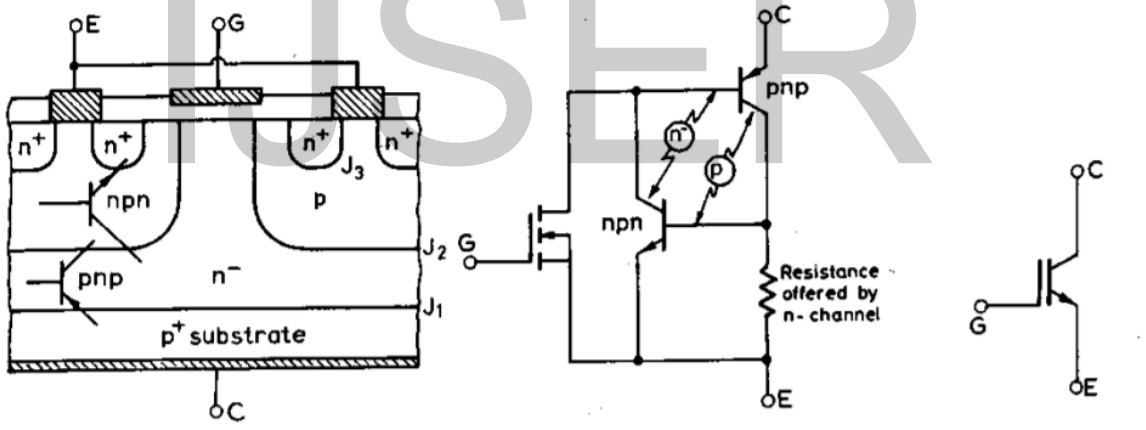


Figure 1. 12. Basic Structure of an Insulated Gate Bipolar Transistor (IGBT) [1].

The three layers p^+, n^- and p forms a PNP transistor with p^+ as emitter, n^- as base and p as collector. Also, a NPN transistor is formed by the layers n^-, p and p^+ as shown in Figure 1.12 [1].



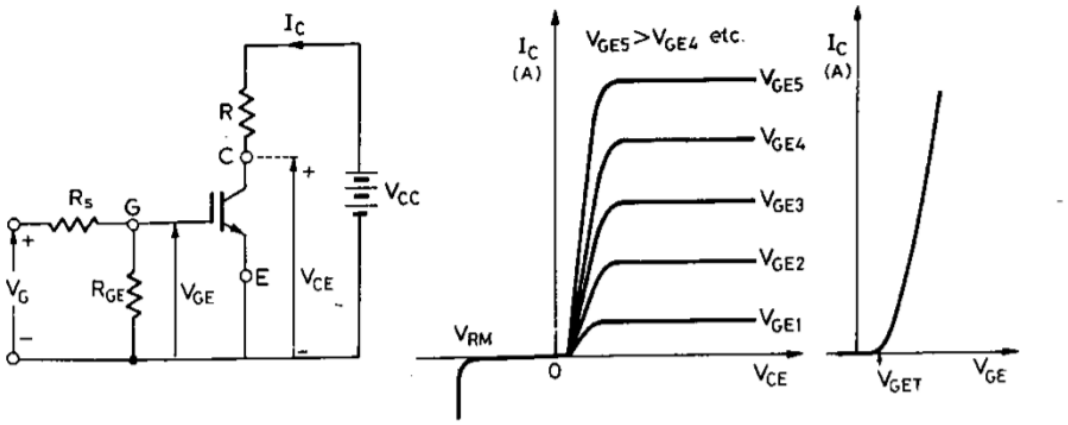
(a) (b) (c)

Figure 1. 13. IGBT (a) basic structure (b) its equivalent circuit and (c) its circuit symbol [1].

Here n^- serves as base for PNP transistor as well as collector for NPN transistor. Similarly, p serves as collector for PNP device as well as NPN transistors can, therefore be connected as shown in Figure 1.13(b) to give the equivalent circuit of an IGBT. Figure 1.13(c) is the circuit for IGBT with gate(G), emitter(E), and collector(C) as its three terminals [1].

- **IGBT Characteristics:**

The circuit of figure 1.14(a) shows the various parameters pertaining to IGBT characteristics.



(a) (b) (c)

Figure 1. 14. IGBT (a) circuit diagram (b) V-I characteristics and (c) its transfer characteristics [1].

The output characteristics or static V-I characteristics of an IGBT are drawn between the collector current I_C versus collector-emitter voltage V_{CE} for various values of gate-emitter voltages. These characteristics are shown, in figure 1.14(b). The shape of the output characteristics is like that of BJT in the forward direction. Here due to IGBT voltage-controlled characteristic, gate-emitter voltage V_{GE} is the control parameter [1].

The above Figure 1.14(c) shows the transfer characteristics of IGBT which is exactly same as PMOSFET. These characteristics are between collector current I_C versus gate- emitter voltage V_{GE} as shown. Only after when the V_{GE} is greater than a threshold value V_{GET}, then IGBT is in turn on state [1].

IGBT will go into off state when junction J_2 blocks the forward voltage otherwise there will be reverse voltage that blocks at junction J_1 across collector and emitter [1].

- **Switching characteristics of IGBT:**

The Figure 1.15 shows the typical switching characteristics of IGBT during turn-on and turn-off states. The time that is taken between the instants of forward blocking to forward on state is known as turn on time. Turn on time t_{on} is composed of two components as usual, delay time t_{dn} and rise time t_r i.e., $t_{on} = t_{dn} + t_r$. The delay time is defined as the time in which the collector-emitter voltage to falls from V_{CE} to $0.9V_{CE}$. Here V_{CE} is the initial collector-emitter voltage. The rise of collector current from initial leakage current I_{CE} to $0.1I_c$ is the time delay t_{dn} where I_C is known to be a final value of collector current. The rise time t_r is defined as the time during which collector-emitter voltage falls from $0.9V_{CE}$ to $0.1V_{CE}$ or the time where the rise of collector current from $0.1I_C$ to its final value I_C. After time t_{on}, the collector-emitter voltage and the collector current I_C falls to small value called conduction

drop=V_{CES} where subscription s denotes saturated value [1].

Delay time (t_{df}), initial fall time (t_{f1}) and final fall time (t_{f1}) and final fall time (t_{f2}) i.e., t_{off} =t_{df}+t_{f1}+t_{f2} are the time periods during the turn on t_{off}. The delay time is defined as the time during which gate voltage falls from V_{GE} to threshold voltage V_{GET}. There will be fall of collector current from I_C to 0.9I_C when V_{GE} falls to V_{GET} during t_{df}, the collector emitter voltage begins to rise at the end of t_{df} [1].

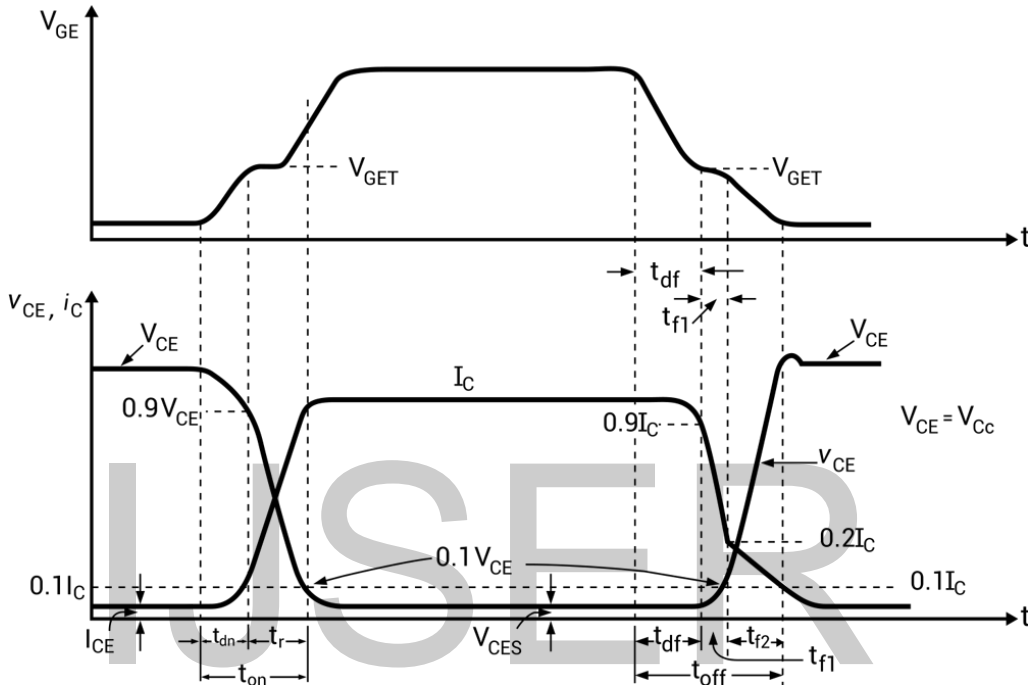


Figure 1. 15. IGBT turn-on and turn-off characteristics [1].

The first full time t_{f1} is the time during which there will be fall of collector current from 90 to 20% of its initial value I_C, or the rise of collector-emitter voltage from V_{CES} to 0.1V_{CE} [1].

As shown in figure 1.16, the final fall time t_{f2} is the time during which collector current falls from 20 to 10% of I_C, or the rise of collector-emitter voltage from 0.1V_{CE} to final value V_{CE} [1].

1.5 Comparison of BJT, MOSFET and IGBT

The comparison of BJT, power MOSFET and IGBT are outlined as below: [1]

BJT and IGBT is a bipolar device and MOSFET is a majority carrier device.

- MOSFET and IGBT is voltage-controlled devices where as BJT is current controlled device.
- BJT has negative temperature co-efficient while in MOSFET and IGBT has positive temperature co-efficient.
- The switching power loss and input impedance is high in BJT and low in MOSFET

and IGBT.

- The on-state voltage drop, and conduction loss are high in MOSFET while in BJT and IGBT it is low.
- Parallel operation is possible in BJT and it is not possible in MOSFET and IGBT,
- The voltage and current ratings of BJT is 1200V and 800A and in MOSFET 500V and 140A, and that of IGBT the ratings are 1200V and 500A.
- Switching frequency rating for BJT is (10-20KHz), for MOSFET up to 1MHz and for IGBT up to 50KHz.

1.6 comparison of Si, GaN and SiC MOSFETS

Silicon IGBTs are most widely used in many applications until the existence of wide band gap semiconductor SiC, GaN and diamond came under usage. Due to low losses and operating at higher temperatures properties, Silicon IGBT is replaced by the SiC MOSFETs. Below table 1 shows the properties of wide band gap semiconductor materials [7].

Table 1. 1 Si and Wide band gap material properties [8] [9]

	Si	GaN	4H-SiC	6H-SiC	Diamond
E_g bandgap eV	1.1	3.4	3.3	3	5.45
v_s saturation velocity cm/sec	1*10^7	2.2*10^7	2*10^7	1.9*10^7	2.7*10^7
m_n electron mobility cm^2/Vs	1350	2000	947	380	2200
e_r dielectric constant	11.8	10	9.7	9.7	5.5
E_c critical field V/cm	3*10^5	2*10^6	3*10^6	2.8*10^6	10*10^6
K thermal conductivity W/cm K	1.5	1.7	5	5	22

During recent years, SiC MOSFETs are widely used in electronic applications because of its unique properties having higher voltage blocking, lower switching losses with high band gap energy by single silicon-carbon bond. In SiC MOSFETs, because of reduction in switching losses will help to increase the switching frequency meanwhile reduces the weight and volume of the system with improved efficiency for same switching frequency. Thermal properties of SiC MOSFETs are very helpful for outer space because of extreme temperatures [7] [10].

1.7 SiC MOSFET

Figure 1.17 shows the cross-section of the SiC MOSFET where n^- region is lightly doped and n^+ region as heavily doped because of ideal drift region properties. Positive biased is applied to drain between the n^- drift region and p-well at gate as zero [11].

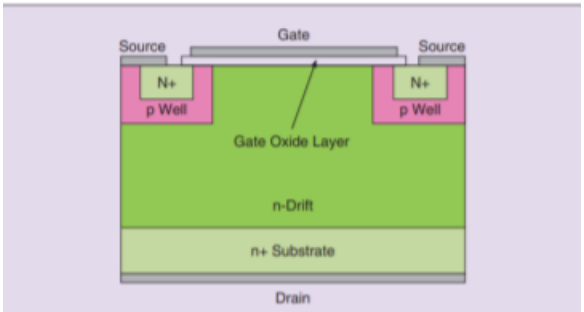


Figure 1. 16. cross-section of SiC MOSFET [12].

Due to these properties, SiC MOSFET is taken as the switch for step-down converter for hardware implementation.

2. Control Strategies of Step-Down Converter

In Power Systems, there will be lot of disturbances due to change in load and from source which may be renewable or non-renewable energy resources, but the system output should be constant without any disturbance. In energy storage systems, we use the DC/DC converters which maintains the constant output by using the different control strategies. In this chapter, control system is designed for buck converter with variable input and load for constant output.

2.1 Basic Converter

The step-down DC-DC converter, commonly known as a buck converter, is shown in Figure 2.1. It consists of dc input voltage source V_s, controlled switch S, diode D, filter inductor L, filter capacitor C, and load resistance R. Typical waveforms in the converter are shown in Figure 2.1. under assumption that the inductor current is always positive. The state of the converter in which the inductor current is never zero for any period is called the continuous conduction mode (CCM). It can be seen from the circuit that when the switch S is commanded to the on state, the diode D is reverse biased. When the switch S is off, the diode conducts to support an uninterrupted current in the inductor in figure 2.2 [13] [14].

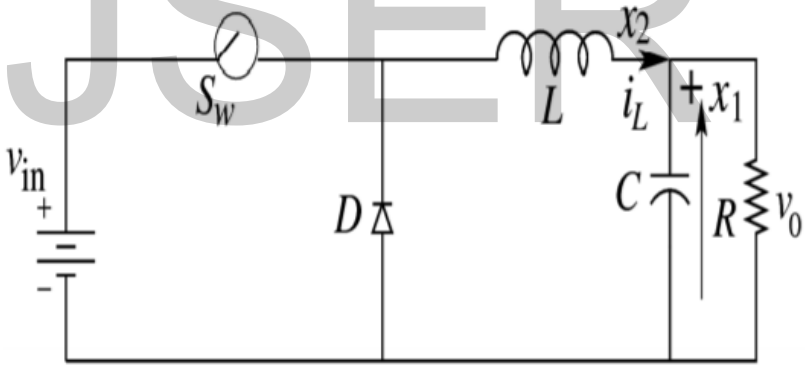


Figure 2. 1. Basic Buck Circuit [13].

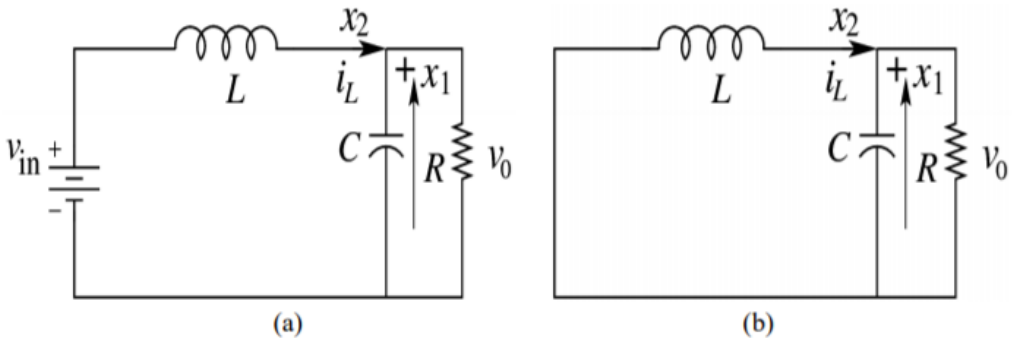


Figure 2. 2. Buck converter during (a) turn-on (b) turn-off [13].

The relationship among the input voltage, output voltage, and the switch duty ratio *D* can be

derived, for instance, from the inductor voltage v_L waveforms in figure 2.3. According to Faraday's law, the inductor volt–second product over a period of steady-state operation is zero. For the buck converter [14].

$$(Vs - V0)DT = -Vo(1 - D)T \quad (2.1.1)$$

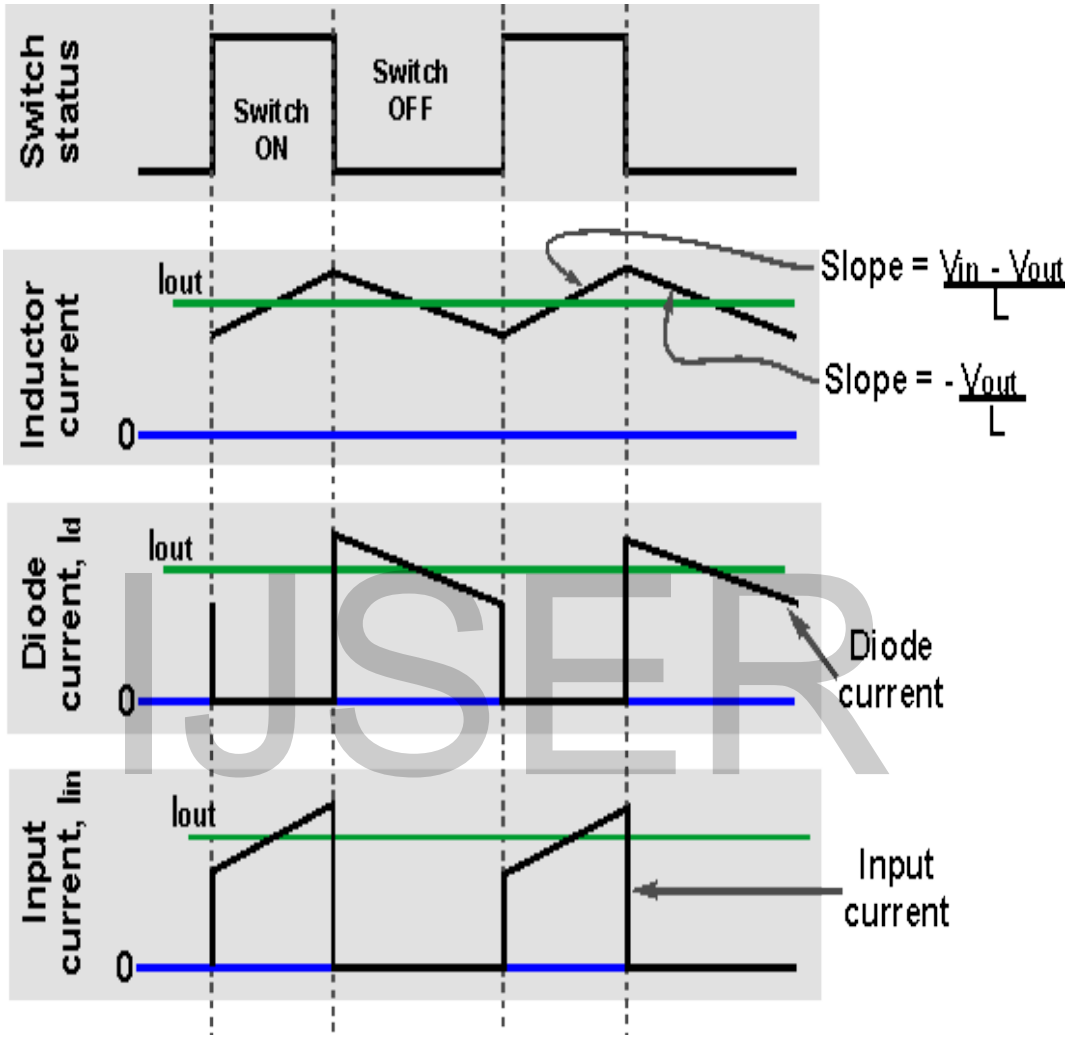


Figure 2. 3. Waveforms of buck converter.

Hence, the dc voltage transfer function, defined as the ratio of the output voltage to the input voltage, is

$$D = \frac{Vo}{Vs} \quad (2.1.2)$$

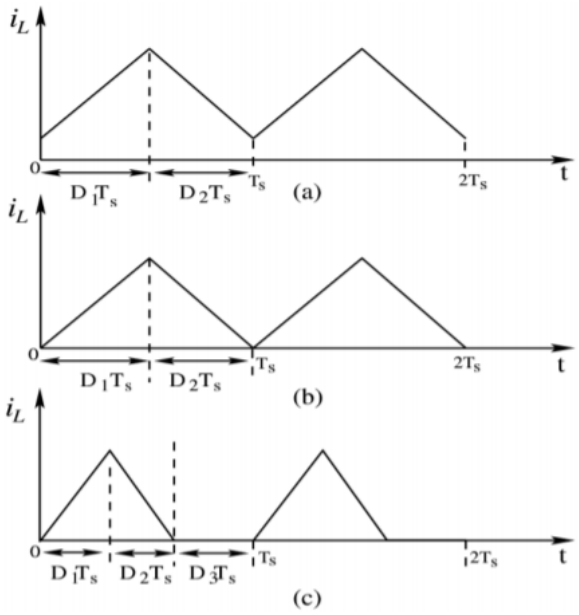


Figure 2. 4. Inductor current waveforms (a) CCM (b) Boundary of CCM and DCM (c) DCM [13].

It can be seen from above equation (2.1.2), that the output voltage is always smaller than the input voltage. The dc–dc converters can operate in two distinct modes with respect to the inductor current iL ,Figure depicts the CCM in which the inductor current is always greater than zero. When the average value of the input current is low (high R) and/or the switching frequency f is low, the converter may enter the discontinuous conduction mode (DCM). In the DCM, the inductor current is zero during a portion of the switching period. The CCM is preferred for high efficiency and good utilization of semiconductor switches and passive components. The DCM may be used in applications with special control requirements, since the dynamic order of the converter is reduced (the energy stored in the inductor is zero at the beginning and at the end of each switching period). It is uncommon to mix these two operating modes because of different control algorithms. For the buck converter, the value of the filter inductance that determines the boundary between CCM and DCM is given by equation (2.1.3) [13].

$$L = \frac{D(Vs-V0)}{2*fsw*Io} \tag{2.1.3}$$

The filter inductor current iL in the CCM consists of a dc component I_0 with a superimposed triangular ac component. Almost all this ac component flows through the filter capacitor as a current iC. Current iCcauses a small voltage ripple across the dc output voltage $V0$. To limit the peak to peak value of the ripple voltage below certain value $Vripple$, the filter capacitance C must be greater than

$$C = \frac{V0(1-D)}{8*L*Vripple*fsw^2} \quad (2.1.4)$$

The Equations (2.1.3) and (2.1.4) are the key design equations for the buck converter. The input and output dc voltages (hence, the duty ratio *D*), and the range of load resistance *R* are usually determined by preliminary specifications. The designer needs to determine values of passive components *L* and *C*, and of the switching frequency f. The value of the filter inductor *L* is calculated from the CCM/DCM condition using Eq. The value of the filter capacitor *C* is obtained from the voltage ripple condition Eq. For the compactness and low conduction losses of a converter, it is desirable to use small passive components. Equations which show that it can be accomplished by using a high switching frequency *f*. The switching frequency is limited, however, by the type of semi- conductor switches used and by switching losses. It should be also noted that values of *L* and *C* may be altered by effects of parasitic components in the converter, especially by the equivalent series resistance of the capacitor [13].

2.2 Mathematical Modelling of Buck Converter [15]

Buck Converter during ON-State:

$$-Vs + L(\frac{dil}{dt}) + Vc = 0 \quad (2.2.1)$$

$$\frac{Ldil}{dt} = Vs - Vc \quad (2.2.2)$$

$$\frac{dil}{dt} = -\frac{Vc}{L} + \frac{Vs}{L} \quad (2.2.3)$$

$$Vc = V0 \quad (2.2.4)$$

$$il = ic + i0 \quad (2.2.5)$$

$$\frac{CdVc}{dt} = il - i0 \quad (2.2.6)$$

$$\frac{dVc}{dt} = \frac{il}{c} - \frac{V0}{RC} \quad (2.2.7)$$

State Equation:

$$\begin{bmatrix} \frac{diL}{dt} & 0 \\ \frac{dVc}{dt} & 0 \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/RC \end{bmatrix} \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} + \begin{bmatrix} iL & 0 \\ 0 & 0 \end{bmatrix} * [Vs] \quad (2.2.8)$$

Output Equation:

$$[V0] = [0\ 1] \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} \quad (2.2.9)$$

Buck converter during OFF-State:

$$iL = iC + i0 \quad (2.2.10)$$

$$C * \frac{dVc}{dt} = iL - i0 \quad (2.2.11)$$

$$\frac{dVc}{dt} = \frac{il}{C} - \frac{Vc}{RC} \quad (2.2.12)$$

$$Vl = -Vc \quad (2.2.13)$$

$$\frac{LdiL}{dt} = -V0 \quad (2.2.14)$$

$$\frac{diL}{dt} = -\frac{Vc}{L}, Vc = V0 \quad (2.2.15)$$

State Equation:

$$\begin{bmatrix} \frac{diL}{dt} & 0 \\ dVc/dt & 0 \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/c & -1/RC \end{bmatrix} \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} \quad (2.2.16)$$

Output Equation:

$$V0 = [0\ 1] \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} \quad (2.2.17)$$

Small Signal Modelling:

$$\dot{x} = [A1D + A2(1-D)]x + [B1D + B2(1-D)U + [(A1 - A2)X + (B1 - B2)U]d \quad (2.2.18)$$

$$\dot{y} = X[C1D + C2(1-D)]x + [D1D + D2(1-D)]U + [(C1 - C2)X + (D1 - D2)U]d \quad (2.2.19)$$

State Equation:

$$\begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} iL & 0 \\ Vl & 0 \end{bmatrix} + \begin{bmatrix} \frac{D}{L} & 0 \\ 0 & 0 \end{bmatrix} Vs + \begin{bmatrix} \frac{Vs}{L} & 0 \\ 0 & 0 \end{bmatrix} d \quad (2.2.20)$$

$$\begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} + \begin{bmatrix} \frac{D}{L} & \frac{Vs}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} Vs & 0 \\ d & 0 \end{bmatrix} \quad (2.2.21)$$

Output Equation:

$$[V0] = [0\ 1] \begin{bmatrix} iL & 0 \\ Vc & 0 \end{bmatrix} \quad (2.2.22)$$

Transfer Function:

$$\frac{y}{u(s)} = C.B[SI - A]^{-1} \quad lets\ say\ Vs = 0 \quad (2.2.23)$$

$$\frac{V0(s)}{d(s)} = [0\ 1] \begin{bmatrix} 0 & Vs/L \\ 0 & 0 \end{bmatrix} \quad (2.2.24)$$

By the Laplace Transformation Method,

$$S.iL(s) = -\frac{1}{L} * Vc(s) + \frac{Vs}{L} * d \quad (2.2.25)$$

$$S.Vc(s) = \frac{1}{C} * ic(s) - \frac{1}{RC} * Vc(s) \quad (2.2.26)$$

$$Vo(s) = Vc(s) \quad (2.2.27)$$

$$S.Vc(s) = \frac{1}{c} * \left[-\frac{1}{LS} * Vc(s) + \frac{Vs}{LS} * d(s)\right] - \frac{1}{SRC} * Vc \quad (2.2.28)$$

$$\left[S^2 + \frac{S}{RC} + \frac{1}{LC}\right] Vc(s) = \frac{Vs}{LC} * d(s) \quad (2.2.29)$$

$$\frac{V0(s)}{d(s)} = \frac{\frac{Vs}{Lc}}{S^2 + \frac{S}{RC} + \frac{1}{LC}} \quad (2.2.30)$$

Finally, the equation (2.2.30) give the transfer function of the step-down converter.

2.3 Different types of Control Strategies

There are different modes of control for buck converter, in that mainly used methods are: [16]

1. Voltage mode control method
2. Current mode control method

- Average current control method
- Peak current control method

1. Voltage mode control method:

For dc-dc buck converter operating with voltage mode control, at first the measured output is compared with the reference voltage. Then the measured output voltage and the reference voltage will give the control voltage. So, the reason behind generation of the control voltage is to determine the switching ratio with the comparison of constant frequency waveform. The average voltage across the inductor is maintained by using the duty ratio which eventually bring the output voltage to the reference value. Thus, constant output voltage is maintained without any variation. In this method, a control signal $Vcontrol$ which is generated is compared with $Vramp$ and switching signal sent through the two conditions as below,

$$If\ Vramp < Vcontrol;\ q = 1$$

$$If\ Vramp > Vcontrol;\ q = 0$$

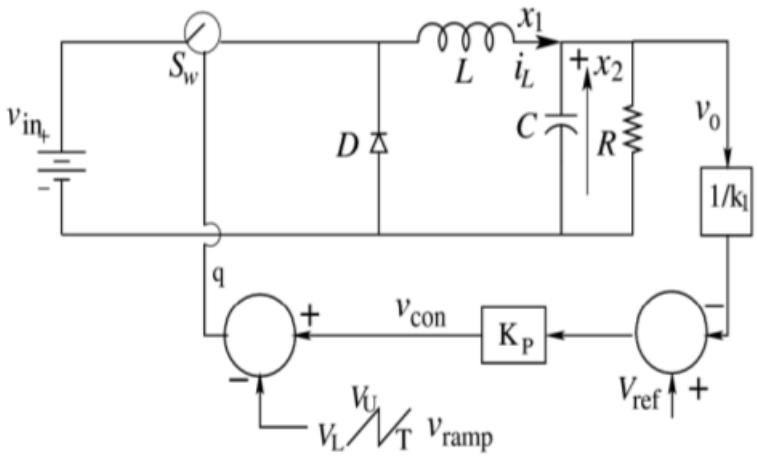


Figure 2. 5. Schematic Diagram with Voltage mode control system [16].

2. Current mode control Method:

In this method, controlling is done by the current across the inductor of dc-dc buck converter. Normally buck converter has the semiconductor switch which is to be controlled is done by the pulse width modulation (PWM). In order to control the semiconductor switch, accordingly controller is to be designed which can give the PWM output. Here, inductor current and the constant current reference is compared for effective operation of current mode control method. Firstly, inductor current will increase linearly up to constant reference value. When the inductor current Il slightly increases more than the constant reference value $Iref$ then the switch will be off and again switch on during next clock signal where this process repeats again and again.

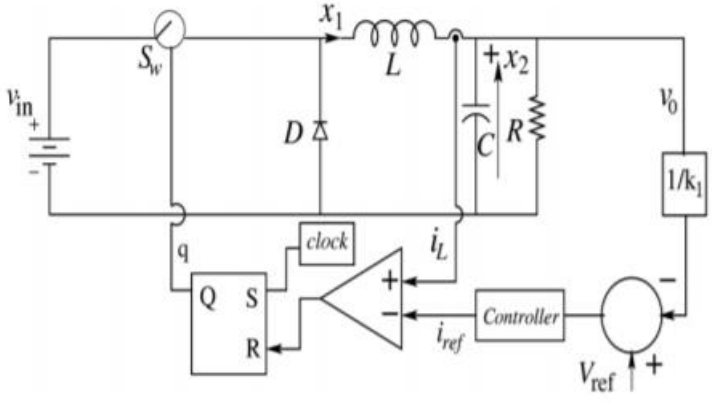


Figure 2. 6. Schematic diagram for current mode control system [16].

2.4 Practical Calculations

Buck Converter Parameters:

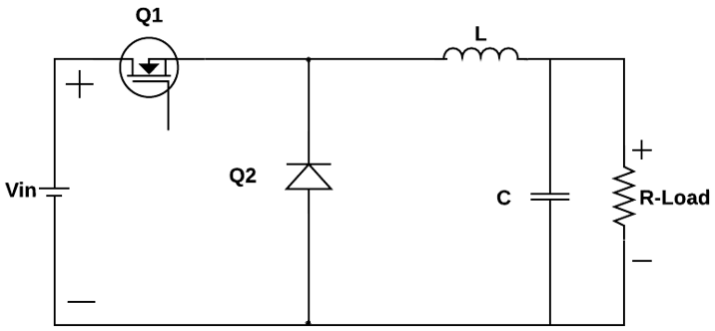
Table 2. 1 Parameters taken for buck converter

Parameters	Values
Output Voltage (V0)	54Volts
Inductor (L)	1mH
Capacitor (C)	100uF
Input Voltage (Vin)	120-150V
Load Resistance (Rl)	10-40ohms
Switching Frequency (Fsw)	100000Hz

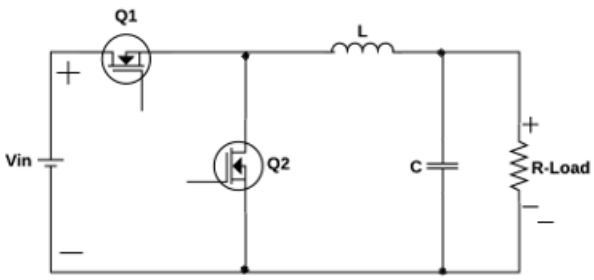
Duty Cycle, D = Vin/V0 = 54/120=0.45

2.4.1 Synchronous Buck Converter

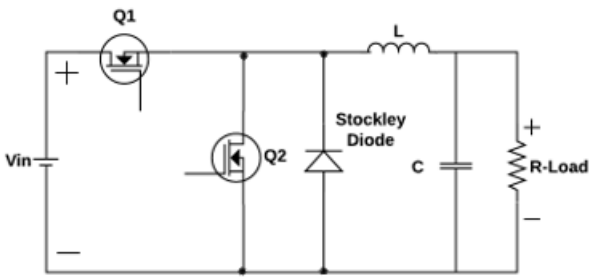
The synchronous buck converter is efficient one compared to basic buck converter. Here instead of diode used in normal buck converter, a MOSFET is used. The synchronous Buck Converter is used in order to increase the efficiency, improves the circuit performance and cost of the circuit [17]. Figure 2.7(a) shows the basic buck converter, figure 2.7(b) shows the synchronous buck converter and 2.7(c) shows the synchronous buck converter with stockley diode.



(a)



(b)

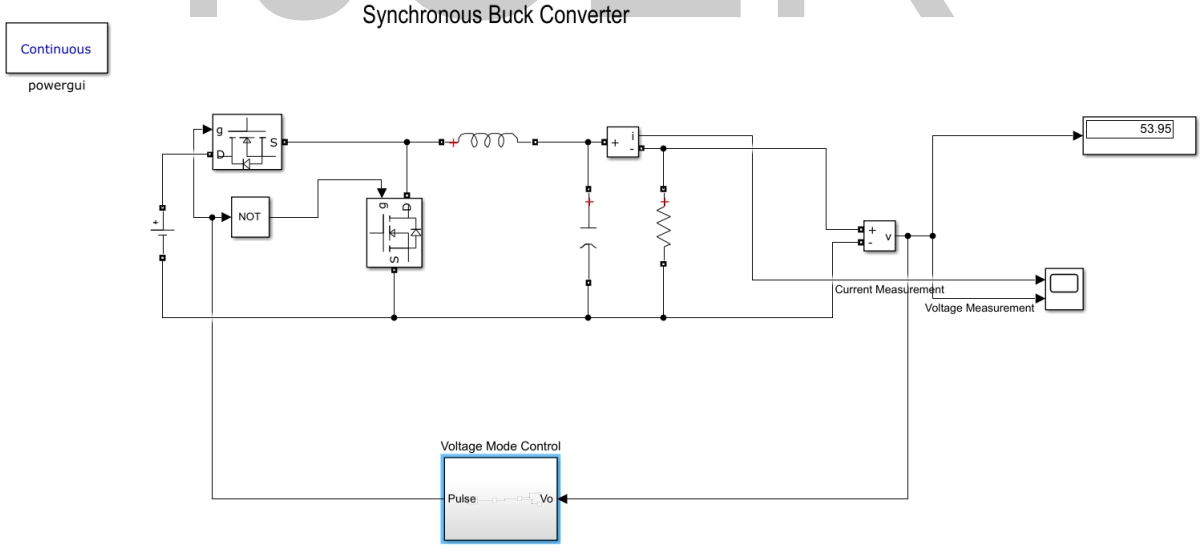


(c)

Figure 2. 7. (a) shows the basic buck converter, (b) as synchronous converter and (c) shows the Synchronous buck converter with the Stockley diode [17].

Various buck converter topologies have been proposed, the main components are *Q1*, which is the high-side power MOSFET; *L,* the power inductor; and *C,* the output capacitor. For the conventional converter topology, a power diode *D* is used. For the new buck converter topology, which is called Synchronous buck converter, a low-side MOSFET *Q2* is used. It is called a synchronous buck converter because it uses two power switches *Q1* and *Q2* that operate synchronously. The principal advantage of a synchronous rectifier is that the voltage drop across the low-side MOSFET *Q2* can be lower than the voltage drops across the power diode of the conventional converter. A MOSFET be an on-resistance Ron and operated with RMS current I_{RMS}, thus the conduction loss is $Ron*(IRMS)^2$. By using a larger MOSFET *Q2*, the on-resistance can be smaller. So, the conduction loss can be decreased as low as desired, and the total converter efficiency can be enhanced. However, the intrinsic body diode in a MOSFET *Q2* is a slow rectifier and would add significant losses if it could switch. Thus, the MOSFET *Q2* is clamped by a Schottky rectifier. This solution prevents the MOSFET's intrinsic body diode from conducting which prevents the body diode from developing a stored charge. This topology finds widespread use in low-voltage power supplies [17] [18].

2.4.2 Practical Results of Synchronous Buck Converter:

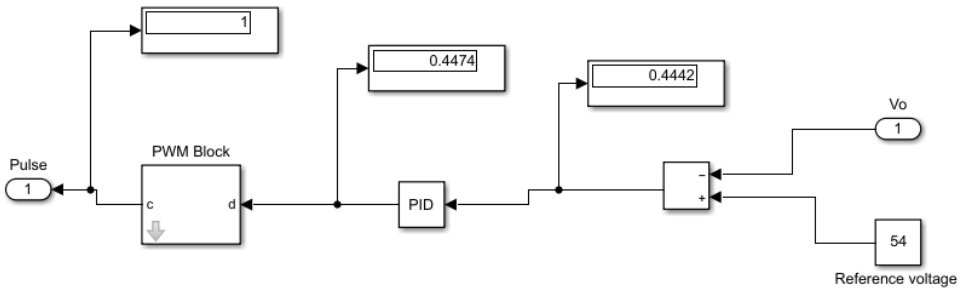


(a)

Figure 2.8(a) shows the synchronous buck converter with voltage mode control system where figure 2.8(b) shows the design of control system and figure 2.8(c) shows the pulse width modulation technique applied to the converter. Then simulations results achieved with 54V constant voltage by varying input voltage from 120-150 for 10-40ohms. In this pi tuning is

done by trial and error method which is commonly used for industrial applications. In the figure 2.9, there is oscillations before output voltage coming to steady state because of the control system which is only compared output voltage with reference voltage where it leads to disturbances for some period of time which we can call it EMI in the hardware circuit for this design.

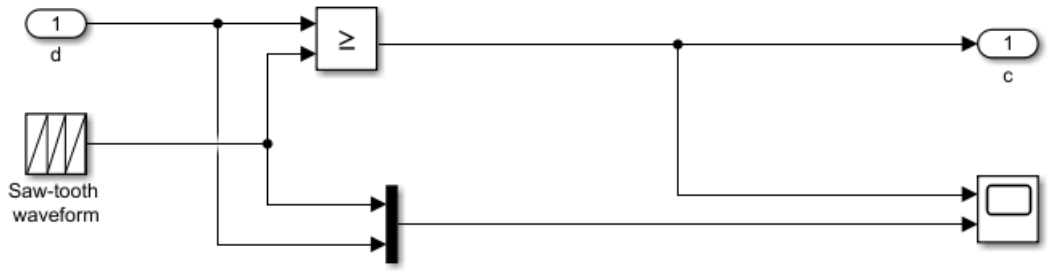
Voltage Mode Control System:



(b)

Figure 2.8(b) shows how the output voltage is compared with the reference voltage 54V in order to achieve constant output voltage. The compared value is tuned by the pi controller and that tuned value is compared with sawtooth waveform as shown in figure 2.8(c) by the relational operator to get the pulse which is given to the gate of the MOSFET high side. Then after giving the pulse the MOSFET will conduct according to pulse and give the output voltage of 54V.

Pulse width modulation:



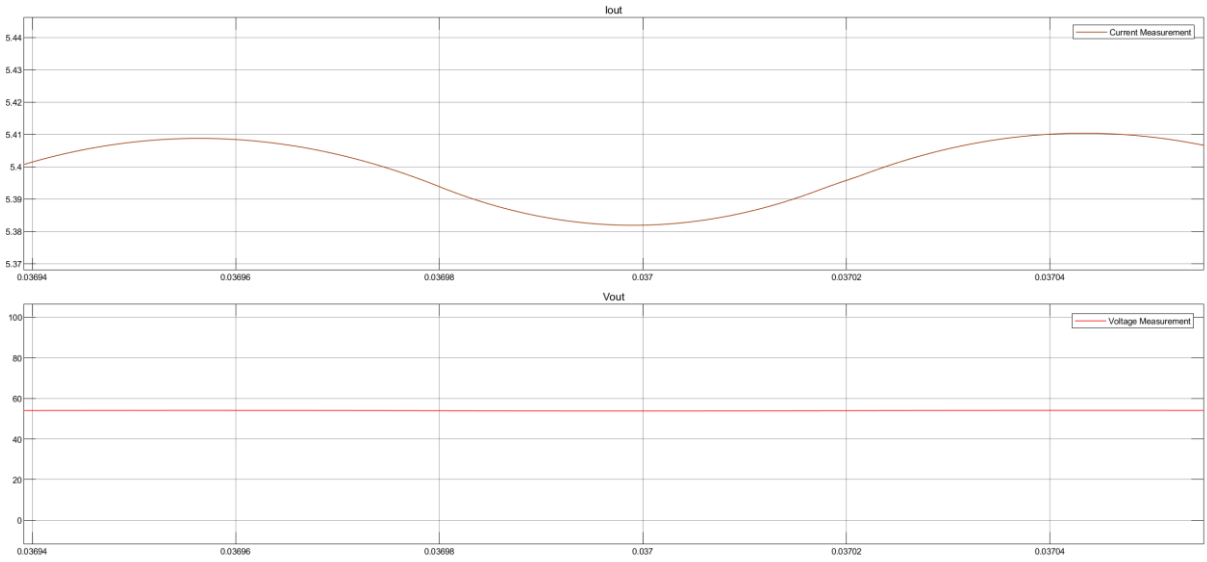
(c)

Figure 2. 8. (a) Synchronous Buck Converter (b) its voltage mode control system and (c) its PWM.

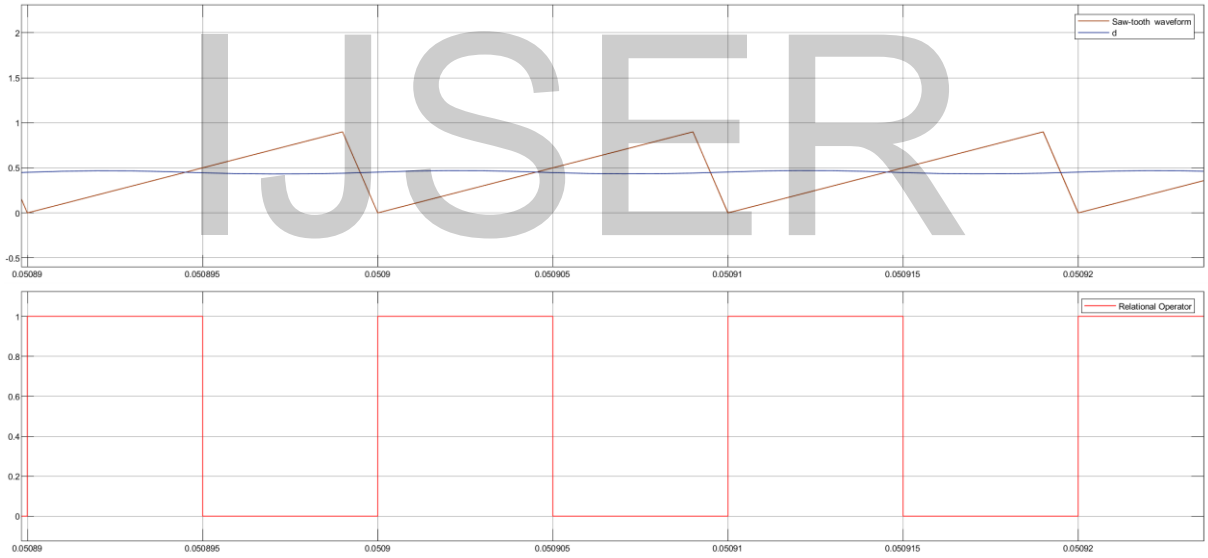
Figure 2.9 will also tell, by using the voltage mode control system for dc/dc buck converter is simple by controlling shorter on time and when there are more oscillations there is the high noise which can be tolerated. But difficult to achieve phase compensation. [19] Due to some instability in the closed system due to oscillations, controlling of voltage and inductor current

is done which is known to be current mode control system for dc/dc buck converter.

Simulink Results:



(a)



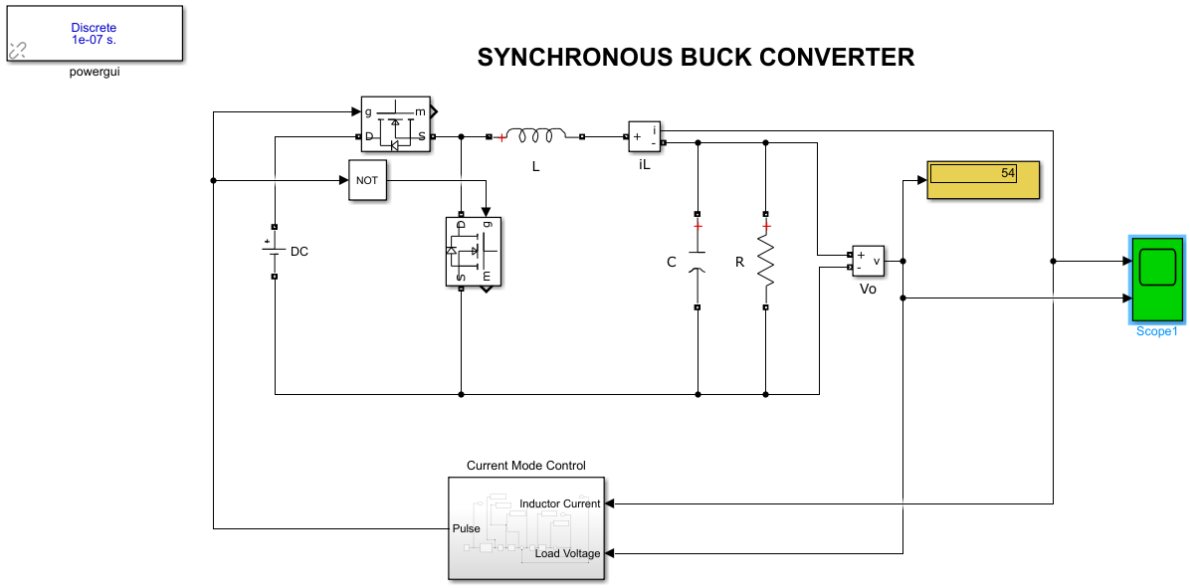
(b)

Figure 2. 9. Simulation Results (a) output voltage and inductor current (b) its PWM for synchronous buck converter with voltage mode control system.

2.4.3 Current mode control method:

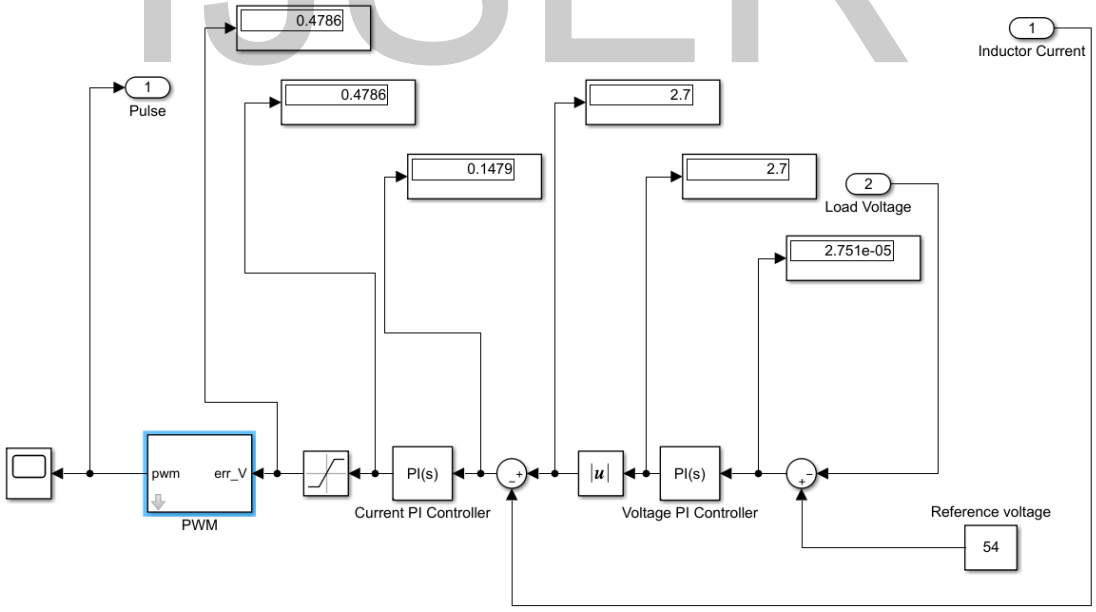
Figure 2.10(a) shows the simulation of synchronous buck converter by using current mode control system which is shown in figure 2.10(b) with PWM from figure 2.10(c). in this voltage comparison and the compared value is again compared with the inductor current and that value is tuned to pi controlled. Output of pi controller is compared with the sawtooth wave by relational operator in order to achieve output voltage constant. In this method, output

voltage is steady soon because of its high stability closed loop with load transient faster. But disadvantage in this system is low noise tolerance.



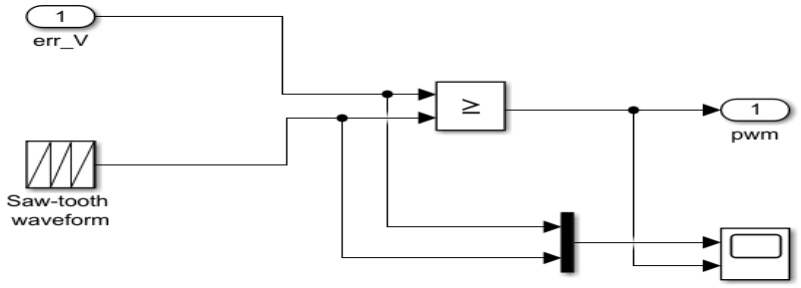
(a)

Control system:



(b)

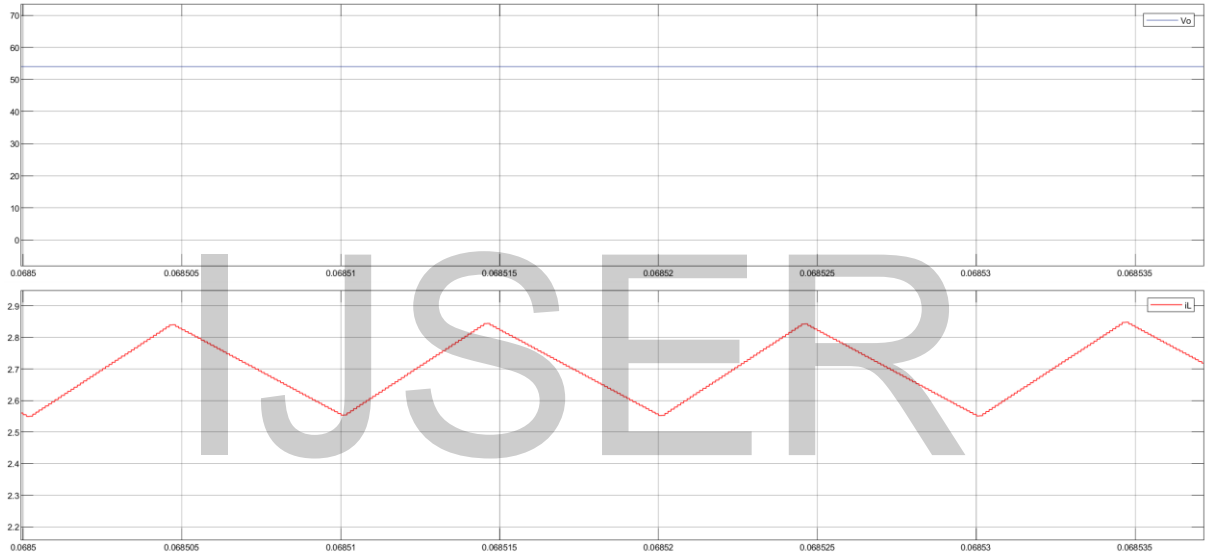
from figure 2.10(c), pulse is given to MOSFET for conduction in order to achieve 54V for 120-150V input and 10-40ohms load which is variable for the switching frequency of 100000Hz.



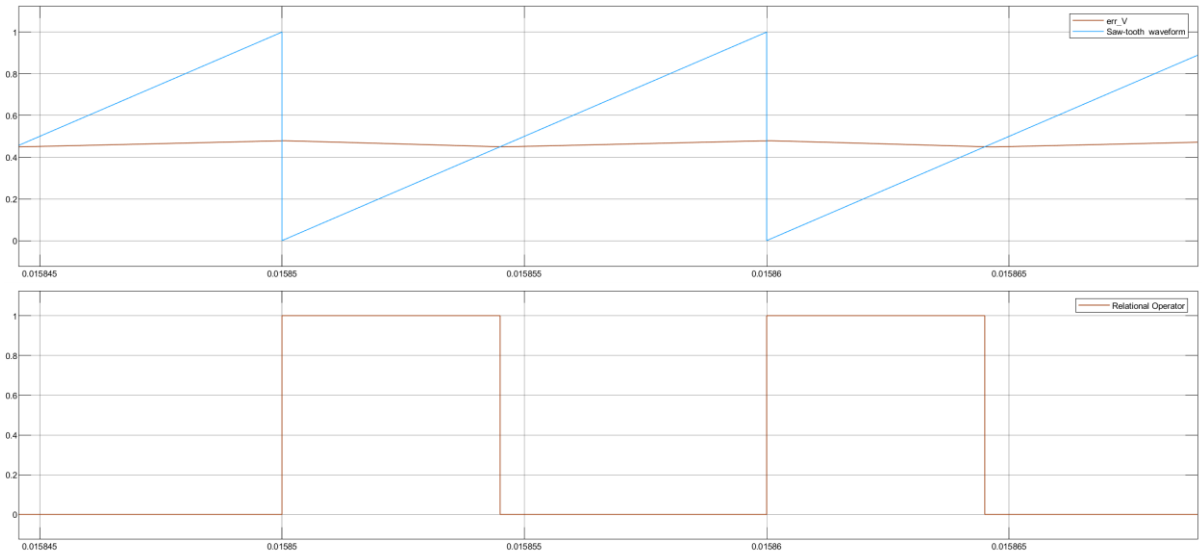
(c)

Figure 2. 10. (a) synchronous buck converter (b) its current mode control system (c) and its PWM.

Simulation Results:



(a)



(b) Figure 2. 10. simulation results for synchronous buck converter (a) inductor current and

output voltage (b) its PWM for current mode current system.

In conclusion, comparison is done by using the voltage and current control systems for synchronous buck converter where in voltage control mode, in order to get output voltage constant, use of control system is voltage mode by taking voltage reference where we cannot get the accurate output and also there will be oscillations in the output voltage and current. So, in order to implement and reduce those oscillations, current mode control system is used. Normally, these oscillations are known to be EMI which effects the system in hardware implementation. From simulation with current control strategy, output is constant for given input voltage and load with reduction of oscillations because in this strategy both voltage and current reference are taken for control. Below Table 2.4 shows, from which range of voltage and load the output is maintained constant.

Table 2. 2 Results of synchronous buck converter with current mode control system

Input voltage (120-150) V	Output voltage (V)	Duty Cycle(d)	Load (10-40 ohms)
120	54	0.45	10
135	54	0.4	20
150	54	0.36	40

From the table 2.2, by using current control system for step down converter desired voltage is achieved.

3. Energy Storage Systems

At present, Renewable Energy sources are increasing where we want to maintain the constant output without any fluctuations and disturbances to transfer power to the grid. So, there is dc/dc converters or dc/ac converters in between the sources which is supplying and to the grid. The dc/dc converters are bidirectional converters where the voltage is stepped down (Buck) or stepped up (Boost) according to the usage [20]. In this chapter, there will be the discussion of some energy storage system topologies.

Recently, due to capability of bidirectional transfer of energy between two buses increasing the need of bidirectional dc/dc converters to the systems. Energy storage in renewable energy systems, fuel cell energy systems, hybrid electric vehicles (HEV) and uninterruptible power supplies (UPS) need bidirectional dc/dc converters apart from traditional application in dc motor drives [21] [22]. Renewable energy sources like solar and wind have the fluctuations which is unsuitable for standalone operations for sole source of power. In order to solve this problem, by compensating the fluctuations to get the smooth and continuous power flow to the load there is the need of energy storage device besides renewable energy resources. So, for medium power range commonly batteries and super capacitors are used where dc-dc converter is required to allow the energy as exchange between storage device and the rest of the system. Then, bidirectional power flow control capability should be there for converter in all operating modes with flexible control [20] [23].

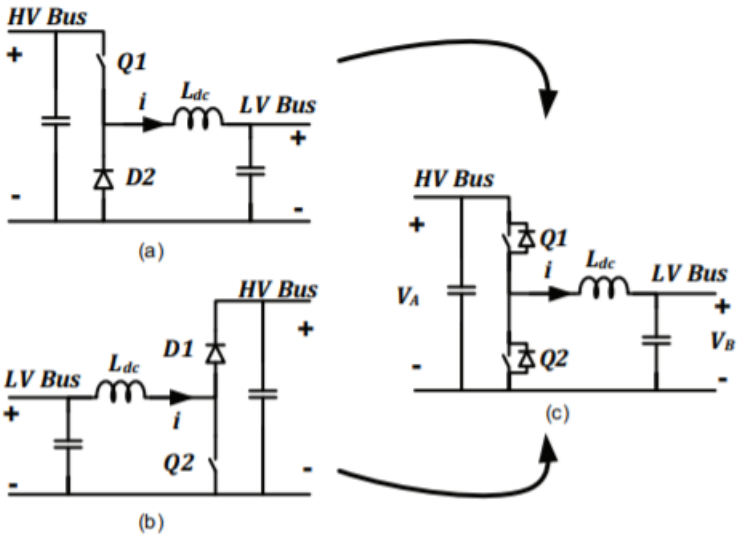


Figure 3. 1. a) unidirectional buck converter b) unidirectional boost converter c) bidirectional dc/dc converter [20].

Figure 3.1 shows how the unidirectional buck and boost converters changed to bidirectional

converters in their structure with the help of replacing diodes. The basic dc/dc converters where buck and boost converters do not have the capability of power flow in a bidirectional manner due to presence of diodes in their topology which do not have the reverse current flow. Figure 3.1(a) represents the buck mode where power is transferred from high voltage (HV) to the low voltage(LV) where Q1 is active switch meanwhile fig(b) represents boost mode where power transferred from low voltage (HV) to the high voltage (HV) with Q2 active switch.

Figure 3.1(c) shows non-isolated bidirectional dc/dc converter where it operates as buck mode in one direction and boost in the other [20].

3.1 Battery Energy Storage Systems

The electrical energy which is used to store energy in the form of electro-chemical materials includes batteries, power conversion system, and battery management system of the system [24].

If the source is solar then standalone system is used during daytime but at night or need to store the extra energy, a battery is needed which is battery storage system. For effective storage of energy, the one of the main objectives is power flow management [24] [25].

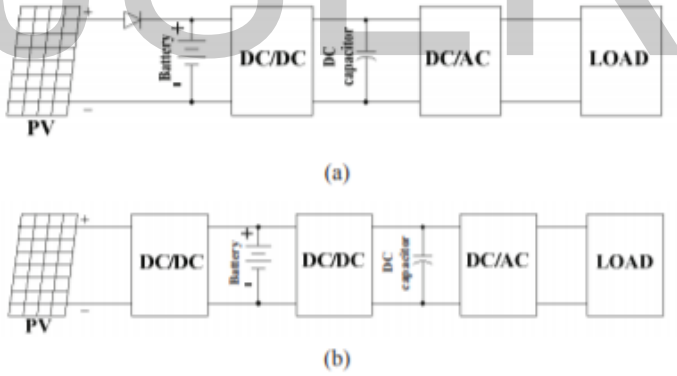


Figure 3. 2. main topologies of battery storage techniques used for standalone and grid connected inverter [24].

From the figure 3.2, we are using the dc/dc converter which is bidirectional converter used to step-up or step-down the voltage and is given to the inverter as shown.

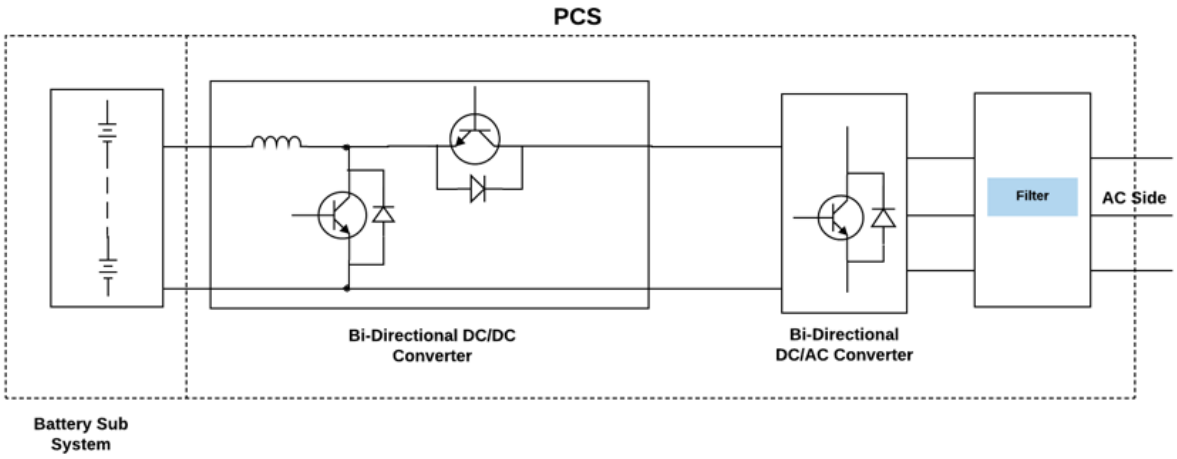


Figure 3. 3. PCS topology with ac/dc and dc/dc links [26].

Above figure 3.3 represents the one of the topologies of battery energy storage system (BESS) which is the two-stage conversion topology which refers to the two stage Power conversion system (PCS) with dc/ac and dc/dc links. The dc/dc link which is bidirectional will provide stable voltage with boosting and reducing the voltage. This topology will give strong adaptability and flexibility due to this dc/dc link in the power conversion system. In order to suppress the voltage fluctuation which are caused by directly connecting such distributed resources(DR) to grid by the connection of intermittent distributed resources with strong fluctuations which are applicable but in other side, the efficiency of power conversion system will be reduced because of dc/dc link [26] [27].

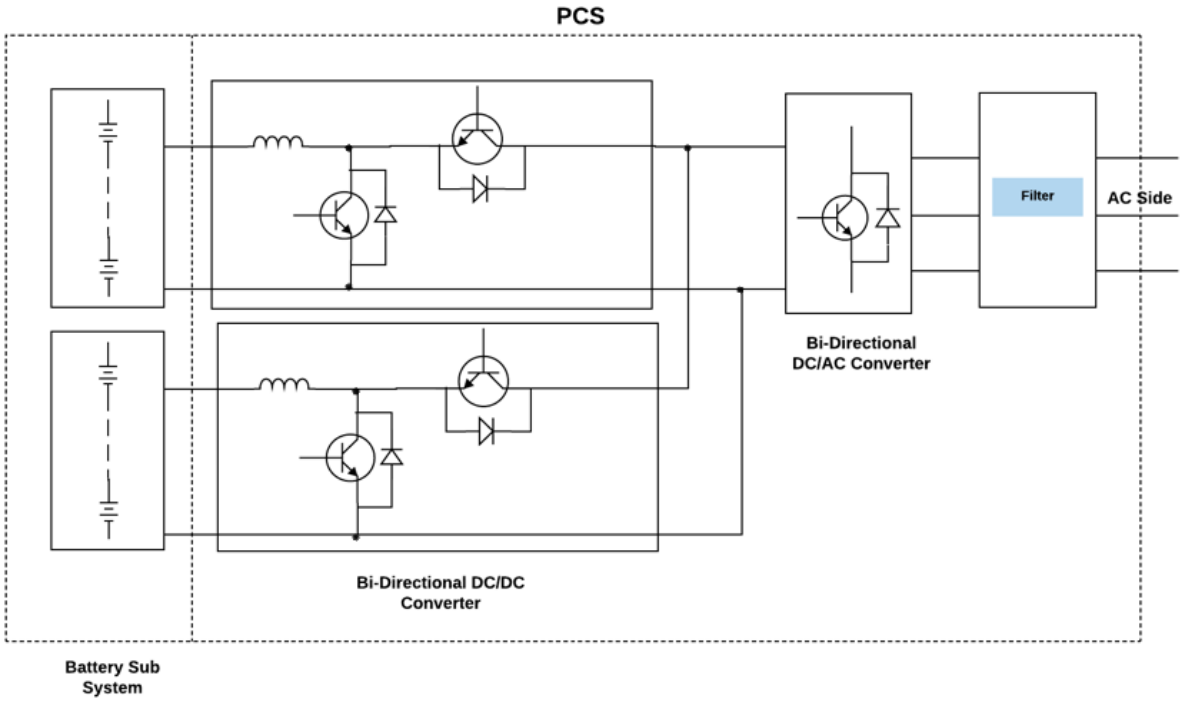


Figure 3. 4. PCS topology with dc/dc links connected in parallel on the dc side of dc/ac link [26].

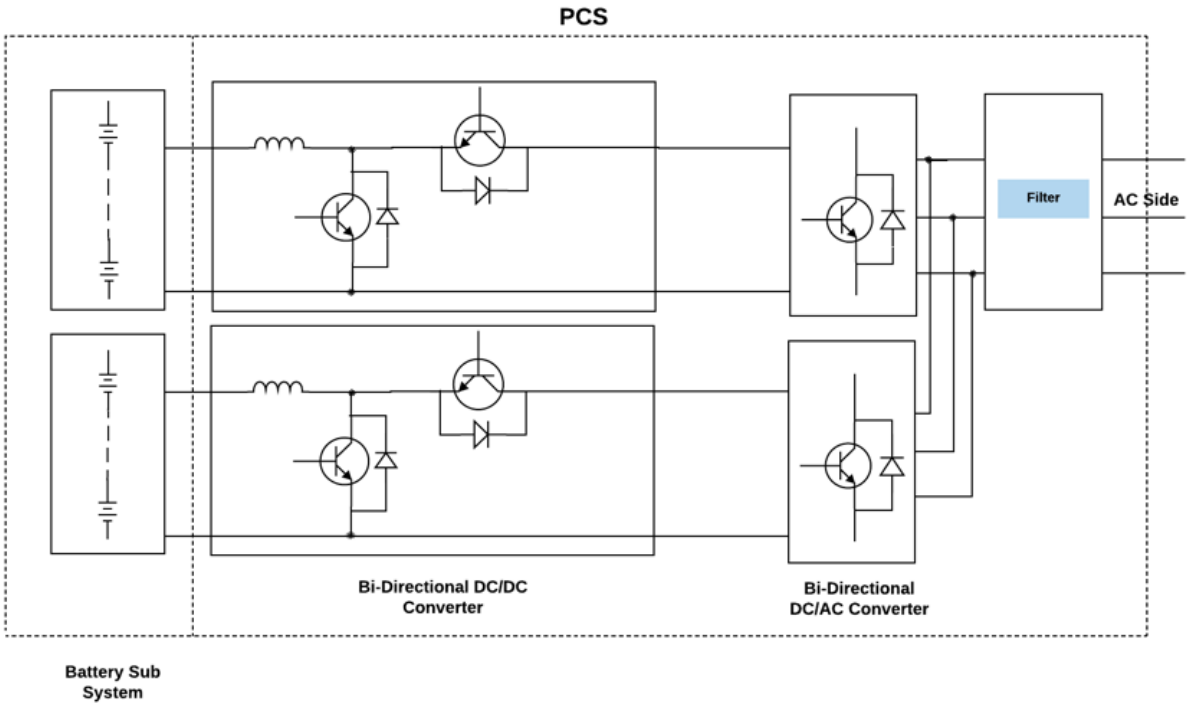


Figure 3. 5. PCS topology with dc/dc and ac/ac links connected in parallel on the ac side [26].

For ease of capacity expansion, the above figures 3.4 and 3.5 shows, the topologies which are connected in parallel for two stage conversion.

3.1.1 Applications of Battery Energy Storage Systems:

for bulk generation domain: In order to maintain the stability of electric power system (EPS) and perform the frequency regulation service, the BESS is connected to generation facilities directly or via step-up transformer which is used for Bulk BESS station [26] [28].

Transmission and distribution domain: In this BESS will be in different topologies for power conversion system and connect to transmission and distribution via step-up transformer or directly which maintain the stability of the electric power system [26].

Customer domain: This is at low voltage level which directly connected for customer facilities with low voltage topologies. In this domain, the BESS used to enhance the reliability of the electric power system at customer side, reduce the power loss and optimize the power quality [26].

3.2 Hybrid Energy Storage System

Energy storage system plays an important role for hybrid electric vehicle (HEV), plug in hybrid electric vehicles (PHEV) and all vehicles [29] [30]. Up to now, most widely battery energy storage system is used but it has several cons like low power density, battery life, and high cost. So, that is the reason where other strategies are used to implement the drawbacks of

battery energy storage system. In order to get the high-power density, the battery need high power density, and which increase the size of battery leads to increase the cost of energy storage systems. Typically, it's very tough to balance the individual cell voltage in the battery pack where there are more number of battery cells in a pack is very high and also demand of instantaneous power will need for batteries used in electric vehicles. At these situations, the instantaneously varying power input and output conditions where there is frequent charge and discharge in the batteries lead to effect the life of the battery. Because of these drawbacks, researchers find the hybrid energy storage system which is the combination of batteries and the super capacitors [31] [32].

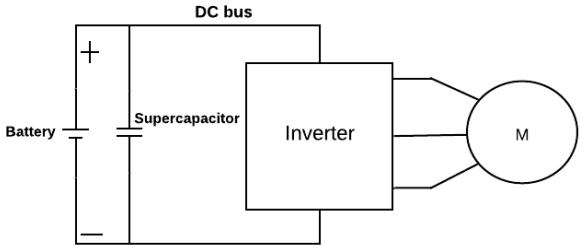


Figure 3. 6. passive parallel configuration [31].

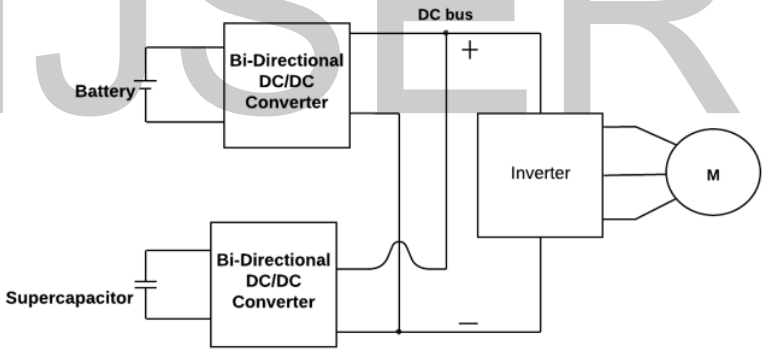


Figure 3. 7. fully active configuration [31].

Figure 3.6 shows the passive and active topologies where in passive configuration which is simple with batteries and super capacitors without any electronic converters/inverters. So, there will be high efficiency and low cost but in order to increase the capacity there will be usage of more supercapacitors directly to improve the filter performance in order to protect the battery will increase the associates cost [31].

And in the active configuration, there will be electronic converters which are converted to DC bus where dc bus voltage is more than the voltages of the battery and supercapacitors which are maintained independently which allows to utilize the functionalities of supercapacitors fully. In this topology, there is increase of cost and decrease of system efficiency [31].

From figure 3.6, it shows the SC/battery and battery/SC configuration where in SC/battery

topology there is usage of bidirectional converter which is interfaced with supercapacitor but allowing the wide range of SC voltage. This topology is widely used but there should be large size of bidirectional dc/dc converters because it must handle the SC power flow. However, due to high pulsed charging and discharging power conditions of supercapacitor frequently will reduce the overall efficiency of the system [31] [33].

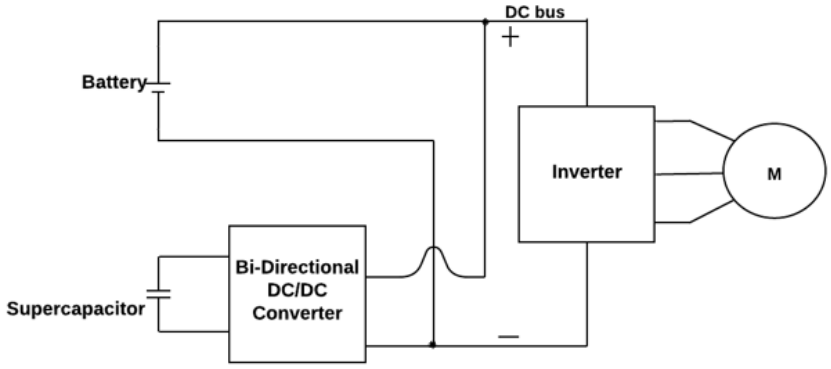


Figure 3. 8. SC/battery configuraton [31].

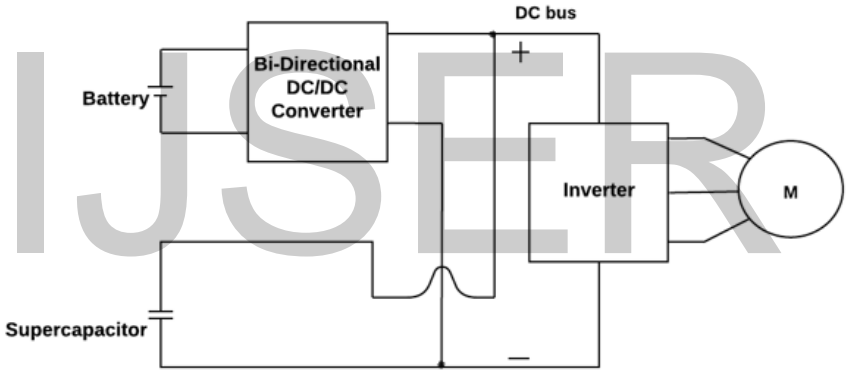
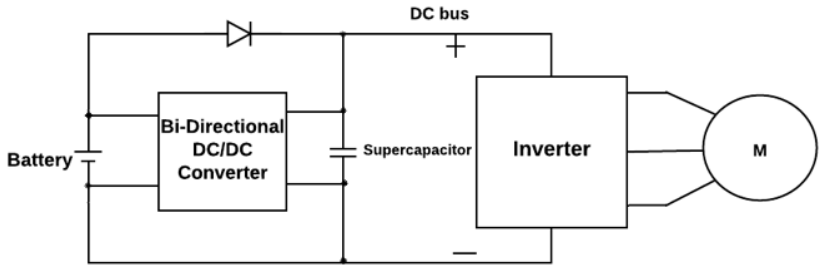
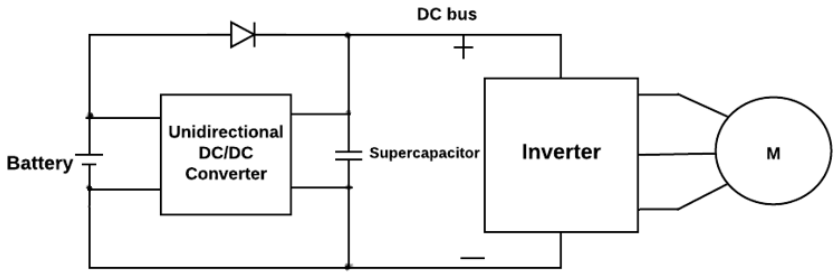


Figure 3. 9. battery/SC configuraton and viceversa [31]

In battery/SC topology, battery is directly connected to the bidirectional dc/dc converter and supercapacitor to the dc bus which works as a low pass filter. Its not recommended for some applications to use because of requirement of full size converter and wide variation of dc bus voltage [31] [34] .



(a)



(b)

Figure 3. 10. (a) and (b) A semi-active configuration topologies [31].

Figure 3.10 shows the semi-active hybrid energy storage system where in one topology diode is used with small dc/dc converter. In this. DC/DC converter acts as a controlled energy pump in order to maintain the SC voltage higher than the battery voltage where constant load profile created for the battery. Whereas in another topology unidirectional dc/dc converter is used instead of bidirectional dc/dc converter [31] [35].

4. EMI Reduction

Over six decades, the use of power electronics is developing and increasing. For example, dc-dc converters are used in portable electronic devices as primarily supplies power from batteries. Mostly all electronic devices have its own voltage with more sub-circuits which is different from the battery or external supplies. And stored power will drain away with the voltage of the battery declination. Then dc/dc converters provide the voltage from half reduction of battery voltage which allows to reduce the space without using multiple batteries. Mostly, electrical or electronic devices will have the components with having sudden change of current which leads to EMI. The unwanted disturbances in the electronic devices is due to electromagnetic conduction or electromagnetic radiation from the outside(external) sources. These disturbances will limit the performance of the devices [36] [37].

DC-DC converters are widely used in many applications, but due to the electromagnetic interference (EMI), the performance of converters is affected. There are so many technical methods where there is possibility for reduction of EMI. Mostly, while simulating in the MATLAB there will be oscillations in the output voltage at starting for some period and then give the steady output due to the passive elements present in the circuit. And, while designing the converter in the PCB layout, due the parasitic inductance and capacitance there will be EMI. Due to inductance, there will be flux which causes some disturbances leads to affect the output. So, in order to reduce the EMI in the hardware setup PCB layout should be accurate with less distance between the passive components where there is the possibility of reduction in EMI. There are two types of EMI one is conducted EMI, and another is radiated EMI in terms of frequency. The physical contact of conductor will cause the conducted EMI at lower frequencies usually in between 10kHz to 30MHz and without physical contact of conductor is radiated EMI which is caused by induction at higher frequencies. There are two modes of noises in the conducted EMI, one is common mode noise where conduction through all lines in same direction with power line and ground. Another is differential mode conducted through all line in inverse direction and exist between power lines [38].

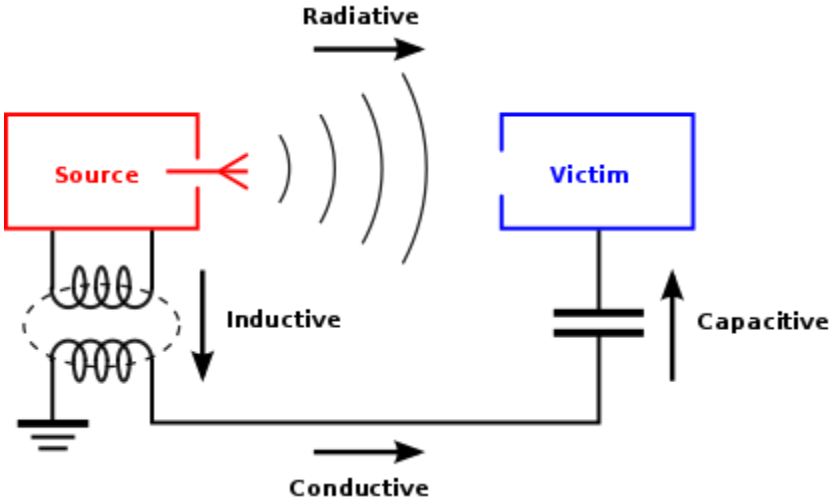


Figure 4. 1. EMI coupling modes [38].

So, in converters there will be flow of differential mode current in and out through power leads and load (or source) of the power supplies which are not dependent on the grounding. And there are no differential mode current flows through the ground connections because there will be common mode current flows through the parasitic capacitors and inductors to the ground. Empirically, the noise currents will be differential mode if frequency is below 5MHz meanwhile, above 5MHz will be common mode. There are radiated EMI in the converters when the frequency is in between 30MHz to 1GHz which generate electric and magnetic fields which can reduced by physically assembling the device of noise emitted source near to source and load [36].

Electromagnetic compatibility:

EMC is a referred word to operate at intended temperature without causing EMI for other electronic devices. There are two basic concepts to understand in order to know about EMC requirements. 1. Emissions and 2. Susceptibility [39] [40].

1. Emissions:

This issue is known as to suppress the unwanted generation of electromagnetic energy by taking countermeasures to reduce and to avoid to effect outside environment [36].

2. Susceptibility:

It refers to the right operation of the electrical equipment in the presence of electromagnetic disturbances. The EMC standards are internationally accepted and adopted between significant countries after it recognized in the year 1930. These standards will help for the electronic and electrical products with control systems in order to reduce emission of EMI [38].

Why do we have to fight with EMI in dc-dc converters?

Normally, as we know that dc-dc converters will convert source of direct current from one voltage level to the other voltage level with the help of duty cycle in the device with main switch. The dc-dc converters widely used in almost all electrical and electronics devices like mobile and data communications, computers, industrial devices, military and spacial systems. For laptops, computers applications will be charged by direct current. So, dc-dc converters play major role in electronic device where ac-dc converters needed to convert supplied ac from sockets to dc inputs which is given from batteries. Therefore, electronic devices have its own voltage requirements which are not same as those supplied from batteries and external sources where power of battery drains away. Advantage in this is there is no need of additional batteries for required voltage by using dc-dc converters with less space. dc-dc converters are classified depending on power levels in to high, low and middle with isolated and non-isolated topologies. So, for effective use of all application, there should be some techniques which helps to reduce EMI [38].

4.1Conventional methods to suppress the EMI [36]

1. EMI Filtering
2. Electromagnetic Shielding
3. Soft Switching
4. Random Modulation

There are different methods in order to suppress the EMI, but EMI filtering is one of the old techniques used to reduce the conducted noise with low frequencies whereas for high frequencies, there will electro-magnetic shielding, soft switching and random modulation.

1. EMI Filtering:

EMI in the converters due to pulsating input currents and change of voltage and current mostly happens in inductors and capacitors. So, EMI filter is need at the input side of the converter where there are common mode and differential mode noises referred from conducted EMI. Below figure shoes the two functions of blocks where C_x and differential choke helps to filter the differential mode noise. In a same way, C_y and common choke filters the common mode noise [36].

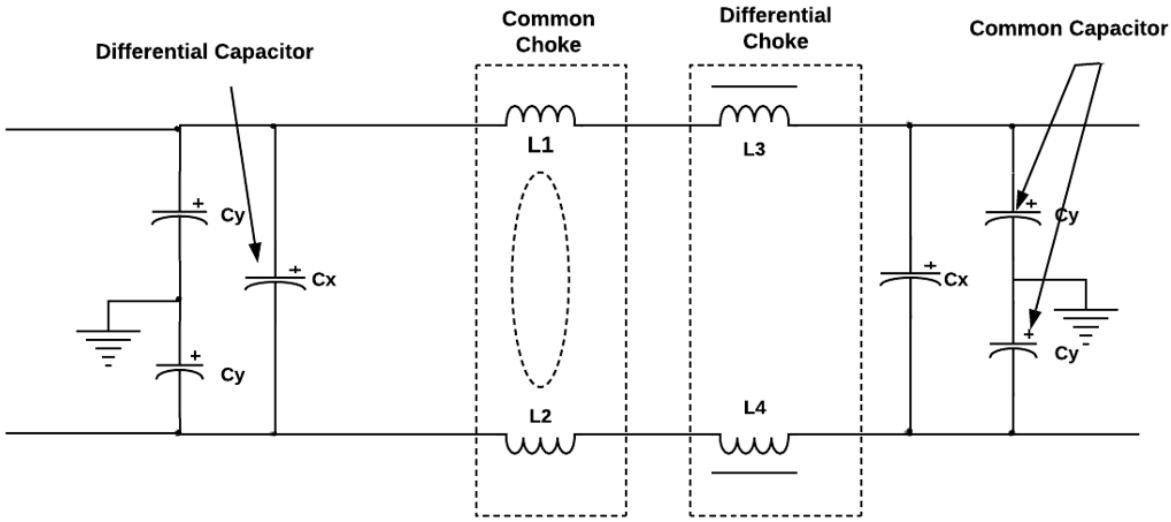


Figure 4. 2. EMI Filter [38].

For converters, this method is used to suppress conducted EMI effectively but this filter is large for using in the converter and also while eliminating the differential and common mode noises it will also eliminate some useful signals in some applications [36].

Passive filter:

In this, there will be inductors and capacitors which is *LC* filter. Due to narrow bandwidth, there will be suppression of some part of noise only possible. So, in order to this limitation, tuned EMI filter can be used with conventional one but have to check the size, weight and temperature constraints [36].

Active filter:

This consists of active operational amplifiers with small passive components where these filters are also used recently for power electronic applications which is effective [36].

Hybrid EMI filters:

It consists of both active and passive filters where there will be effective suppression of noise. Here compensating current is injected for the hybrid filters. Design of capacitors and inductors for EMI filter must be effective in order to suppress the EMI but volume of these filters is too huge where design is possible for narrow band [36].

2. Electromagnetic Shielding:

In this method, there will be penetration of electromagnetic fields with the help of conductive material by blocking those fields. Even though this method is effective, but cost is too high in order to suppress the EMI. This shielding will be used to block the radio frequency electromagnetic radiation where its range is from 3kHz to 300GHz [38].

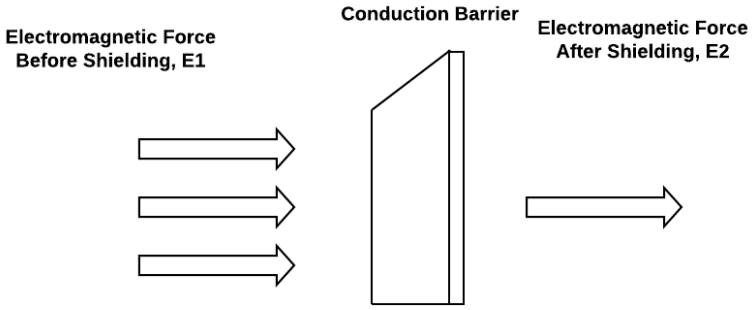


Figure 4. 3. electromagnetic shielding [38].

3. Soft Switching:

Mostly, due to capacitive coupling, large *di/dt* and large *dv/dt* will cause the conducted and radiated EMI according to electromagnetic compatibility. Because of large *dv/dt* and *di/dt* leads to high switching losses which cause the EMI too. In order to solve this problem, methods like snubbing systems and mostly soft switching are included [36] [41].

This method first came in the year 1990 and usage of this method increased in recent years. In order to reduce the EMI, the switching losses must be reduced. So, converters with on and off switching at zero voltage and current at high frequencies are alleviated. In other words, this switching also known to be resonant switching, quasi-resonant switching, multi resonant switching, zero current switching (ZCS), zero-voltage switching (ZVS), zero-current transition (ZCT), and zero-voltage transition (ZVT). In many fields, this method is applied with the pulse width modulation. Limitations for this method is soft switching can be done only for converters with power levels over 30W because it increases power losses for low power converters. And also, it needs auxiliary switches and diodes, resonant inductors and capacitors, which makes the design of switched mode converters more complicated [38].

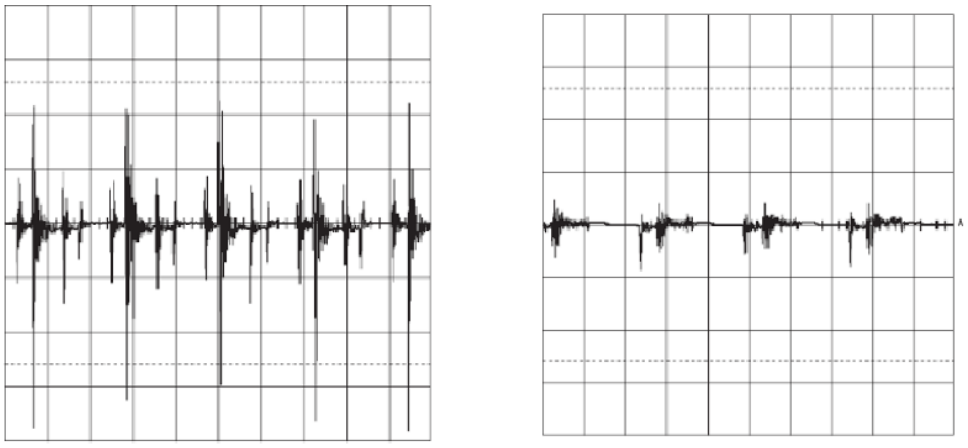


Figure 4. 4. power loss waveforms hard switching and soft switching difference for power MOSFETS in dc-dc converters (X-axis: Power Loss and Y-axis: Time) [36] [38].

4. Random Modulation:

This method is the new method in order to reduce the EMI recently over two decades. In this, for a given random signal there will be change in switching frequency. In periodic mode of converter, the peaks observed in the frequency band will smoothen the overall frequency band where the EMI suppressed with the help of reduced peaks. Generating real random signals are tough which is one of the disadvantages in this method and also random frequency makes the design of converter hard because the converter functions with the frequency. So, in order to calculate the equivalent inductance (2πfL) which depends on the frequency. To avoid this drawback in this method, pseudo- random signals are used to get real random signals. Here figure 4.5 shows the frequency spread for total energy [38] [42].

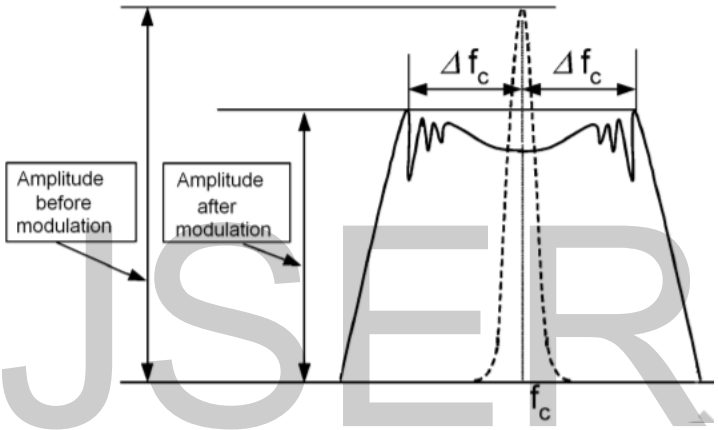


Figure 4. 5. spectrum of a frequency modulated sine signal following a sine modulation profile in time (initial frequency f_c and peak deviation Δf_c [38].

5. Damping Resistors:

In DC-DC converter, noise is caused by the ground bounce of the parasitic elements in the PCB and also because of the LC oscillations at the output. In order to reduce the noise which affects the output performance there will use of damping resistors in series with the capacitor as shown in figure below [43].

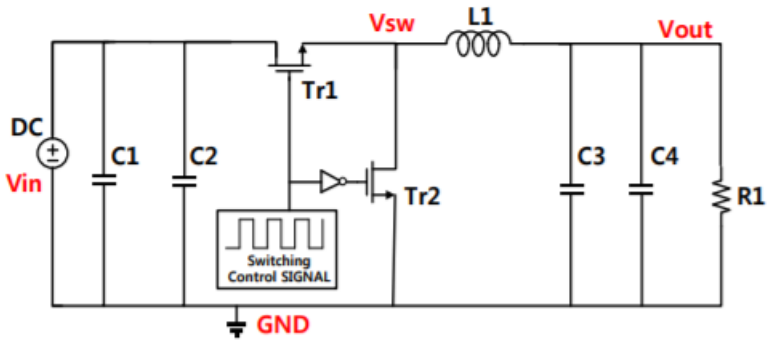


Figure 4. 6. typical converter [43].

Above figure 4.6, represents the synchronous buck converter where no parasitic elements are

considered then the results from this is shown in figure 4.7 how the output has the oscillations with respect of the input voltage.

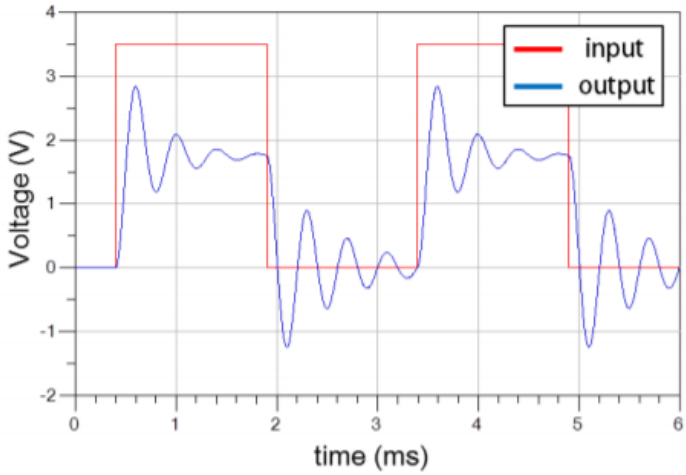


Figure 4. 7. input and output waveforms for typical converter [43].

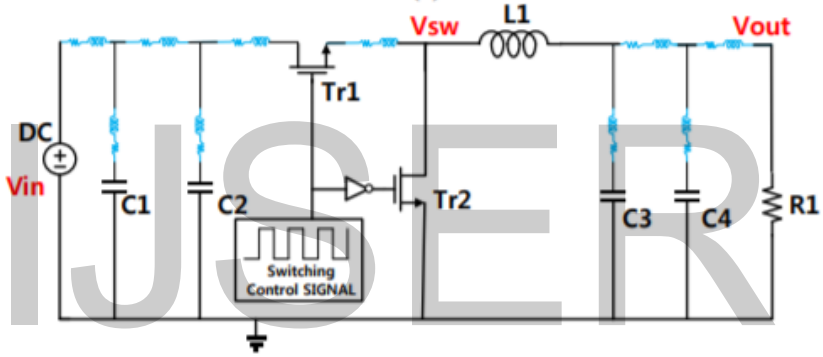


Figure 4. 8. converter with parasitic elements [43].

Figure 4.8 shows the converter with parasitic elements where the below waveforms shows the output voltage with the EMI for the taken input voltage.

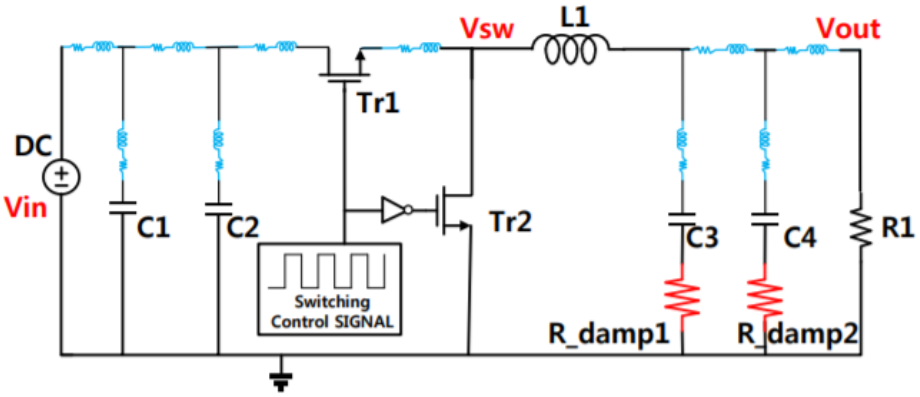


Figure 4. 9. Buck Converter with parasitic elements and damping resistor [43].

This damping resistor is calculated by the formulae given by as follows, [44]

$$Rdamp = 2\sqrt{(\frac{L}{C})}$$

After adding the damping resistance, there will be reduction EMI where below graphs show the example how the output voltage varies,

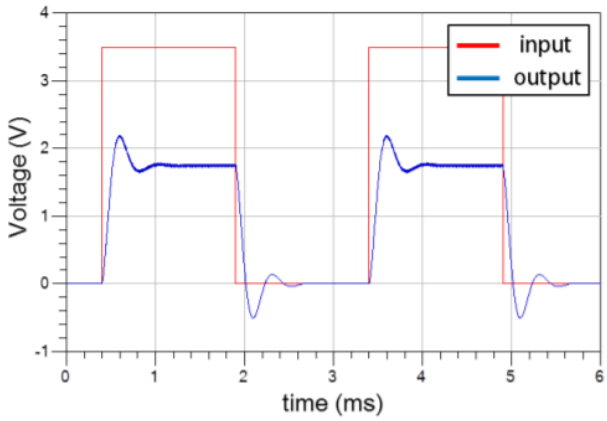


Figure 4. 10. without damping resistor [43].

From figure 4.10, there will be observation that for a given input voltage there will be oscillations caused due to LC.

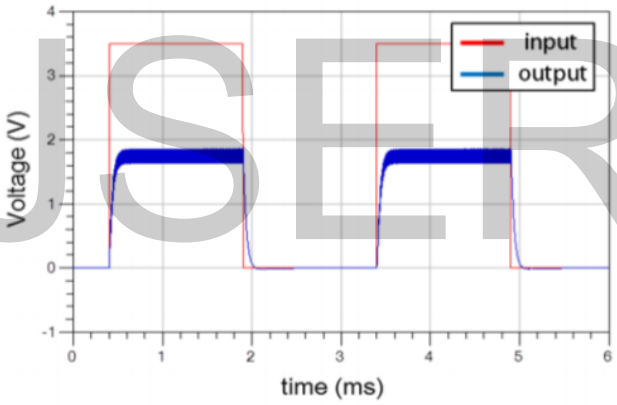


Figure 4. 11. with damping resistor [43].

After adding damping resistor, figure 4.11 shows how the spike(oscillations) are suppressed at the output voltage where noise will be reduced [45].

4.2 Chaos control

During initial conditions, there will be sensitive nature for a scientific and mathematical chaos to deterministic behavior where the chaos system as a random. There will be large oscillations at the start which is fundamental frequency as called as EMI. If the system operates in chaotic modes, there will be spread of peaks for entire frequency band which is known to be chaos modulation. This chaotic control is applied to dc-dc converters to drive the system which are non - linear. Control is done by modulating circuit parameters and other one as pulse width modulation control which is chaotic PWM control [36].

4.2.1 Chaotic parameter modulation:

Mostly chaos controls were implemented by the current mode control with parameter modulation. With this control, EMI can be suppressed. Normally, there will be large ripples in the output which can be reduced by using the peak current control mode of dc/dc converter for EMI reduction. In this method, parameter modulation is done by the control of magnitude of ripple which will also decrease the EMI. In this, switch is controlled with the clock period having reference current signal with i_{low} and i_{upp} where output ripple is controlled [38].

4.2.2 Chaotic PWM control:

In this control, there will be addition of external chaotic signals for dc/dc converters for more flexibility. Here chaotic carrier is implemented by the digital processor and ripple magnitude with the help of program. Here carrier plays major role for distribution of harmonics and this chaotic behavior will suppress the EMI. This chaotic PWM will be designed by changing carrier frequency or voltage. Ripples in output waveforms is controlled by the chaotic pulse width modulation by varying amplitude is more than the chaotic pulse width modulation carrier frequency. Spectra is unchanged even the current increases with ripples in the output waveforms but if the spectra are as per the electromagnetic compatibility standards then current is smaller in practice. So, in order to get chaotic PWM controls, need of control circuit should be more complicated than the traditional PWM control must be implement. With the help of integration technology, the control circuit should be integrated on the PCB or small chip [38].

Design of chaotic carrier will be done both analog or digital manner. Accurate signal is possible with the help of the digital chaotic carrier which is adjusted its frequency and amplitude easily with the help of digital processor programming without changing external interface circuit. Only, cons in this is digitally generated frequency is based on the speed if the digital signal processor (DSP) for chaotic carrier where there is the need of interface circuit, single chip and another digital processor which costs high for digital carrier signal. For analog chaotic carrier there will be broader frequency by changing the resistance and capacitance of the analog chaotic carrier where it costs less which is suitable for high frequency dc/dc converters. There will be numerous chaotic oscillators for designing analog chaotic carriers, but these cannot be adjusted better than the digital chaotic carriers because of non- ideal characteristics and also complex hardware implementation which are not identified during programming [36].

There will be high frequencies in the dc/dc converters where the chaotic carrier frequencies

has to be high. There will be some techniques like sawtooth map and different chaotic oscillators which helps to reduce EMI with low frequency band and chaotic carriers [36].

4.2.3 Chaotic soft switching PWM:

As know that the EMI in dc/dc converters is reduced with turn on and turn off the switch at zero current and zero voltage which alleviate the rate of change of the voltage and current by reducing the switching losses and EMI. Meanwhile by the chaotic control, there will be reduction of EMI by the spread of spectra of signals and the time series in the whole frequency. By the combination of soft switching and chaotic control suppress the EMI which is known to be soft chaotic switching PWM control for the dc/dc converters [38].

In conclusion, here chaotic control the system differently compared with the conventional methods. For accurate design of dc/dc converter parameters, there will be computational method. And there will be mean value estimation method which gives the state variables for chaotic PWM for designing and selecting of circuit components even though there are high ripples which are caused by chaotic carriers in dc/dc converters will reduce EMI under stable chaotic PWM control. This all above mentioned controls for EMI is helpful for the practical PWM dc/dc converters [38].

Estimation of EMI is done by the spectrum which is analyzed from the Fast Fourier Transform (FFT) but it is not applicable for the inner harmonics, non-integral multiples of the fundamental frequency for the chaotic signals. In order to estimate the chaotic spectra of dc/dc converters, Prony method is used. By this method, the frequencies, phases, amplitudes, and damping factors of the harmonics of currents or voltages are obtained for the dc/dc converters. The use of Prony method is better than the FFT for spectra analysis of converters with the involvement of chaotic signals [36] [46].

4.3 Some other techniques

4.3.1 Grounding:

Return path of current is grounding where closing the current loop but not earthing where diverting the EMI with the alternative path that is low impedance path from the victim. Therefore, diversion of interference current into ground is successful or it will return to the source. Improvement of EMI will depend on the good grounding for dc/dc converters. [36]

In PCB's, there will be modularization and integration of dc/dc converters with integration of more and more circuits in the PCB for EMI suppression increases the power density, decreases the size, weight and cost. [47] While designing PCB, conducted and radiated EMI should be considered [48] [49].

Other methods like using snubber resistor, gate resistor, boot resistor and integrated methods will also reduce the EMI [50].

5. Hardware Development of Converter in Buck Mode

In this chapter, discussion is based on the SiC based MOSFETs which is having advantageous properties than silicon. SiC MOSFETs are used for high voltage, high frequency and high temperature where the gate driving topology for SiC MOSFETs is different than the silicon MOSFETs [51]. SiC MOSFETs are too sensitive with parasitic capacitance, package inductance, and PCB power loop inductance. And the rate of change of voltage and current i.e switching transitions will create unwanted oscillations, overshoots and electromagnetic interference which impacts the overall system operation and reliability [52]. In order to improve the EMI and oscillations are by the change of gate resistance *Rg* [53].Switching losses will be reduced due to high value of gate resistance by acting as a damping resistance which makes increase *di/dt* and *dv/dt*. So *Rg* should be very selective in order to reduce the EMI and switching oscillations. So, a detailed discussion of driving mechanism for SiC MOSFET with two C3M0065090J in a phase leg configuration [54].

5.1 Factors that Effecting while driving SiC MOSFETs

5.1.1 Impact of gate resistance in switching noise and switching time:

Due to very fast switching transient, driving SiC MOSFET will cause the switching noise. The only solution is to select the appropriate value of gate resistance (*Rg*). If choosing of small value of gate resistance will provide a large peak current with very di/dt, dv/dt and low switching losses. Because of low gate resistance there will be EMI induction in the system. In order to reduce the EMI, high gate resistance should be selected but there will be the increase of switching losses. So, the gate resistance which is taken should be tradeoff with EMI and also gate resistance will act as a damper resistance in order to reduce oscillations [55]. The equivalent damping resistance during turn-on and turn-off with formulae are as follows:

$$\mathrm{Req(on)} = \mathrm{Rg} * \frac{(\omega \mathrm{onLd})^2}{(\mathrm{Rg})^2 + 1/\left(\omega \mathrm{onLG} + \omega \mathrm{onLs} - \left(\frac{1}{\omega \mathrm{onCiss}}\right)\right)^2} \quad (5.1.1)$$

$$Req(off) = Rg * \frac{\left(\omega offLs - \left(\frac{1}{\omega offCs}\right)\right)^2}{(Rg)^2 + \left(\frac{1}{\omega offLG} + \omega offLs - \frac{1}{\omega offCG} - \frac{1}{\omega offCs}\right)^2} \quad (5.1.2)$$

Where,

Req(on), Req(off) – Damping resistance during turn on and turn off

ωon, ωoff - resonating frequency during turn on and turn off

Ls, LG – parasitic inductance

Cs, CG – parasitic capacitance

The gate resistance during turn on and turn off will not be same where there will be *Rg(on)* as high and *Rg(off)* as low. Due to *Rg(off)* low there will quick turn off of the MOSFET. Below figure 5.1 shows the gate driver circuit with different gate resistance during turn on and turn off.

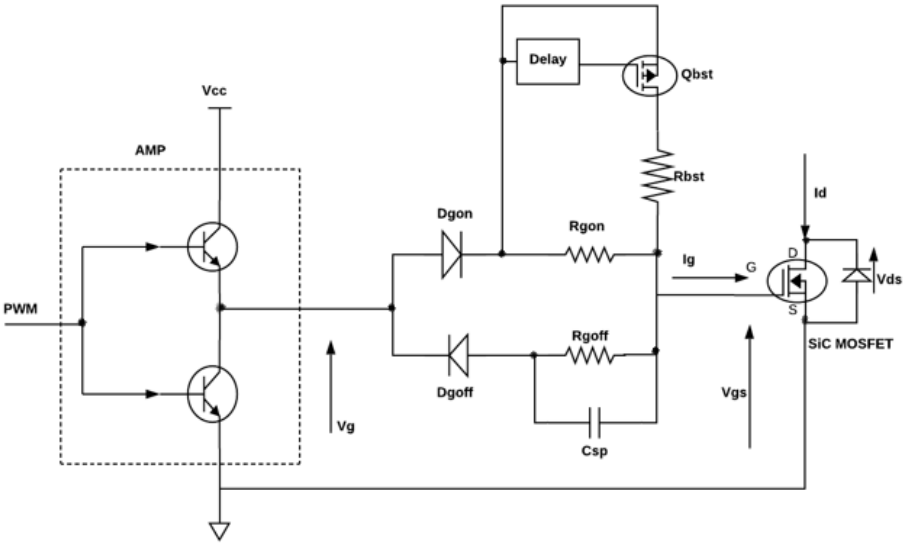


Figure 5. 1. gate boost circuit with separate *Rg(on)* and *Rg(off)* [52].

5.1.2 Effect on switching performance because of parasitic elements:

Due to high sensitivity nature of SiC MOSFETs, there will switching losses and poor waveform of di_d/dt, dV_{ds}/dt, and dV_{gs}/dt because of parasitic capacitance and inductance. Figure 5.2 shows the parasitic elements in the double pulse test [54].

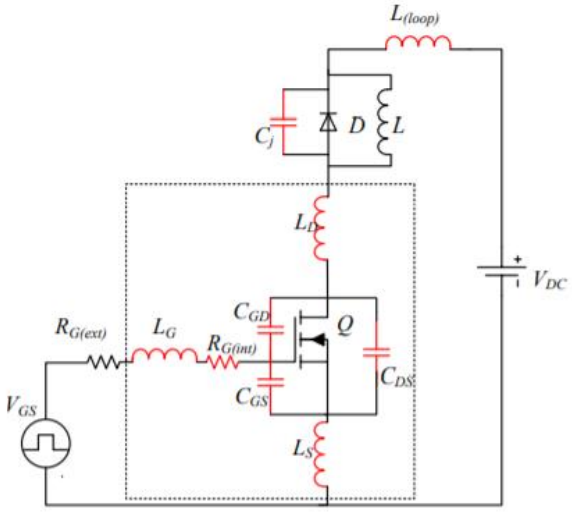


Figure 5. 2. inductive switching's with parasitic elements by double pulse test (DPT) [54].

During turn on transient, the MOSFET drain to source capacitance *Cds* is bypassed while diode's junction capacitance *Cj* is charging with the parasitic inductance *Lloop*, *Ls* and *Cj* are resonating at the frequency of *ωon*. During turn off, the MOSFET capacitance C_{DS} and C_{GD}

are resonating with frequency resonation of *ωoff*. Damping resistance as gate resistance during turn on and turn off. Below equation (5.2.1) and (5.2.2) represents the turn on and turn off formulae [56].

$$\omega on = \frac{1}{\sqrt{(Lloop+Ld+Ls)Cj}} \quad (5.2.1)$$

$$\omega off = \frac{1}{\sqrt{(Lloop+Ld+Ls)(CGD+CDS)}} \quad (5.2.2)$$

Figure 5.3 shows the prototype of the oscillations for *Vgs* and *Vds*. Figure shows the large loop and common source inductance because of the long loop wires which produces high turn on and turn off oscillations in both *Vgs* and *Vds* [54].

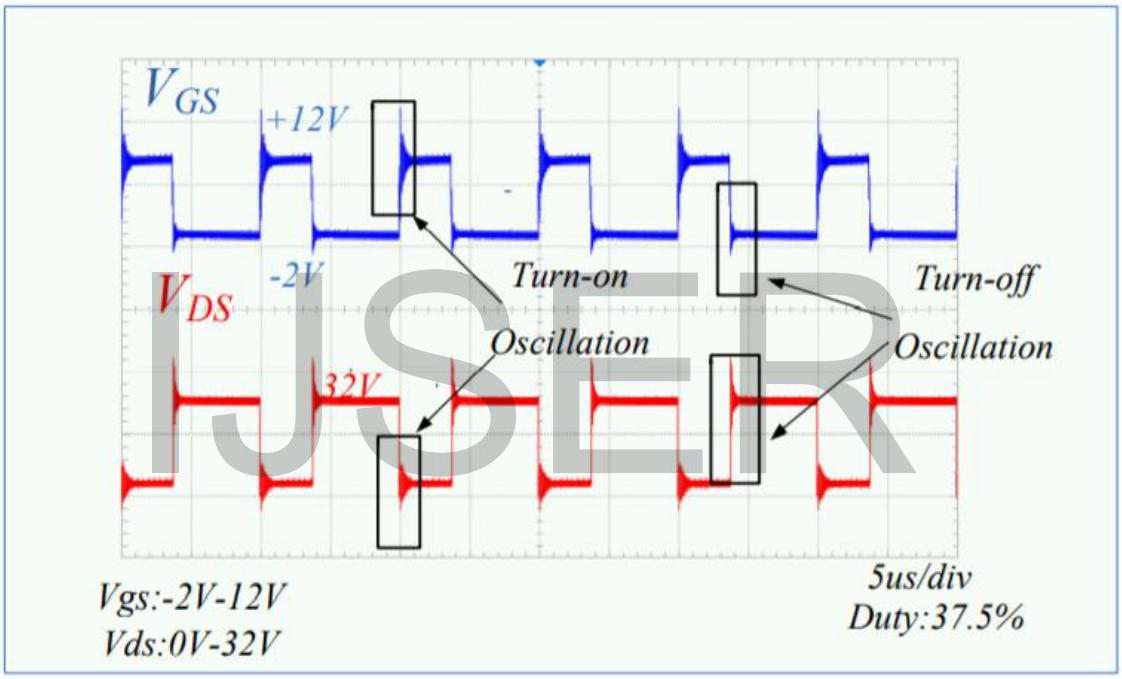


Figure 5. 3. gate voltage and drain voltage oscillations.

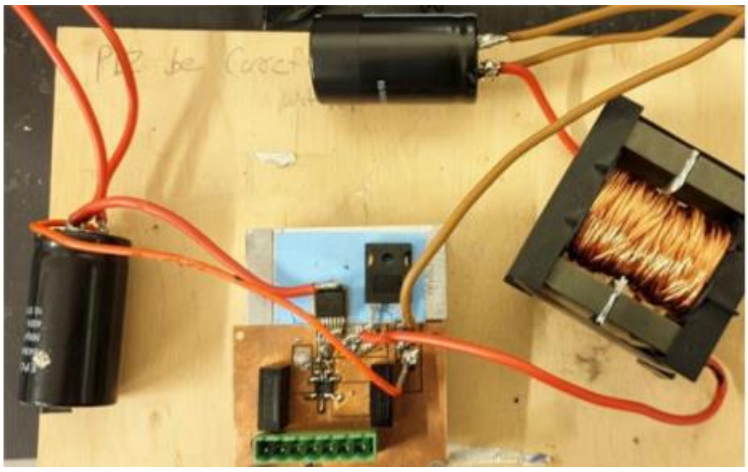


Figure 5. 4. physical setup of a buck regulator.

Switching losses are cause by the parasitic inductance. There are two different types of

parasitic inductances. One is power loop inductance *(Lloop)* which is created by the long traces of PCB layouts and packaging inductance and another one is common source inductance *(Ls)* which is mainly controlled by the packaging inductance [54]. There will be influence of power loop inductance and common source inductance on the buck voltage regulator which is explained in [57]. During turn on there will less impact on the negative feedback nature of the common source inductance and during turn off the negative voltage induced across the *Ls* will minus from the source voltage holding *Vgs* to *Vplateau* with increase in turn off time. So, turn on losses will be slightly increased and turn off losses will be greatly increased due to parasitic inductance. In conclusion, power loss will increase due to the parasitic loop inductance [54].

5.1.3 Effect of the crosstalk phenomenon:

Even though, switching converters have the good performance, there should be some attention while driving the SiC MOSFETs in a bridge configuration with the low threshold voltage leads to unwanted turn on. Figure 5.5 represents the crosstalk phenomenon of upper switch during turn on and turn off [54].

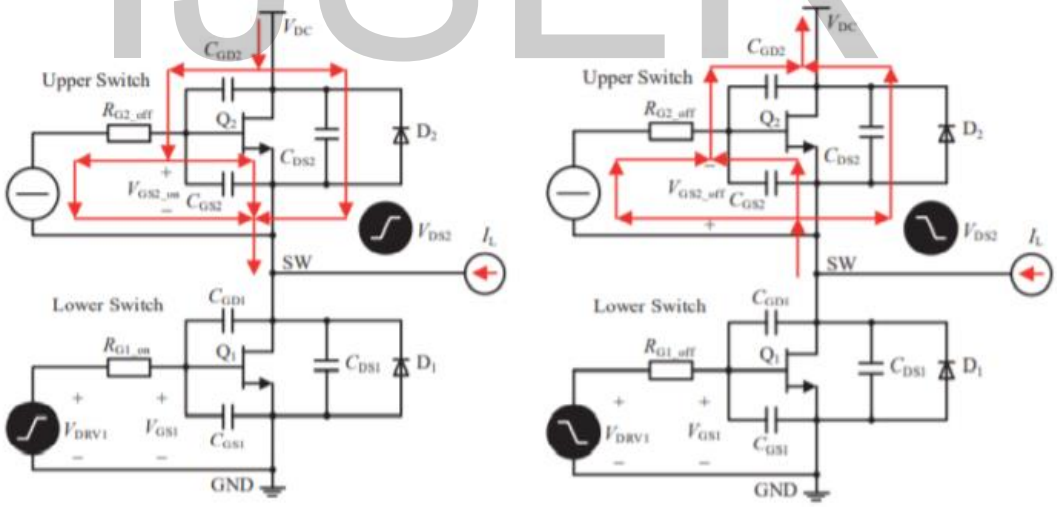


Figure 5. 5. (left) lower switch turn on and (right) upper switch turn off in a phase leg [58].

When lower switch is turned on, there will be high dV_{ds1}/dt which induces charging current in C_{GD2} where this charging current leads to voltage drop across $R_{g(off)}$. Upper switch will turn on only when overshoot of positive gate voltage is higher than the threshold voltage. Induced voltage formulae is given as [58]:

$$Vgs2(on), Vgs2(off) = Rg2(off).Cgd2.\left(\frac{Vm}{Tm}\right).\left(1 - e^{\left(-\frac{Tm}{Rg2(off)(Cgd2+Cgs2)}\right)}\right) \quad (5.3.1)$$

Where,

V_m = maximum voltage of drain to source voltage

T_m = voltage fall time

Accordingly, lower switch will turn off where negative voltage is induced at the gate terminal. But due to negative voltage there will be damage of MOSFET permanently. So, in order to avoid the unwanted turn on the optimal value of gate resistance is chosen. From equation, there will be increase of positive and gate voltage with turn off gate resistance. In conclusion, crosstalk can be prevented by selecting the low value of $R_{g2(off)}$. Additionally, extra gate to source capacitance in the upper switch will reduce the $V_{gs2(on)}$, $V_{gs2(off)}$ but it will slow down the turn on of an upper switch [54].

5.2 Design of a Gate Driver

For SiC MOSFETs, gate driver used is almost same as conventional driver where the components are soldering manually. In order to get the flexibility, here used the driving with different switching which can be possible with change of gate resistance, turn on voltage, turn off voltage and addition of additional input capacitors. The developed gate driver is optimized to drive Cree's C3M0065090J SiC MOSFET with 900V, 35A, 65mΩ on-state resistance [54].

5.2.1 Selecting Power Supply:

Here desired gate driving voltage is needed to power supply the gate driving circuit where this voltage is given by the manufacturer. Normally, turn on voltage is in between 18V-25V to get the minimum $R_{ds(on)}$ and meanwhile V_{gs} is -5V. For C3M0065090J will have the optimal value of -4/+18V. for good ΔVgs for MOSFET and IGBT, there will be usage of Recom's unregulated, high voltage isolation DC-DC converters. RP-1212 with single input and dual output chip for +15V and RP-1205S with single input single output for -5V with specifications are shown from table 5.1 below, [59]

Specifications:

Table 5. 1 parameters selection for driver circuit.

Parameters	RP-1212(turn on)	RP-1205S (turn off)
Input Voltage	12V	12V
Output Voltage	12/24V	5V
Output Current	+-42mA	+-200mA
Output Type	Dual	Single
Pin Count	5	4

Efficiency	82%	70%

5.2.2 Driver ICs selection:

Usually ΔVgs is given by the manufacturer. So, according to ΔVgs, selection of driver ICs will be done. For selecting driver ICs, there are things that should consider in order to get the correct design for the application.

Driver strength:

Driver's ability can be defined with help of source and sink driver current or in other word, how fast the MOSFETs input capacitance can be charged i.e, $C_{iss} = C_{gs}+C_{gd}$. In order to charge the gate capacitance, there is need to find out the gate current with the help of MOSFET gate charge, which is given as,

$$Ig = Qg.ton \tag{5.4.1}$$

As far as known, switching losses need to be reduced but for reduction of switching losses, high gate current is need where driver has to provide the peak gate current to charge the C_{iss} [54].

Propagation delay:

Due to large propagation delay, there will be switching losses. The mismatch of input signal rise to output signal rise and input signal fall to output signal fall is known as propagation delay or delay reached from 50% of input to 50% of output and this delay is considered to optimize the dead time. [54]

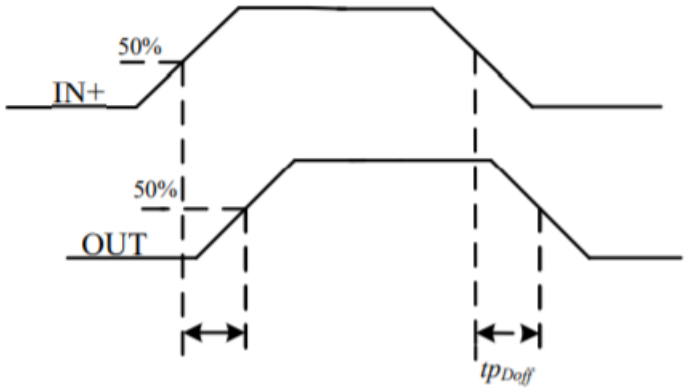


Figure 5. 6. input to output propagation delay.

Here dead time is needed in order to avoid both switches to operate simultaneously where the propagation delay will be less than dead time. And also more dead time will affect the efficiency i.e it will reduce and for gate driver low propagation delay is best [54].

Under Voltage Lockdown:

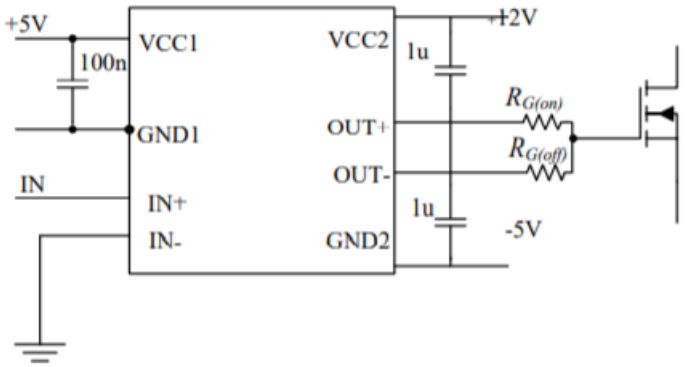


Figure 5. 7. driver pin diagram (1EDI60N12AF).

In order to make the gate driver circuit more advance, under voltage lockdown feature is there in the driver IC. V_{cc2} is given some certain value when positive gate driving voltage is given to V_{cc2} which locks the input signal until gate voltage set back to the desired gate voltage. If there is decrement of gate voltage will lead to the conduction losses in the MOSFET. This MOSFET, increases the $R_{ds}(on)$ having low gate voltage which decreases the gate current giving slow turn on mode and high turn on losses. In conclusion, conduction losses and switching losses will reduce with the help of high under voltage lockdown ratings. [54]

Different outputs for turn on and turn off:

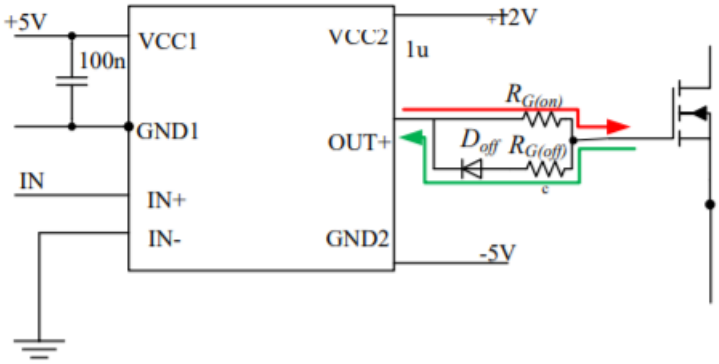


Figure 5. 8. Conventional gate driver with a single input and turn off diode.

In order to limit the switching speed and voltage overshoots, gate resistance is important parameter to drive the MOSFET. Normally, MOSFET turn on gate resistance $R_g(on)$ is more than the turn off gate resistance $R_g(off)$. So these gate turn on and turn off resistances are connected in parallel where turn off gate resistance is in series with diode. Usually gate drivers are with one output pin but some manufacturers provide different output pins for turn on and turn off. Here separate gate resistances used with no diode at turn on gate resistance.

From figure, two output pins for on and off gate resistors which makes driver design easy.

From above discussions, gate driver IC choose to drive two C3M0065090J SiC MOSFETs is Infineon's 1200V, 10/9.4A source-sink, separate-output pins, IEDI60N12AF IC [60]. This Infineon load all protective features which is designed in order to make gate drivers more convenient. The pin diagram is shown in figure and below table represents the specifications.

- Provided input-output voltage isolation up to 1200V which avoids the optocoupler in order to design the gate driver small in size and easier.
- Gate driver is capable with 10/9.4A source/sink current.
- One pin for gate turn on resistance and other pin for gate turn off resistance.
- Separate inverting (IN+) and non-inverting (IN-) pins for input PWM signals.
- Undervoltage lockdown with 10V.
- If output chip is not connected to the power supply, there should be active shutdown for MOSFET off-state.
- Short circuit clamping.

Driver specifications:

Table 5. 2 driver specifications.

Gate Driver Specifications	1EDI60N12AF(Infineon)
Peak Output Current (source/sink)	10A/9.4A
Supply Voltage Range at V_{cc2}	10-35V
Common mode transient immunity	100kV/us
Isolation Voltage	1200V
Propagation Delay (turn on and turn off)	120/125ns
Output rise time	10ns
Output fall time	9ns

From datasheet, passive components are selected, and design of gate driver is done from the above specifications. Below table 5.3 shows the gate resistance of turn on and turn off and the voltage.

Table 5. 3 on and off resistance, gate voltage parameters.

Rg(on)	10ohms
Rg(off)	10ohms
+VE gate voltage	+12V
-VE gate volatge	-2V

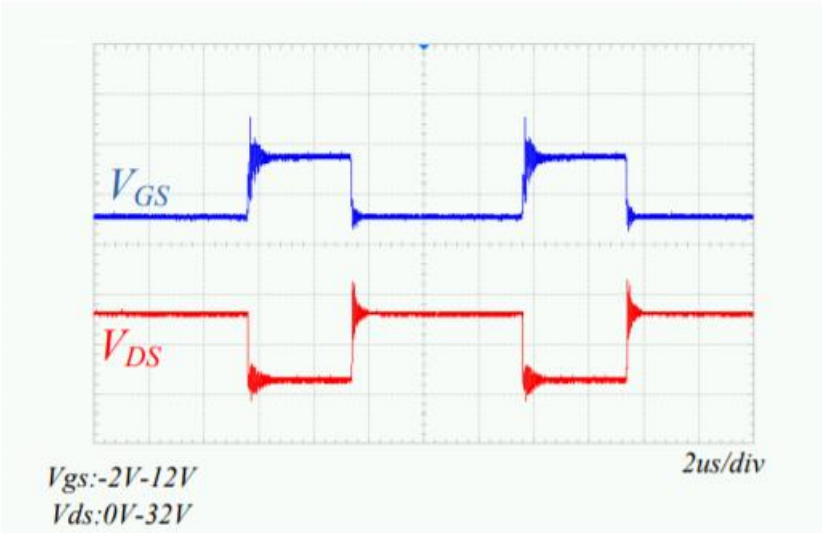


Figure 5. 9. V_{GS} at -2/12V and V_{DS} at 32V

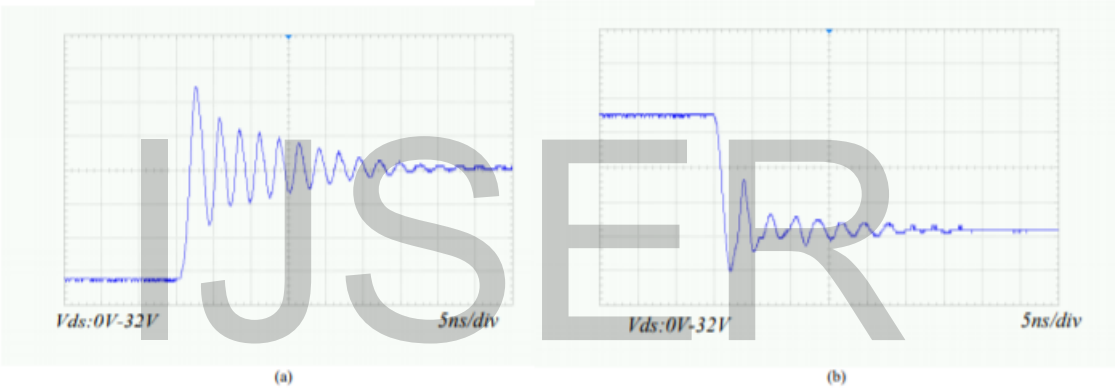


Figure 5. 10. V_{ds} with 32V and 37.5% duty cycle with turn on and turn off

Figure 5.10 shows the oscillations because of parasitic inductances which are caused due to use of long wires which is shown in Figure5.4. but these will be reduced by the PCB layout by ranging wires and parameters for short distance.

5.3 Experimental Results in Buck Mode

Experimental setup is done with the bidirectional converter where it can work for both buck and boost modes but my work is only to research and analyze the converter in buck mode where the PCB is manufactured from JLCPCB Co., limited in china. The driver circuit and power stage in done on the single board. Below figure 5.11 show the experimental setup and the laboratory equipment's for the experiment from the table 5.4.

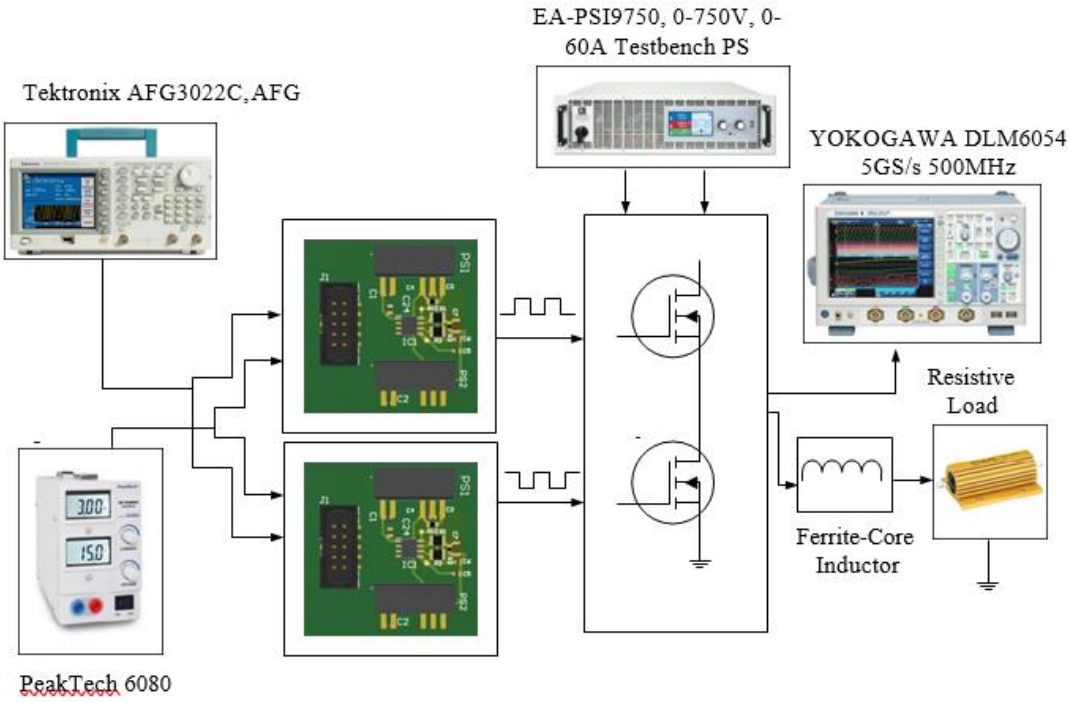


Figure 5. 11. Experimental setup

List of Laboratory Equipment's:

Table 5. 4 list of equipment's used for experimental setup.

Laboratory Elements	Description
High voltage Power Supply DC	EA-PSI9750, 0-750V, 0-60A Testbench PS: supplies power source to the converter.
Dual-Channel Function Generator	Tektronix AFG3022C: Used for initial dead time optimization to get complementary signal.
Signal Oscilloscope	YOKOGAWA DLM6054 5GS/s 500MHz:to get all waveforms from experimental prototype.
Lab Power supply	PeakTech 6080 DC PS(0-32V): used to power gate driver circuitry with low voltage power supply.
Variable Load Resistor	10A 7.5Ω variable resistor: load resistor for converter.
Three capacitors at high side and low side each	Each capacitor with 4.7µF with the total of 14µF at high side and with 0.33µF with total of 1µF which are DC film Type
Inductor	Having 180µH with ferrite magnetic core and E

	type core, 27 number of turns/windings, 1.6mm airgap, peak current of 12A, saturation flux density: 0.32mT.
AC Current Probe	PEM CWT AC Rogowaski Current Probe: used in order to get the inductor current ac component.
AC/DC Current Probe	Tektronix A622: for measurement of inductor current and dc output current.
AC/DC Current Probe	HENTEK-CC65: for measurement of inductor current and dc output current.
Differential probe	MICSIG DP10013: used to get drain-source voltage, gate-source voltage and output voltage.
Differential Probe	Tektronix P5200: used to get drain-source voltage, gate-source voltage and output voltage.

Figure 5.12 shows the waveform of the PWM and the gate to source voltage where the propagation delay is 125 ns. There should be dead time which is more than the propagation delay and this dead time helps to stop the operation of high side and low side switch to operate at the same time where in figure 5.13 shows the 150ns. From figure 5.13, it shows the gate-source voltage operating at 18V during turn on and with the -5V during turn off without applying any drain voltage. Figure 5.14 shows the PCB design in buck mode where it shows the total view of the converter and figure 5.15 shows the circuit with the inductor. So, from this setup, main observations are made that there is the oscillations due to parasitic elements when the drain-source voltage (V_{ds}) is low. The increase in the V_{ds} reduces the oscillations. Observations are made where the increase of gate voltage will cause the reduction of switching and conduction losses from the drain- source voltage and the drain current. And also from the specifications, normal dead time is 150ns from driver data sheet.

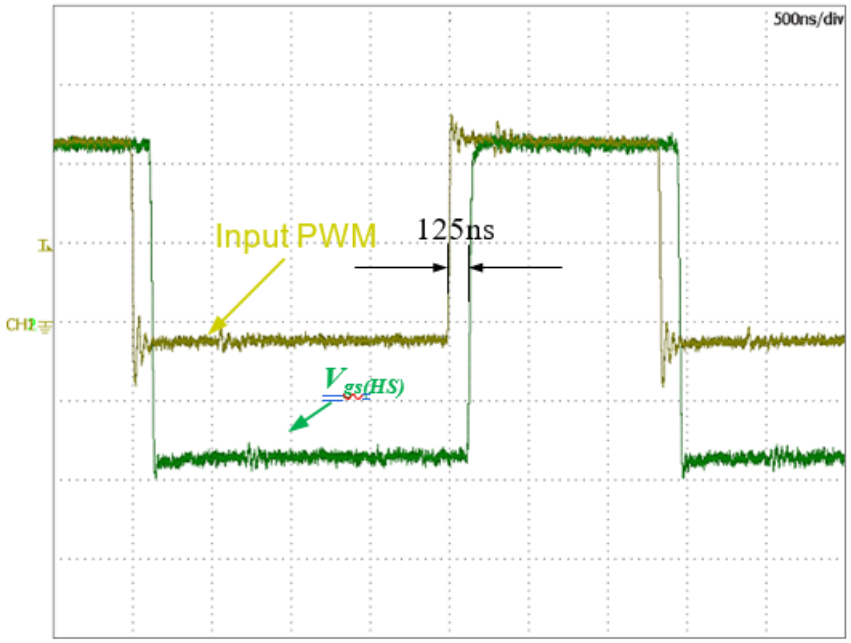


Figure 5. 12. waveform of input PWM and the V_{gs}(HS).

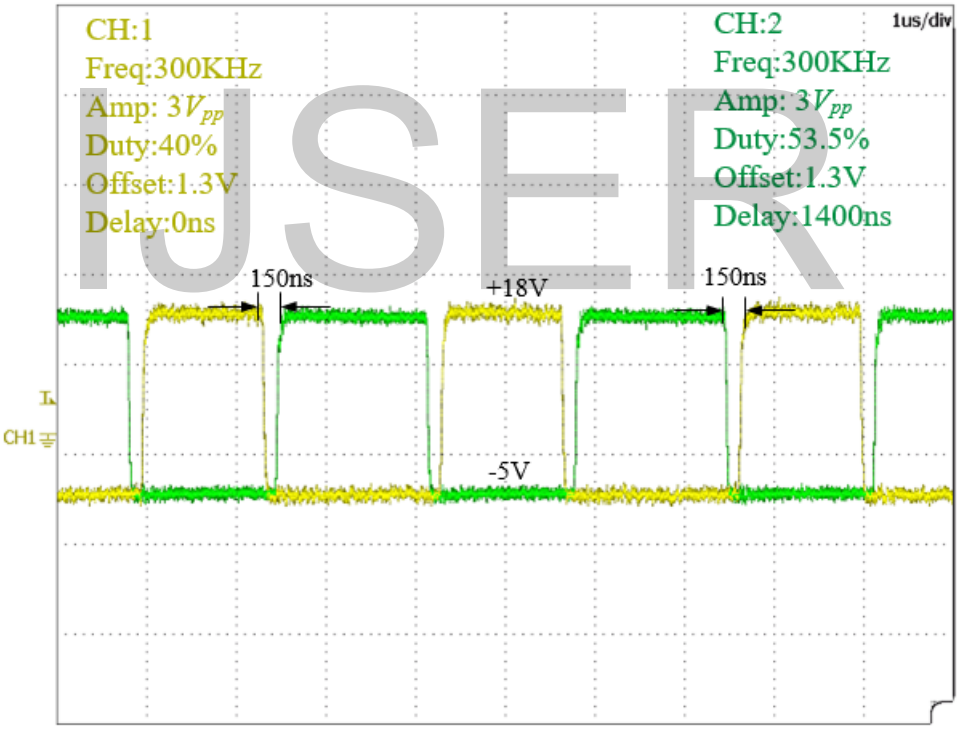


Figure 5. 13. dead time of 150ns for gate to source voltage (V_{gs}) without DC voltage.

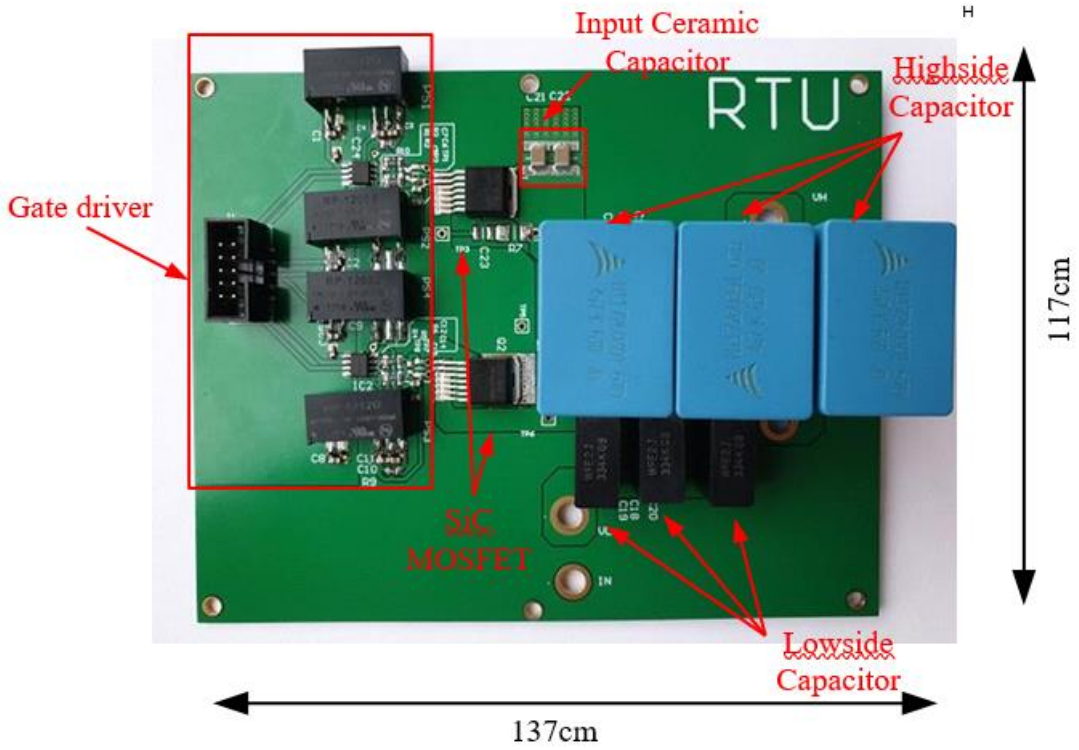


Figure 5. 14. PCB design of converter in Buck Mode.

Figure 5.14 shows the PCB design of the non-isolated bi-directional converter which is operating during the Buck mode where all components are highlighted and the figure 5.15 shows the converter with the inductor.

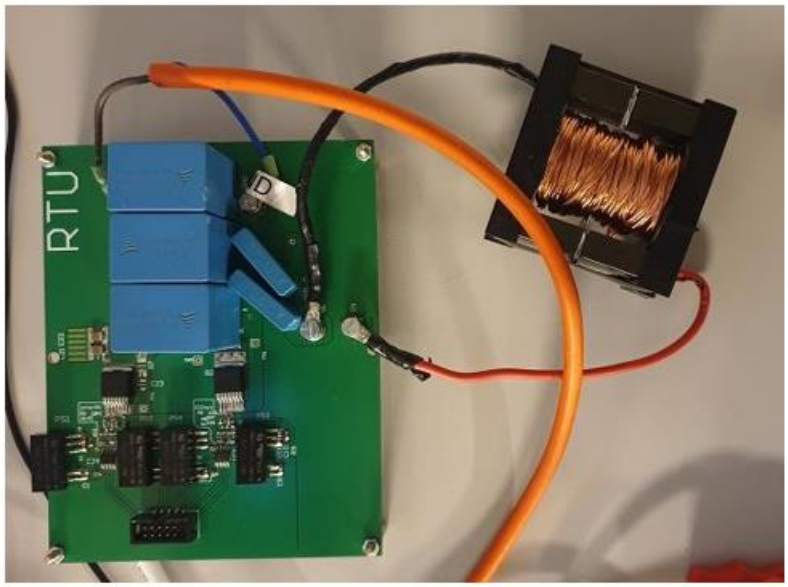
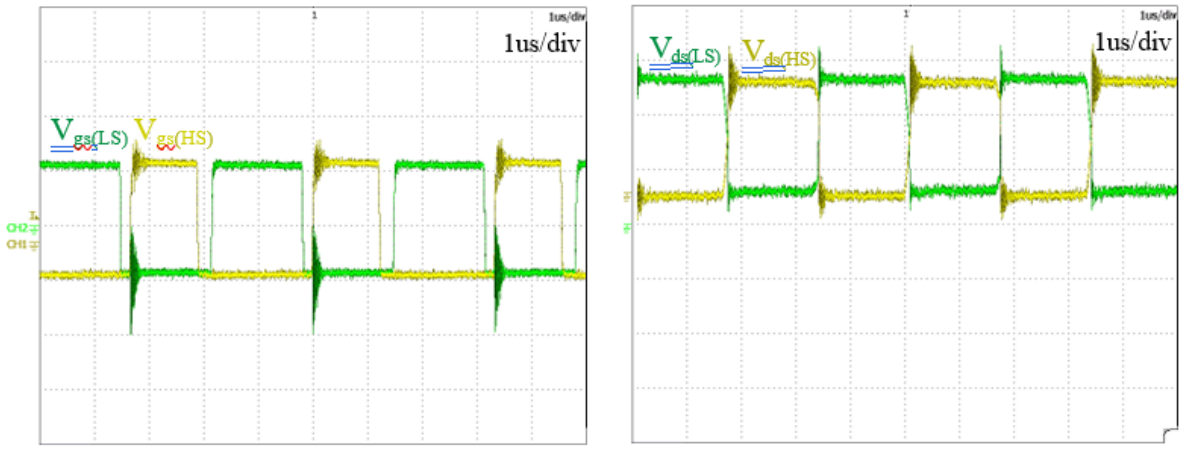


Figure 5. 15. PCB design of converter in Buck Mode with inductor.



(a) (b)

Figure 5. 16. (a) waveforms of gate to source voltage V_{gs} at high side (HS) and Low side (LS). (b) waveforms of drain to source voltage V_{ds} at high side (HS) and Low side (LS).

Figure 5.16 shows the gate to source voltage V_{gs} and the drain to source voltage V_{ds} for the dc voltage applied at 100V which shows the oscillations because of low voltage applied for the high rated (900V) SiC MOSFET.

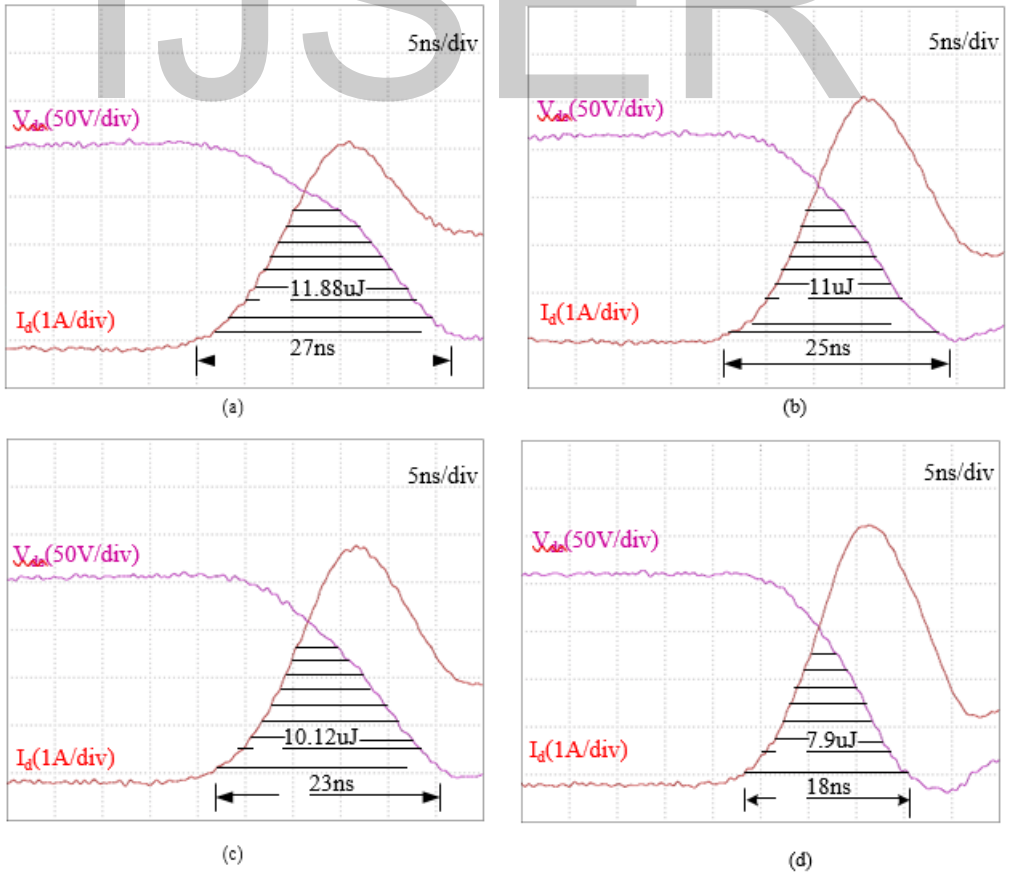


Figure 5. 17. (a) +12/-2V (b) +14/-3V (c) +16/-4V (d) +18/-5V for MOSFET during turn on.

Figure 5.17 shows the how the switching and conduction losses will be reduced by changing the gate voltage. Normally there is the chance of change in voltage up to 20V but will increases the stress. So, gate voltage is chosen as 18/-5V. from figure 5.17 there is reduction of switching time when the voltage is increased which helps to know that when the reduction of time lead to operate the switch faster with less energy and low conduction, switching losses where above figure operating at 200V, 3A.

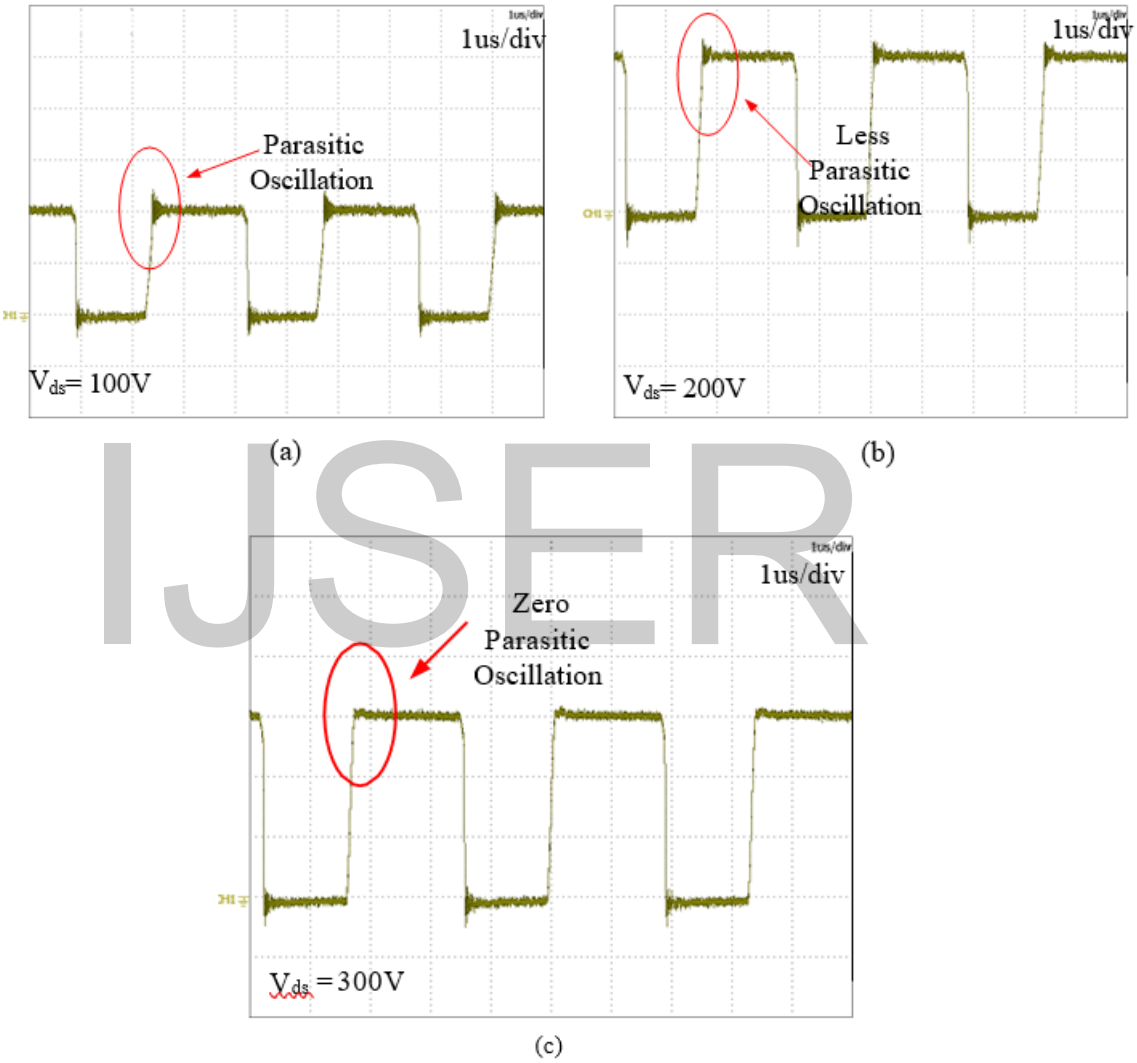


Figure 5. 18. (a) V_{ds} at 100V (b) V_{ds} at 200V and V_{ds} at 300V.

Figure 5.18 shows the oscillations reduction when the drain voltage is increased from 100V to 300V where it helps to learns that increase of drain voltage up to some extend will lead to reduction of the oscillations.

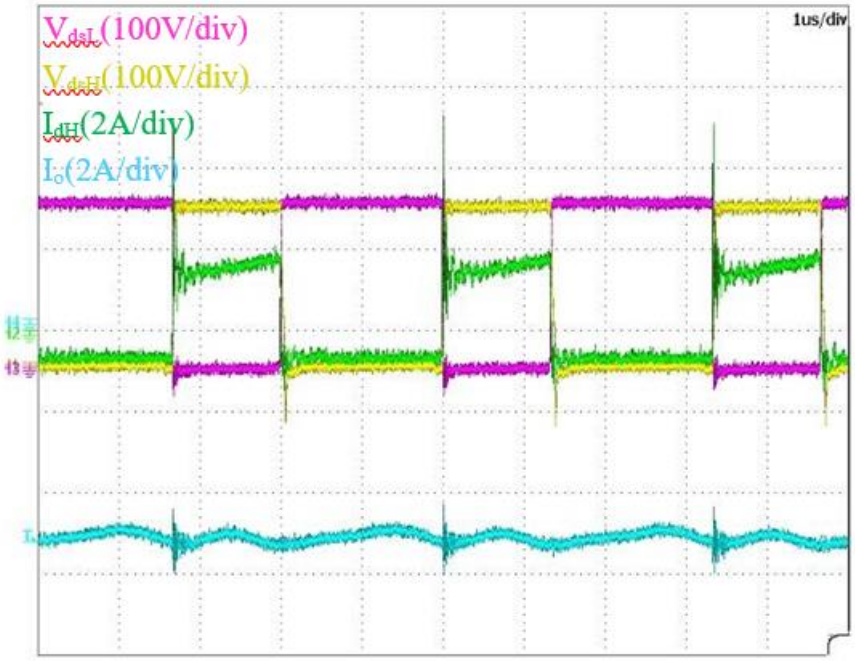


Figure 5. 19. Buck Mode waveforms.

Figure 5.18 shows the results of Buck converter operated with a frequency of 300kHz having high temperature coefficient of 65º for a SiC MOSFET where channel1(CH1) gives the drain to source voltage V_{ds} at high side of 200V for a duty cycle of 40%, channel2(CH2) gives the drain current of 1.8A, channel3(CH3) with V_{ds} at low side 200V and channel4 (CH4) with output current of 4.5A which gives the power of 341.1W for output voltage of 75.8V practically instead of 360W and 80V due to losses. So, efficiency is calculated as,

$$Efficiency(\eta) = \frac{output\ power}{input\ Power}$$

$$\eta = \frac{VoIo}{VdsId} = \frac{75.8 * 4.5}{200 * 1.8} = \frac{341.1}{360}$$

$$\eta = 94.75\%$$

but this converter is used up to power range of 1.5kW range but due to temperature changes and EMI effect leads for the damage of SiC MOSFET for high power range.

CONCLUSION

The Buck converter is developed by using the voltage mode and current mode control systems with variable converter input voltage (120-150V) and variable Resistive load of the converter (10-40ohms) for a constant converter output voltage (54V) using MATLAB Software which is idealized topologies in order to use for energy storage system applications and in power system according to system specifications. Normally, basic buck converter is explained which is compared with the synchronous buck converter due to low conduction losses, less voltage drops across the low side MOSFET(Q2) (shown in figure2.7.) than using the diode and less cost from study. The reason of explaining both voltage and current mode control systems for synchronous buck converter is to show the comparison and effectiveness of the current mode control system which gives the accurate output voltage with less oscillations than the voltage mode control system.

Usually in voltage mode control system, the output voltage is compared with the reference voltage by tuning PI controller where the tuned value is compared with the sawtooth signal in order to get the pulse width modulation of signal which is given to the gate of MOSFET but in current mode control system, both output voltage and inductor current are compared with their respective reference values which give pulse to gate by PWM technique where there is reduction of oscillations and accurate output is achieved than the voltage mode control system.

Applications of battery storage and hybrid storage systems are explained in order to know the use of synchronous buck converter. Mainly, there is the electromagnetic interference (EMI) problem in converters which lead to the reduction of output power and gives the losses. So, in order to reduce this problem, study is done by explaining the different methods for the EMI reduction. Various conventional, chaos control methods, grounding are studied. Using damping resistors in series with output capacitor will also help to reduce the EMI.

Finally, hardware setup is made by using the non-isolated bidirectional converter where it could be called as synchronous buck converter when it is operated in buck mode. The SiC MOSFET as an active switch in buck mode is used which have wide band gap semiconductor properties. In this, driving voltage of 18/-5V is given to the gate of high side and low side MOSFETs which are operated like when high side switch is on while low side switch is off and vice versa. Observations are made that how the conduction and switching losses are reduced by increasing the gate voltage up to desired value and reduction of parasitic oscillations with the increment of drain to source voltage (V_{ds}). Then the results from the

experimental hardware setup for converter in buck mode is achieved with the efficiency of 94.75% for input converter voltage as 200V and the output converter voltage as 75.8V having output power of 341.1W. In future, this buck converter can achieve high efficiency with increase in power if the design of converter is done by using the EMI reduction method like soft switching instead of hard switching.

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