DESIGN OF HIGH RESOLUTION ADC USING MICRON TECHNOLOGY

ABSTRACT

Analog-to-digital converters (ADCs) are key design blocks and are currently adopted in many application fields to improve digital systems, which achieve superior performances with respect to analog solutions. With the fast advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. Wide spread usage confers great importance to the design activities, which nowadays largely contributes to the production cost in integrated circuit devices (ICs). This has recently generated a great demand for low-power, low-voltage ADCs that can be realized in a mainstream deep-submicron CMOS technology. Various examples of ADC applications can be found in data acquisition systems, measurement systems and digital communication systems also imaging, instrumentation systems. Hence, we have to considered all the parameters and improving the associated performance may significantly reduce the industrial cost of an ADC manufacturing process and improved the resolution and design specially power consumption .

The ADC designed is carried out by designing each building block of the circuit separately and then assembling them together to get

the required ADC. The CMOS comparator, the digital to analog converter (DAC) and the successive approximation register (SAR) are the key elements in the design of the ADC. The CMOS operational amplifier was designed with a high unity gain frequency that will direct the ADC to operate at a greater speed. Design has been carried out in Tanner EDA tools.

We have designed, fabricated and tested the second-generation (2G) design of a high-resolution, dynamically programmable analog-to-digital converter (ADC) for radar and communications applications. The ADC chip uses the phase modulation–demodulation architecture and on-chip digital filtering.

The 2G ADC design has been substantially enhanced. Both ADC front-end modulator and demodulator, as well as decimation digital filter, have been redesigned for operation at 20 GHz. Test results of this 6000 Josephson junction 2G ADC chip at clock frequencies up to 19.6 GHz are described.

There are many different types of ADC structures, one of these is the Pipelined ADC, which is characterised by having relative high speed, with a low area- and power consumption.

The pipelined ADC design was achieved by initially analysing the di®erent options regarding the overall structure. The 1.5-bit stage

resolution is chosen in order to accommodate the speed requirements. The ¯nal overall structure is with 8 1.5-bit stages and one 2-bit stage, so that digital error correction can be applied. Further analysis of the structure of the stage structure concluded that an redesign of the traditional structure into a subADC/MDAC structure would be advantages. Generally the design is fully differential in order to compensate for offset errors and other limitations.

As technology scales, the improved speed and energy efficiency make the successive-approximation-register (SAR) architecture an attractive alternative for applications that require high-speed and high-accuracy analog-to-digital converters (ADCs). In SAR ADCs, the key linearity and speed limiting factors are capacitor mismatch and incomplete digital-to-analog converter (DAC)/reference voltage settling. In this thesis, a sub-radix-2 SAR ADC is presented with several new contributions. The main contributions include investigation of using digital error correction (redundancy) in SAR ADCs for dynamic error correction and speed improvement, development of two new calibration algorithms to digitally correct for manufacturing mismatches, design of new architecture to incorporate redundancy within the architecture itself while achieving 94% better energy efficiency compared to conventional switching algorithm, development of a new capacitor DAC structure

to improve the SNR by four times with improved matching, joint design of the analog and digital circuits to create an asynchronous platform in order to reach the targeted performance, and analysis of key circuit blocks to enable the design to meet noise, power and timing requirements.

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CHAPTER – 1

INTRODUCTION

Analog-to-digital converters (ADCs) are important building blocks in many electronic applications. Various architectures — folding, subranging and pipeline — have been used to deliver these high-speed, medium-resolution ADCs. Of these, pipeline architecture has proven to be the most efficient for applications such as digital communication systems, data acquisition systems and video systems. Especially, power dissipation is a primary concern in applications requiring portability. Thus, the objective of this work is to design and build a low-voltage low-power medium-resolution (8-10bits) high-speed pipeline ADC in deep submicron CMOS technology.

The non-idealities of the circuit realization are carefully investigated in order to identify the circuit requirements for a low power circuit design of a pipeline ADC. The resolution per stage plays an important role in determining overall power dissipation of a pipeline ADC. The pros and cons of both large and small number of bits per-stage are examined. A power optimization algorithm was developed to assist in determining whether a large or a small number of bits per stage performs best. Approaches using both an

identical and non-identical numbers of bit per-stage were considered and their differences analyzed.

A low-power, low-voltage 10-bit 100Msamples/s pipeline ADC was designed and implemented in a 0.18µm CMOS process. Its power consumption was minimized through proper selection of the per-stage resolutions based on the result of the power optimization algorithm and by scaling down the sampling capacitor size in subsequent stages.

Over the past two decades, silicon integrated circuit (IC) technology has evolved so much and so quickly that the number of transistors per square millimeter has almost doubled in every eighteen months. Since the minimum channel length of transistors has been shrunk, transistors have also become faster. The evolution of IC technology has been driven mostly by the industry in digital circuits such as microprocessors and memories. As IC fabrication technology has advanced, more analog signal processing functions have been replaced by digital blocks. Despite this trend, analog-to-digital converters (ADCs) retain an important role in most modern electronic systems because most signals of interest are analog in nature and must to be converted to digital signals for further signal processing in the digital domain.

In telecommunication systems, the goal of this trend toward digitalization is to move ADCs close to the antennas so that all the analog functions such as mixing, filtering and demodulating, can be implemented in the digital domain. Thus, one radio system can handle multiple standards by simply changing the programs in the digital signal processing block. This concept is known as software-defined radio. Recently, a cognitive radio, based on a concept similar to software-defined radio, is getting attention due to the its ability to adapt to the environment. Because of these trends and rapidly growing wireless digital communication market, ADCs with higher sampling rates and linearity are in high demand. However, since ADCs with a higher sampling rate are often designed solely for maximum speed, they tend to consume significant amount of power as shown in Figure 1. Consequently, the demand for increased functionality of high-speed ADCs also carries with it a need for these improved ADCs to have low power dissipation.

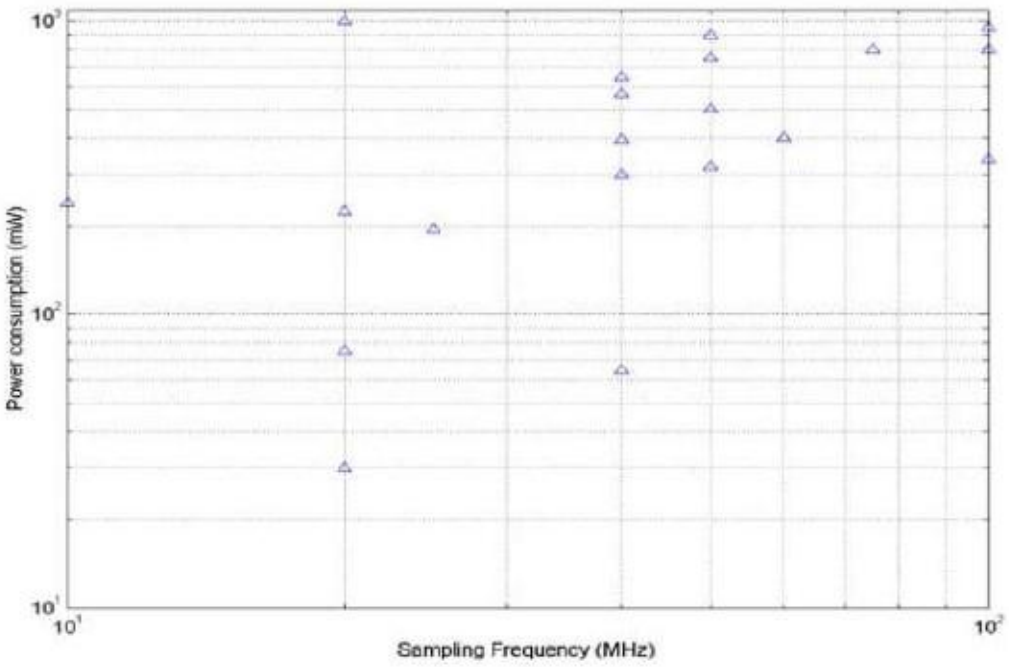


Figure 1: Power versus sampling rate for 10-bit ADCs.

Another trend is toward higher-level circuit integration, which is the result of demand for lower cost and smaller feature size. The goal of this trend is to have a single-chip solution, in which analog and digital circuits are placed on the same die with advanced CMOS technology. Although advanced fabrication technology benefits digital circuits, it poses great challenges for analog circuits. For instance, the scaling of CMOS devices degrades important analog performance such as output resistance, lowering amplifier gain. Cascading transistors or an added gain stage can compensate for this lowered gain. However, the use of cascading transistors runs into a limitation on the number of transistors that

can be stacked, a limitation that is imposed by the low power supply voltage of scaled CMOS technology. And turning to the solution of additional stages has the disadvantages of increased power dissipation and more complicated circuitry. The low power supply voltage of scaled CMOS technology also limits the performance of analog circuits.

The various ADC architectures available include flash, two-step, folding, pipeline, successive approximation, and over-sampling. Each variation has unique features and which of them is deployed in specific applications is typically determined by the speed and resolution requirements involved.

There is wide variety of different ADC architectures available depending on the requirements of the application. Pipeline ADCs are one of the best examples. Pipeline analog–to-digital converters (Pipeline ADC) have recently become very attractive in energy efficient moderate-resolution/moderate-speed applications due to their minimal active analog circuit requirements. It typically generate one bit per clock cycle, the benefits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size. The pipeline

analog-to-digital converter (ADC) is a promising topology for high-speed data conversion with compact area and efficient power dissipation. Its speed of operation far surpasses that of serial-based structures, such as successive approximation or cyclic converters, while its die area and power dissipation favorably compare to that of flash and other more parallelized architectures. Pipelined ADCs are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, studio cameras, ultrasound monitors, and many other high speed applications. Pipeline analog-to-digital converters (ADCS) represent the majority of the ADC market for medium-to high-resolution ADCS. Pipeline ADCS provide up to 5Msps sampling rates with resolutions from 8 to 18 bits. The Pipeline ADC architecture allows for high performance, low power ADCS to be packaged in small form factors for today's applications. With ADC we have designed 4 bit low power high speed Pipeline ADC with 0.18µm technology.

The contribution of signal processing as one of the major motivation to the fast development of electronic circuits is always worth mentioning. With the incredible advancement of modern VLSI technology, people are able to build more and more complex digital circuits on a single chip to realize signal processing that is traditionally achieved by analog circuits, because digital circuit has

advantages over its analog counterpart in several aspects such as much lower noise sensitivity, excellent signal regenerating capability and it is easier to realize design and test automation as well.

However, the object of signal processing originates in the fact that physical signals of the real world are always in analog form. Therefore, to facilitate the extensive DSP functions in the digital domain, interfaces between analog and digital blocks are omnipresent in all contemporary mixed signal processing integrated circuits. Analog to digital data converters are among the major components in the interfaces. Today"s trend in mixed-signal ASICs leads to integration of Analog-Digital-Converters (ADCs) with complex digital circuitry on a single chip. ADCs are a key element in mixed-signal ICs.

Wide applications such as wireless communications and digital audio and video have created the need for cost-effective data converters that will achieve higher speed and resolution. The needs required by digital signal processors continually challenge analog designers to improve and develop new ADC and DAC architectures.

Basically, the successive-approximation A/D converter, which is known for its very good power efficiency, consists of three main

components-an analog comparator, a DAC, and a successive-approximation register (SAR), all of which are connected in a feedback arrangement as shown in Figure2. A more complete converter contains additional control logic for the CLOCK, CLEAR and START signals, and perhaps a set of data latches for the output bits. Because the SAR is the only digital network of the three, it has been one of the limiting factors in prior attempts to fabricate costcompetitive monolithic successive-approximation A/D converters since both analog and digital networks could not successfully be built on the same chip. Consequently, earlier attempts at a single-chip converter employed a dual-chip approach keeping the analog and digital portions of the converter on separate monolithic chips and then connecting on a single hybrid substrate.

The work starts with designing a high frequency low power operational amplifier (OPAMP). An OPAMP is a DCcoupled high-gain electronic voltage amplifier with a differential input and, usually, a single-ended output. An op-amp produces an output voltage that is typically hundreds of thousands times larger than the voltage difference between its input terminals. OPAMPs are key elements in analog processing systems. Operational amplifier is the main bottleneck in our circuit. As shown in the figure 2, we need one DAC and Comparator circuit. OPAMP based DAC and comparator is implemented in the design of the analog to digital

converter circuit. So design of high frequency low power OPAMP is the building block of the ADC circuit.

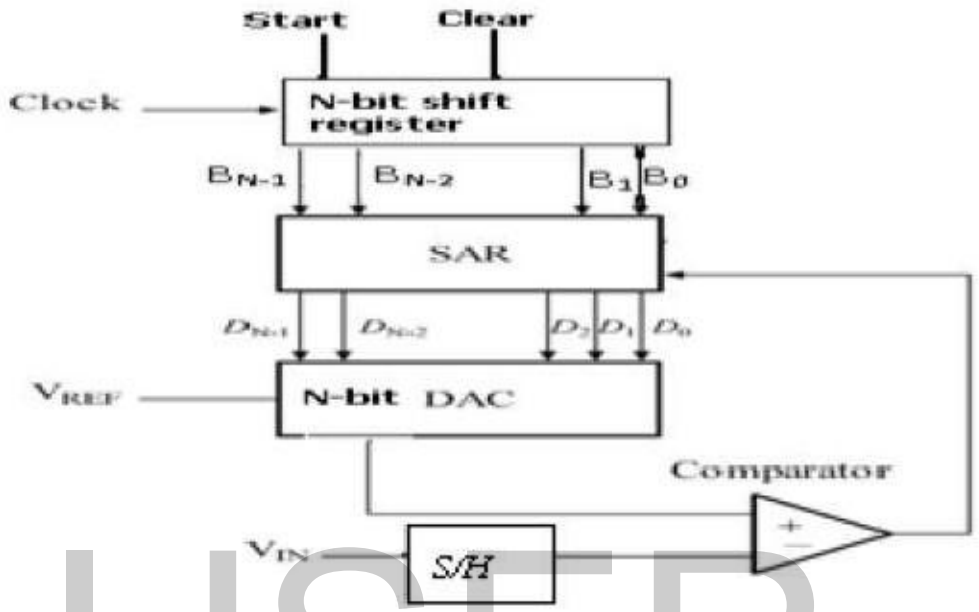


Figure 2: Successive approximation ADC block diagram

ANALOG-TO-DIGITAL CONVERTER ARCHITECTURES

The basic ADC function is shown in Figure 3. This could also be referred to as a quantizer. Most ADC chips also include some of the support circuitry, such as clock oscillator for the sampling clock, reference (REF), the sample and hold function, and output data latches. In addition to these basic functions, some ADCs have additional circuitry built in. These functions could include multiplexers, sequencers, auto-calibration circuits, programmable gain amplifiers (PGAs), etc.

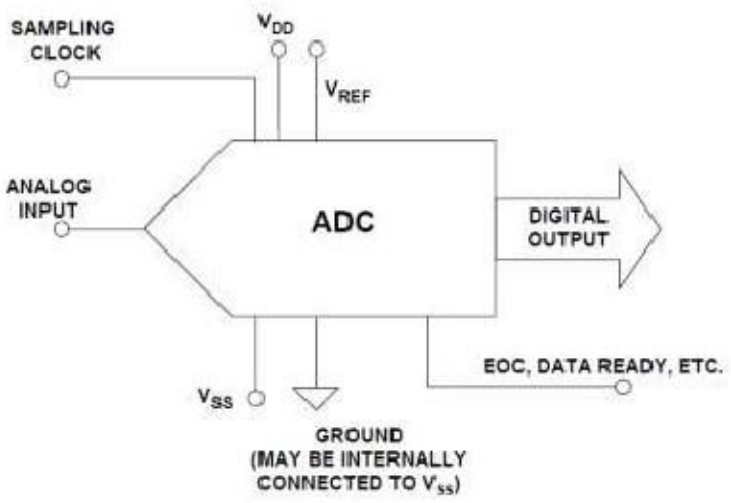


Figure 3: Basic ADC Function.

Similar to DACs, some ADCs use external references and have a reference input terminal, while others have an output from an internal reference. In some instances, the ADC may have an internal reference that is pinned out through a resistor. This connection allows the reference to be filtered (using the internal R and an external C) or by allowing the internal reference to be overdriven by an external reference. The AD789X family of parts is an example of ADC that use this type of connection. The simplest ADCs, of course, have neither—the reference is on the ADC chip and has no external connections.

If an ADC has an internal reference, its overall accuracy is specified when using that reference. If such an ADC is used with a perfectly accurate external reference, its absolute accuracy may actually be

worse than when it is operated with its own internal reference. This is because it is trimmed for absolute accuracy when working with its own actual reference voltage, not with the nominal value. Twenty years ago it was common for converter references to have accuracies as poor as ±5% since these references were trimmed for low temperature coefficient rather than absolute accuracy, and the inaccuracy of the reference was compensated in the gain trim of the ADC itself. Today the problem is much less severe, but it is still important to check for possible loss of absolute accuracy when using an external reference with an ADC which has a built-in one.

ADCs which have reference terminals must, of course, specify their behavior and parameters. If there is a reference input the first specification will be the reference input voltage—and of course this has two values, the absolute maximum rating, and the range of voltages over which the ADC performs correctly.

Most ADCs require that their reference voltage is within quite a narrow range whose maximum value is less than or equal to the ADC's VDD. The reference input terminal of an ADC may be buffered as shown in Figure 4, in which case it has input impedance (usually high) and bias current (usually low) specifications, or it may connect directly to the ADC. In either case, the transient currents developed on the reference input due to the

internal conversion process need good decoupling with external low inductance capacitors. Good ADC data sheets recommend appropriate decoupling networks.

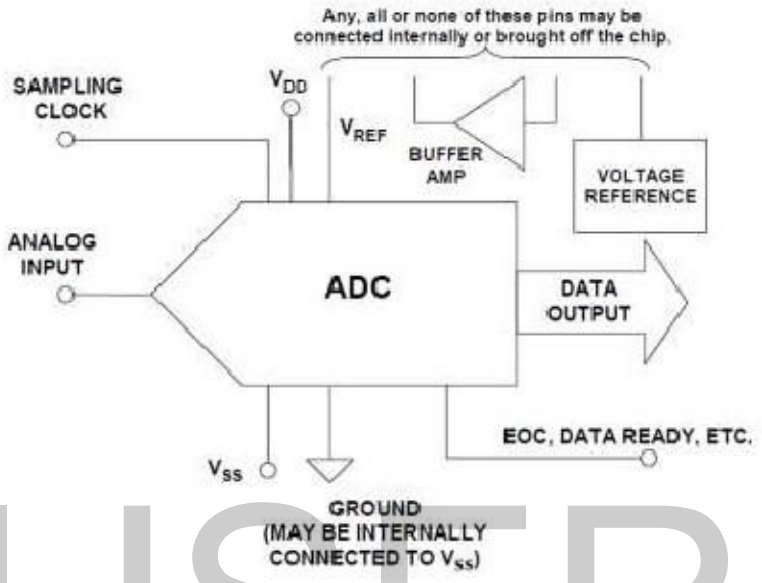


Figure 4: ADC with Reference and Buffer.

The reference output may be buffered or unbuffered. If it is buffered, the maximum output current will probably be specified. In general such a buffer will have a unidirectional output stage which sources current but does not allow current to flow into the output terminal. If the buffer does have a push-pull output stage (not as common), the output current will probably be defined as ±(SOME VALUE) mA. If the reference output is unbuffered, the output impedance may be specified, or the data sheet may simply advise the use of a high input impedance external buffer.

There are some instances where the power supply is the reference. In these cases it is imperative to make sure the power supply is clean. The sampling clock input is a critical function in an ADC and a source of some confusion. It could truly be the sampling clock. This frequency would typically be several times higher than the sampling rate of the converter. It could also be a convert start (or encode) command which would happen once per conversion. Pipeline architecture devices and sigma delta (Σ-Δ) converters are continuously converting and have no convert start command.

Regardless of the ADC, it is extremely important to read the data sheet and determine exactly what the external clock requirements are, because they can vary widely from one ADC to another.

At some point after the assertion of the sampling clock, the output data is valid. This data may be in parallel or serial format depending upon the ADC. Early successive approximation ADCs such as the AD574 simply provided a STATUS output (STS) which went high during the conversion, and returned to the low state when the output

data was valid. In other ADCs, this line is variously called busy, end-of-conversion (EOC), data ready, etc. Regardless of the ADC, there must be some method of knowing when the output data is

valid—and again, the data sheet is where this information can always be found.

Another detail which can cause trouble is the difference between EOC and DRDY (data ready). EOC indicates that conversion has finished, DRDY that data is available at the output. In some ADCs, EOC functions as DRDY—in others, data is not valid until several tens of nanoseconds after the EOC has become valid, and if EOC is used as a data strobe, the results will be unreliable.

There are one or two other practical points which are worth remembering about the logic of ADCs. On power-up, many ADCs do not have logic reset circuitry and may enter an anomalous logical state. Several conversions may be necessary to restore their logic to proper operation so: (a) the first few conversions after power-up should never be trusted, and (b) control outputs (EOC, data ready, etc.) may behave in unexpected ways at this time (and not necessarily in the same way at each power-up), and (c) care should be taken to ensure that such anomalous behavior cannot cause system latch-up. For example, EOC (end-of-conversion) should not be used to initiate conversion if there is any possibility that EOC will not occur until the first conversion has taken place, as otherwise initiation will never occur.

Some low-power ADCs now have power-saving modes of operation variously called standby, power-down, sleep, etc. When an ADC comes out of one of these low-power modes, there is a certain recovery time required before the ADC can operate at its full specified performance. The data sheet should therefore be carefully studied when using these modes of operation.

As a final example, some ADCs use CS (Chip Select) edges to reset internal logic, and it may not be possible to perform another conversion without asserting or reasserting CS (or it may not be possible to read the same data twice, or both).

For more detail, it is important to read the whole data sheet before using an ADC since there are innumerable small logic variations from type to type. Unfortunately, many data sheets are not as clear as one might wish, so it is also important to understand the general principles of ADCs in order to interpret data sheets correctly. That is one of the purposes of this section.

There are a couple of general trend in ADCs that should be addressed. The first is the general trend toward lower supply voltages. This is partially due to the processes, particularly CMOS, which are used to manufacture the chips. Increasing demand for speed has driven the feature size of the processes down. This typically results in lower breakdown voltages for the transistors.

This, in turn, requires lower supply voltages. Very few new parts are developed with the legacy ±15 V supplies and ±10 V input range.

Since the input signal range of the ADCs is shrinking, there is also a trend towards differential inputs. This helps improve the dynamic range of a converter, typically by 6 dB. There could be even further improvement since the common-mode ground referenced noise is rejected. In many cases the differential input can be driven single endedly (with the resultant reduction of SNR). Occasionally the REF input might also be differential.

The Comparator: A 1-Bit ADC -

A comparator is a 1-bit ADC (see Figure 5). If the input is above a threshold, the output has one logic value, below it has another. There is no ADC architecture which does not use at least one comparator of some sort. So while a 1 bit ADC is of very limited usefulness it is a building block for other architectures.

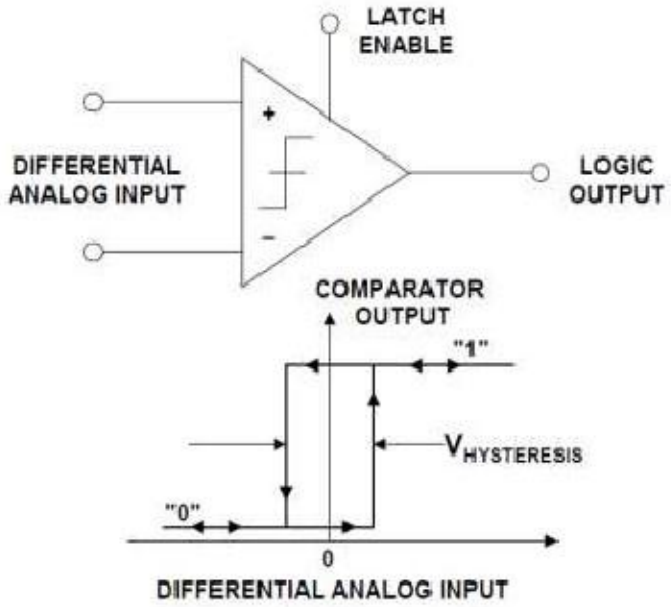


Figure 5: The Comparator: A 1-Bit ADC.

Comparators used as building blocks in ADCs need good resolution which implies high gain. This can lead to uncontrolled oscillation when the differential input approaches zero. In order to prevent this, hysteresis is often added to comparators using a small amount of positive feedback. Figure 5 shows the effects of hysteresis on the overall transfer function. Many comparators have a millivolt or two of hysteresis to encourage “snap” action and to prevent local feedback from causing instability in the transition region. Note that the resolution of the comparator can be no less than the hysteresis, so large values of hysteresis are generally not useful.

Successive Approximation ADCs -

The successive approximation ADC has been the mainstay of data acquisition for many years. Recent design improvements have extended the sampling frequency of these ADCs into the megahertz region.

The basic successive approximation ADC is shown in Figure 6. It performs conversions on command. On the assertion of the CONVERT START command, the sample-and-hold (SHA) is placed in the hold mode, and all the bits of the successive approximation register (SAR) are reset to “0” except the MSB which is set to “1.” The SAR output drives the internal DAC. If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The next most significant bit is then set to “1.” If the DAC output is greater than the analog input, this bit in the SAR is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of the SAR correspond to the value of the analog input, and the conversion is complete. These bit “tests” can form the basis of a serial output version SAR-based ADC.

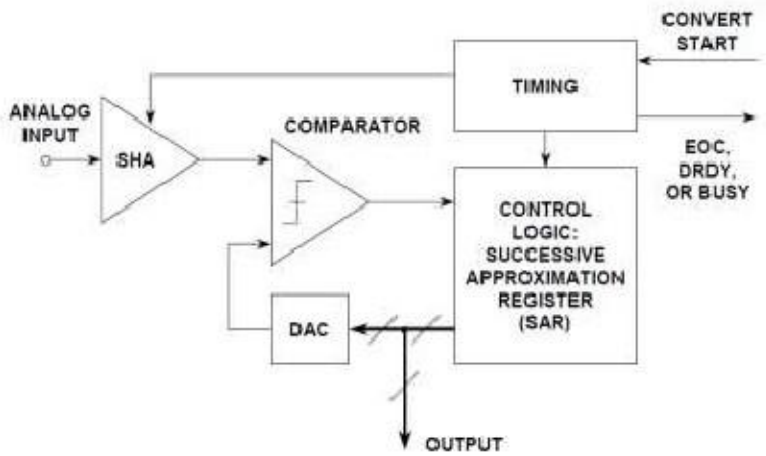


Figure 6: Basic Successive Approximation ADC(Feedback Subtraction ADC).

The fundamental timing diagram for a typical SAR ADC is shown in Figure 7. The end of conversion is generally indicated by an end-of-convert (EOC), data-ready (DRDY), or a busy signal (actually, not-BUSY indicates end of conversion). The polarities and name of this signal may be different for different SAR ADCs, but the fundamental concept is the same. At the beginning of the conversion interval, the signal goes high (or low) and remains in that state until the conversion is completed, at which time it goes low (or high). The trailing edge is generally an indication of valid output data, but the data sheet should be carefully studied—in some ADCs additional delay is required before the output data is valid.

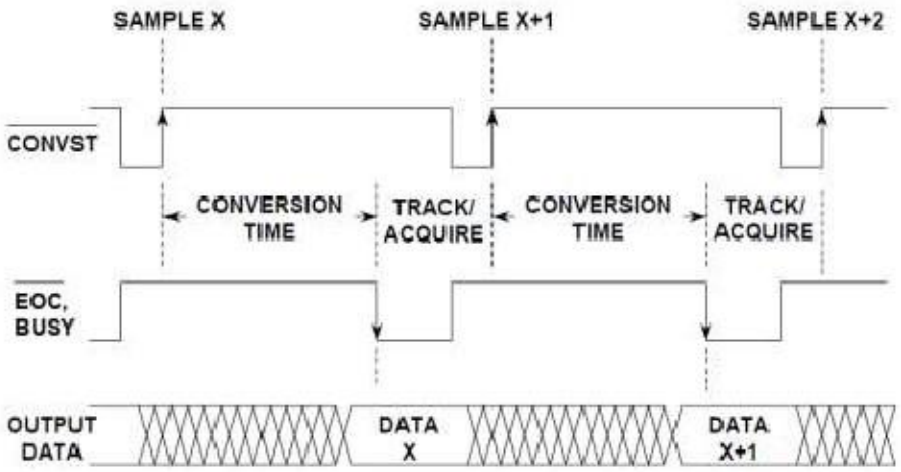


Figure 7: Typical SAR ADC Timing.

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have twice the conversion time of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

While there are some variations, the fundamental timing of most SAR ADCs is similar and relatively straightforward. The conversion process is initiated by asserting a CONVERT START signal. This signal is typically named something like CONVST or CS. This signal

is a usually a negative-going pulse whose positive-going edge actually initiates the conversion. The internal sample-and-hold (SHA) amplifier is placed in the hold mode on this edge, and the various bits are determined using the SAR algorithm.

The negative-going edge of the CONVST pulse causes a signal typically called EOC (End Of Conversion) or BUSY to go high. When the conversion is complete, the BUSY line goes low (or EOC goes high), indicating the completion of the conversion process. In most cases the trailing edge of the BUSY line can be used as an indication that the output data is valid and can be used to strobe the output data into an external register.

There may also be other control lines. And sometimes control lines have dual function. This is primarily done when the chip is pin limited. Because of the many variations in terminology and design, the individual data sheet should always be consulted when using a specific ADC.

It should also be noted that some SAR ADCs require an external high frequency clock in addition to the CONVERT START command. In most cases, there is no need to synchronize the two. The frequency of the external clock, if required, generally falls in the range of 1 MHz to 30 MHz depending on the conversion time and resolution of the ADC. Other SAR ADCs have an internal

oscillator which is used to perform the conversions and only require the CONVERT START command. Because of their architecture, SAR ADCs generally allow single-shot conversion at any repetition rate from dc to the converter's maximum conversion rate.

Notice that the overall accuracy and linearity of the SAR ADC is determined primarily by the internal DAC. Until recently, most precision SAR ADCs used laser-trimmed thin-film DACs to achieve the desired accuracy and linearity. The thin-film resistor trimming process adds cost, and the thin-film resistor values may be affected when subjected to the mechanical stresses of packaging.

For these reasons, switched capacitor (or charge-redistribution) DACs have become popular in newer SAR ADCs. The advantage of the switched capacitor DAC is that the accuracy and linearity is primarily determined by photolithography, which in turn controls the capacitor plate area and the capacitance as well as matching. In addition, small capacitors can be placed in parallel with the main capacitors which can be switched in and out under control of autocalibration routines to achieve high accuracy and linearity without the need for thin-film laser trimming. Temperature tracking between the switched capacitors can be better than 1 ppm/°C, thereby offering a high degree of temperature stability.

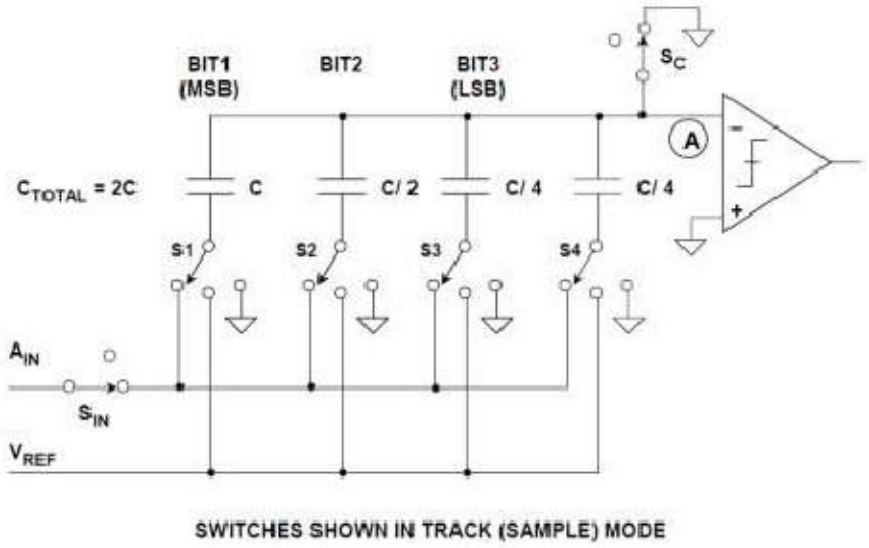


Figure 8: 3-Bit Switched Capacitor DAC.

A simple 3-bit capacitor DAC is shown in Figure 8. The switches are shown in the track, or sample mode where the analog input voltage, AIN, is constantly charging and discharging the parallel combination of all the capacitors. The hold mode is initiated by opening SIN, leaving the sampled analog input voltage on the capacitor array. Switch SC is then opened allowing the voltage at node A to move as the bit switches are manipulated. If S1, S2, S3, and S4 are all connected to ground, a voltage equal to –AIN appears at node A. Connecting S1 to VREF adds a voltage equal to VREF/2 to –AIN. The comparator then makes the MSB bit decision, and the SAR either leaves S1 connected to VREF or connects it to ground depending on the comparator output (which is high or low depending on whether the voltage at node A is negative or positive,

respectively). A similar process is followed for the remaining two bits. At the end of the conversion interval, S1, S2, S3, S4, and SIN are connected to AIN, SC is connected to ground, and the converter is ready for another cycle.

Note that the extra LSB capacitor (C/4 in the case of the 3-bit DAC) is required to make the total value of the capacitor array equal to 2C so that binary division is accomplished when the individual bit capacitors are manipulated.

The operation of the capacitor DAC (cap DAC) is similar to an R-2R resistive DAC. When a particular bit capacitor is switched to VREF, the voltage divider created by the bit capacitor and the total array capacitance (2 C) adds a voltage to node A equal to the weight of that bit. When the bit capacitor is switched to ground, the same voltage is

subtracted from node A.

An example of charge redistribution successive approximation ADCs is Analog Devices' PulSAR™ series. The AD7677 is a 16-bit, 1-MSPS, PulSAR, fully differential, ADC that operates from a single 5 V power supply. The part contains a high speed 16-bit sampling ADC, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. The AD7677 is

hardware factory calibrated and comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity. It features a very high sampling rate mode (Warp) and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

The operation of a successive approximation ADC is as follows. An example, one side of the balance is loaded with half scale (in this case 32 lbs.). Call this the proof mass. The test mass is then put on the other side of the balance. If the test mass is greater, as it is in this case, the proof mass is retained, otherwise it is discarded. Next a proof mass equal to ¼ scale is added. Again, if the test mass is still greater the proof mass is retained, otherwise it is rejected. It the example it is rejected. This process is continued, each time cutting the proof mass in half, until the desired resolution is reached. The proof masses are added up. This will equal the mass of the test mass, to the resolution of the test.

FLASH ADC -

As the nomenclature implies, Flash ADC conversion is the fastest possible way to quantize an analog signal. The concept of this

architecture is relatively simple to understand. In order to achieve N-bit from a flash ADC, it requires $2^N - 1$ comparators, $2^N - 1$ reference levels and digital encoding circuits. The reference levels of comparators are usually generated by a resistor string.

One example of simple flash ADC is shown in Figure 9. First, the analog input signal is sampled by comparators and is compared with one of the reference levels. Then, each comparator produces an output based on whether the sampled input signal is larger or smaller than the reference level. The comparators generate the digital output as a thermometer code. This thermometer code output is usually converted to a binary or a gray digital code by encoding logic circuits at the end. Since this operation is done in only one clock cycle, a flash ADC can attain the highest conversion rate.

The high sensitivity of the comparator offset and a large circuit area are the main drawbacks of a flash ADC. For instance, to build a 10-bit ADC based on flash architecture requires more than 1,023 comparators. Therefore, it will occupy a very large chip area and dissipate high power. Moreover, each comparator must have an offset voltage smaller than $1/2^{10}$, which is quite difficult to build. That is why we seldom see flash architecture with ADCs of more than 8-bits.

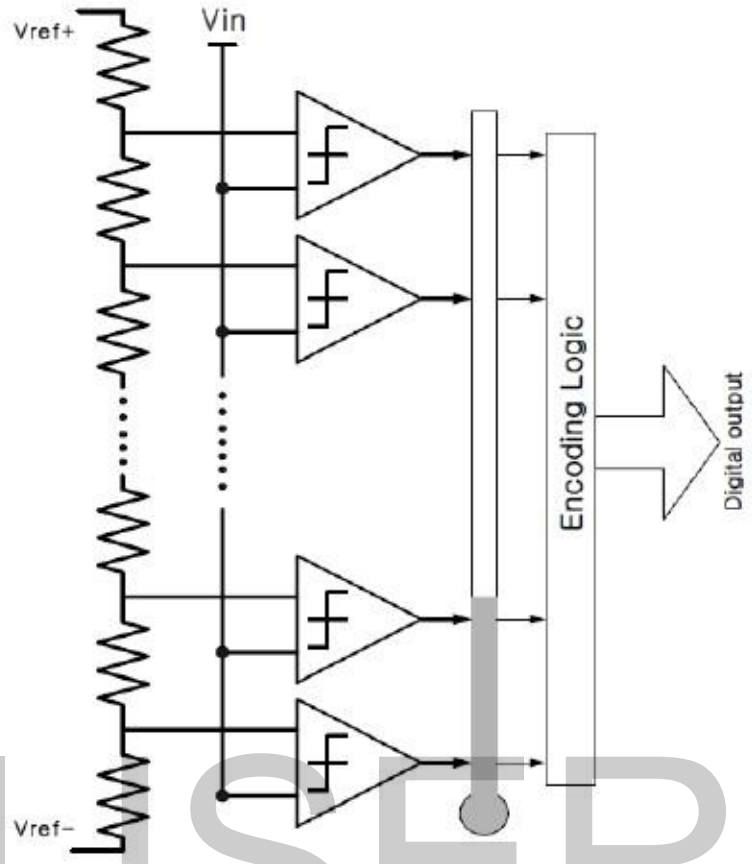


Figure 9: Flash ADC

TWO STEP FLASH ADC -

The block diagram of a two-step flash ADC is shown in Figure 10. It consists of a Sample and Hold Amplifier (SHA), two low-resolution flash ADCs, a digital-to-analog (DAC), a subtracter and a gain block. The conversion is executed in two-steps as the name implies. The sampled analog signal is digitized by the first coarse quantizer producing the B_1 Most Significant Bits (MSBs). This digital code is changed back to an analog signal by the DAC and

subtracted from the sampled input signal producing the residue signal. The residue signal is amplified by the gain block and digitized by the second quantizer producing the B_2 LSBs. Because 1-bit out of the output digital codes is often used for error correction, the overall resolution is (B_1+B_2-1) bit.

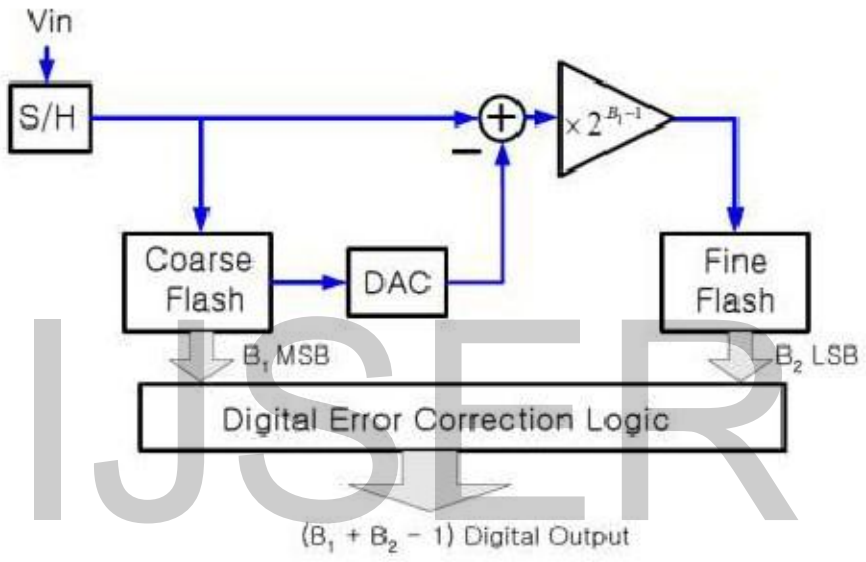


Figure 10: Two step flash ADC

In a subranging architecture, the fine quantizer must have full resolution accuracy while the coarse quantizer can have a much more relaxed accuracy requirement. In the two-step flash architecture, both quantizers can have relaxed accuracy requirement because the gain block amplifies the residue signal to the full input scale. The major drawback of the two-step ADC is that the DAC must have an accuracy of the entire resolution of the

ADC. The DAC needs time to settle to the required accuracy and will limit the conversion speed of the ADC.

FOLDING ADC -

A folding ADC can have a high-speed conversion rate because it uses the parallelism of the flash ADC but uses fewer comparators and less power dissipation than a conventional flash ADC. This performance is achieved by adapting analog preprocessing. A typical block diagram of a folding ADC is shown in Figure 11. The analog preprocessor, in front of the fine quantizer, consists of folding amplifiers that generate the folded signals. The folded signal is similar to the residue signal in a subranging ADC, except for the fact that the residue signal is not generated from the output results of the coarse quantizer. A high conversion rate is achieved because the coarse and fine quantizers are in parallel. The open-loop design of the folding amplifiers also speeds up the converter.

Ideally, an analog preprocessor should generate a sawtooth waveform, but this is difficult to implement. Instead, a triangle waveform is used in actual implementation, but sharp corners remain difficult to realize.. The actual waveform is more sinusoidal, and causes nonlinearity errors in the ADC.

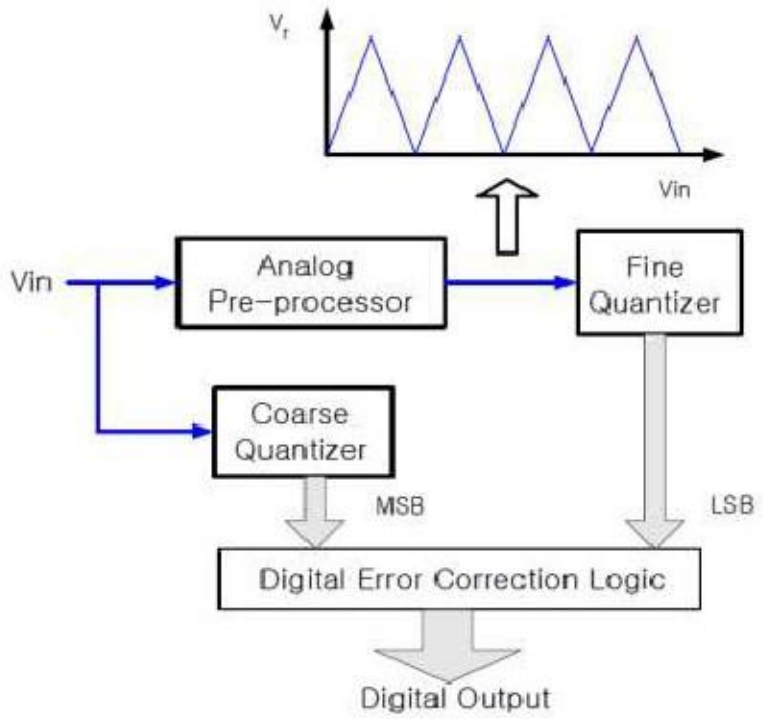


Figure 11: Folding ADC.

SUBRANGING ADC -

In order to overcome such drawbacks as hardware complexity, large chip area and high power dissipation, subranging architecture was developed at the cost of the sampling speed. A simplified subranging ADC is illustrated in Figure 12. It comprises a SHA, reference level generators, comparators and decoders. The number of comparators is $2^{N/M} \times M$, where N is the total ADC resolution, and M is the number of stages. For a 2-stage (two-stage?) 10-bit subranging ADC, only 64 comparators are required instead of the 1,024 comparators in a flash ADC. Therefore,

compared with a flash ADC, subranging architecture yields a quite significant reduction in power consumption and in the required circuit area However, the conversion in subranging architecture is done by multiple clocks instead of one clock as in a flash ADC. The operation of the 2-stage subranging ADC is as follows: In the first clock, an analog input signal is sampled by the SHA and quantized by a coarse flash ADC that determines the most significant bit from the sampled input signal. In the next clock, the segment of the resistor string is selected by the results from the coarse flash ADC, and the least significant bits are produced by the fine flash ADC. The comparator requirement of the coarse flash ADC can be relaxed, but the comparators of the fine flash ADC should be as accurate as the full resolution of the ADC. The conversion speed decreases as the number of subranging stages increase.

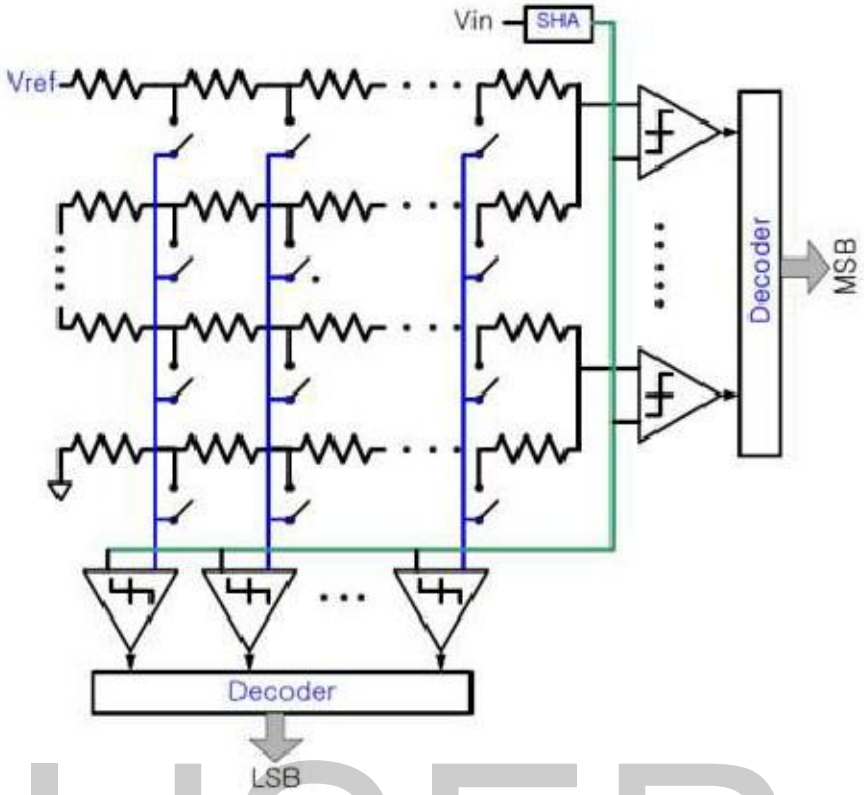


Figure 12: Subranging ADC.

PIPELINE ADC -

A typical pipeline architecture is illustrated in Figure 13. Each stage has the four elements of a SHA, a sub-ADC, a sub-DAC and an inter-stage gain amplifier.

The operation of a single stage consists of four steps. First, the input signal is captured by the sample and hold amplifier. Second, this signal is quantized by the sub-ADC, which produces a digital output. Third, this digital signal goes to the sub-DAC which converts it to an analog signal. This analog signal is subtracted

from the original sampled signal – thereby, leaving a residual signal. Fourth, this residual signal is increased to the full scale through the inter-stage amplifier.

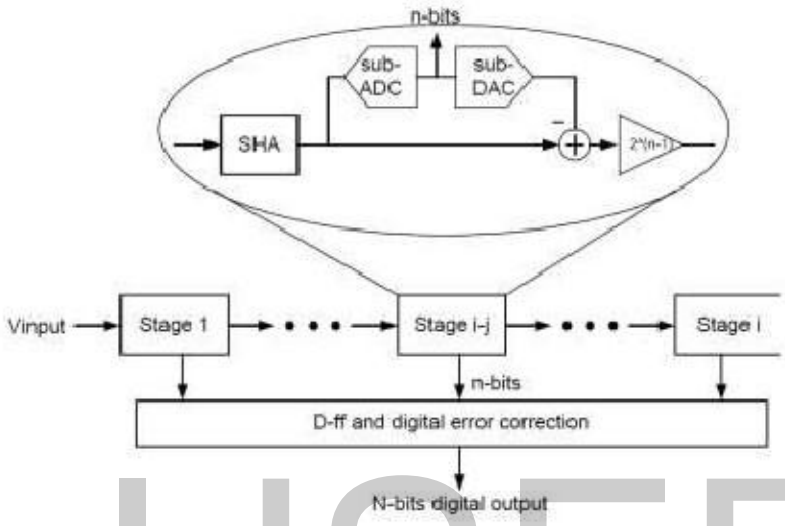


Figure 13: A pipeline ADC block diagram.

The residual signal is passed to the next stage and the procedure mentioned above is repeated. Since every stage has the element of sample and hold, the above procedure occurs concurrently in every stage. The most interesting feature of a pipeline ADC is the throughput behavior. For a pipeline with i-stages, the very first signal will take i-clock cycles to go through the entire i-stages. Obviously, it will have the latency of i-clock cycles. The next signal – given the nature of the sample and hold element – will have the latency of (i-1) clock cycles. After i-clock cycles, we will have a complete digital output in every clock cycle. At this moment, each

sampled signal will have the latency of a singular clock cycle. The advantage of a pipeline ADC is that the conversion rate does not depend on the number of stages. The overall speed is determined by the speed of the single stage.

OVERSAMPLED ADC -

A sigma-delta ADC is also known as an oversampling data converter. The ADCs seen so far in this study are often called as Nyquist rate ADCs because the conversion rate of those ADCs is equal to the Nyquist rate. In sigma-delta ADCs, however, the sampling is performed at a much higher rate than the Nyquist rate. The ratio of the sampling rate to the Nyquist rate is called the oversampling ratio (OSR). Each doubling OSR allows to reduce the quantization noise power resulting in 3dB SNR improvement.

A sigma-delta ADC also uses noise-shaping techniques to increase resolution. The quantization noise power is moved to higher frequencies by negative feedback. Then, the out-of-band noise is removed by a digital low pass filter, leaving only a small amount of the quantization noise. The conceptual block diagram is shown in Figure 14. It consists of a S/H, a sigma delta modulator, a digital filter and a down sampler. The down sampler converts the oversampled digital signal into the lower sample rate digital signal.

The resolution of the sigma delta ADC can be enhanced by increasing either the order of the modulator or the resolution of the quantizer. An L-th-order sigma delta modulator improves SNR by 6L + 3dB/octave. However, increasing the order of the modulator more than 2 nd can cause instability problems. To avoid instability problem with a high order modulator, a special architecture like multi-stage noise shaping (MASH) can be employed. Increasing the resolution of the quantizer also cause a problem because of the nonlinearity of the DAC. Dynamic element matching is one of the methods available to reduce the distortion from the multi-bit DAC.

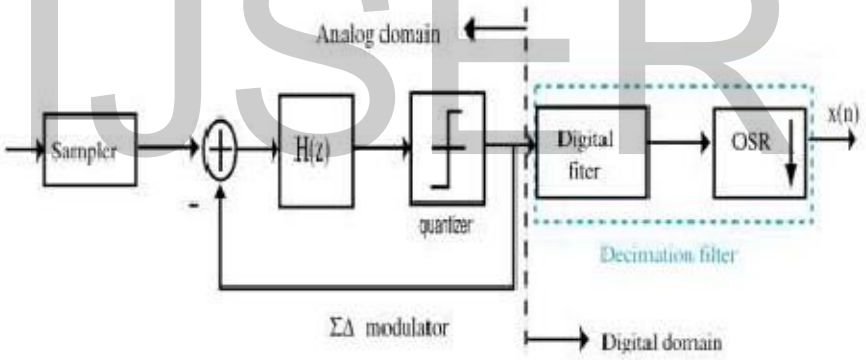


Figure 14: Block diagram of an oversampling ADC.

ADC TYPES

Analog-to-Digital Converters (ADCs) transform an analog voltage to a binary number (a series of 1's and 0's), and then eventually to a digital number (base 10) for reading on a meter, monitor, or chart.

The number of binary digits (bits) that represents the digital number determines the ADC resolution. However, the digital number is only an approximation of the true value of the analog voltage at a particular instant because the voltage can only be represented (digitally) in discrete steps. How closely the digital number approximates the analog value also depends on the ADC resolution.

A mathematical relationship conveniently shows how the number of bits an ADC handles determines its specific theoretical resolution: An n-bit ADC has a resolution of one part in 2n. For example, a 12-bit ADC has a resolution of one part in 4,096, where 212 = 4,096. Thus, a 12-bit ADC with a maximum input of 10 VDC can resolve the measurement into 10 VDC/4096 = 0.00244 VDC = 2.44 mV. Similarly, for the same 0 to 10 VDC range, a 16-bit ADC resolution is 10/216 = 10/65,536 = 0.153 mV. The resolution is usually specified with respect to the full-range reading of the ADC, not with respect to the measured value at any particular instant.

Successive-Approximation ADCs A successive-approximation converter, Figure 15, is composed of a digital-to-analog converter (DAC), a single comparator, and some control logic and registers. When the analog voltage to be measured is present at the input to the comparator, the system control logic initially sets all bits to

zero. Then the DAC's most significant bit (MSB) is set to 1, which forces the DAC output to 1/2 of full scale (in the case of a 10-V full-scale system, the DAC outputs 5.0 V).

The comparator then compares the analog output of the DAC to the input signal, and if the DAC output is lower than the input signal, (the signal is greater than 1/2 full scale), the MSB remains set at 1. If the DAC output is higher than the input signal, the MSB resets to zero. Next, the second MSB with a weight of 1/4 of full scale turns on (sets to 1) and forces the output of the DAC to either 3/4 full scale (if the MSB remained at 1) or 1/4 full scale (if the MSB reset to zero). The comparator once more compares the DAC output to the input signal and the second bit either remains on (sets to 1) if the DAC output is lower than the input signal, or resets to zero if the DAC output is higher than the input signal. The third MSB is then compared the same way and the process continues in order of descending bit weight until the LSB is compared. At the end of the process, the output register contains the digital code representing the analog input signal.

Successive approximation ADCs are relatively slow because the comparisons run serially, and the ADC must pause at each step to set the DAC and wait for its output to settle. However, conversion rates easily can reach over 1 MHz. Also, 12 and 16-bit successive-

approximation ADCs are relatively inexpensive, which accounts for their wide use in many PC-based data acquisition systems.

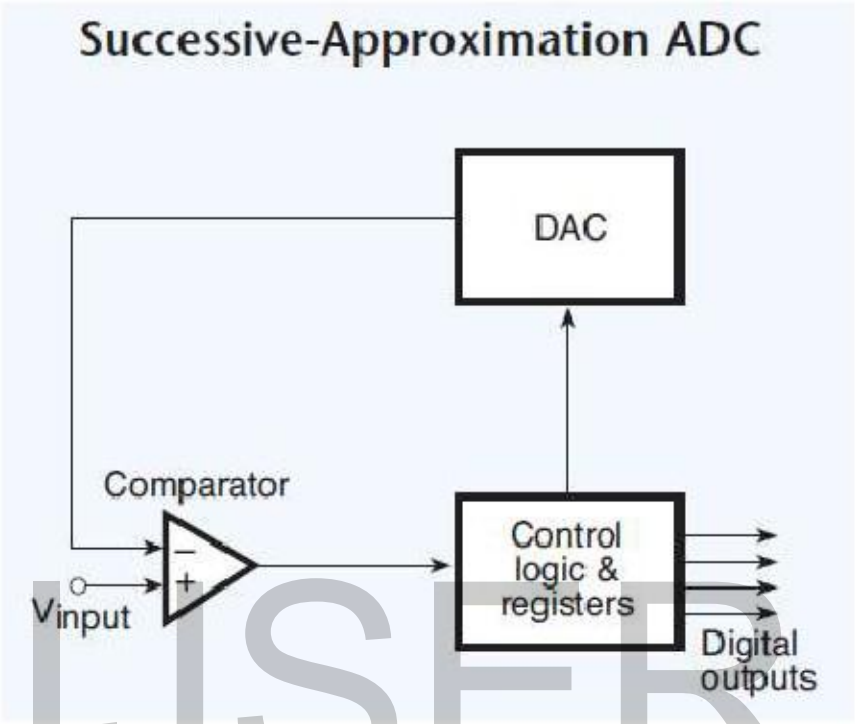


Fig. 15. Interestingly, this ADC uses a digital-toanalog converter and a comparator.

The logic sets the DAC to zero and starts counting up, setting each following bit until it reaches the value of the measured input voltage. The conversion is then finished and the final number is stored in the register.

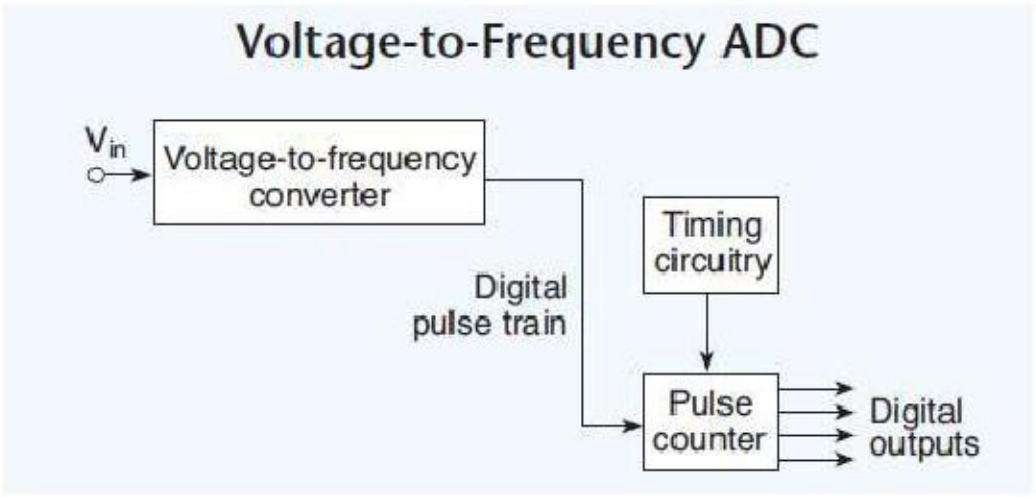


Fig. 16. Voltage-to-frequency converters reject noise well and frequently are used for measuring slow signals or those in noisy environments.

Voltage-To-Frequency ADCs –

Voltage-to-frequency ADCs convert the analog input voltage to a pulse train with the frequency proportional to the amplitude of the input. (See Figure 16.) The pulses are counted over a fixed period to determine the frequency, and the pulse counter output, in turn, represents the digital voltage.

Voltage-to-frequency converters inherently have a high noise rejection characteristic, because the input signal is effectively integrated over the counting interval. Voltage-to-frequency conversion is commonly used to convert slow and noisy signals. Voltage-to-frequency ADCs are also widely used for remote sensing

in noisy environments. The input voltage is converted to a frequency at the remote location and the digital pulse train is transmitted over a pair of wires to the counter. This eliminates noise that can be introduced in the transmission lines of an analog signal over a relatively long distance.

Integrating ADCs: Dual Slope -

A number of ADCs use integrating techniques, which measure the time needed to charge or discharge a capacitor in order to determine the input voltage. A widely used technique, called dual-slope integration, is illustrated in Figure 17. It charges a capacitor over a fixed period with a current proportional to the input voltage. Then, the time required to discharge the same capacitor under a constant current determines the value of the input voltage. The technique is relatively accurate and stable because it depends on the ratio of rise time to fall time, not on the absolute value of the capacitor or other components whose values change over temperature and time.

Integrating the ADC input over an interval reduces the effect of noise pickup at the ac line frequency when the integration time is matched to a multiple of the ac period. For this reason, it is often used in precision digital multimeters and panel meters. Although 20-bit accuracy is common, it has a relatively slow conversion rate,

such as 60 Hz maximum, and slower for ADCs that integrate over multiples of the line frequency.

Sigma-Delta ADCs-

A sigma-delta ADC is another type of integrating ADC. It contains an integrator, a DAC, a comparator, and a summing junction. (See Figure 18.) Like the dual-slope ADC, it's often used in digital multimeters, panel meters, and data acquisition boards. Sigmadelta converters are relatively inexpensive primarily because they have a single-bit DAC, but they can obtain high-resolution measurements using oversampling techniques. Although the ADC works best with low-bandwidth signals (a few kHz), it typically has better noise rejection than many others, and users can set the integration time (albeit below 100 samples/sec).

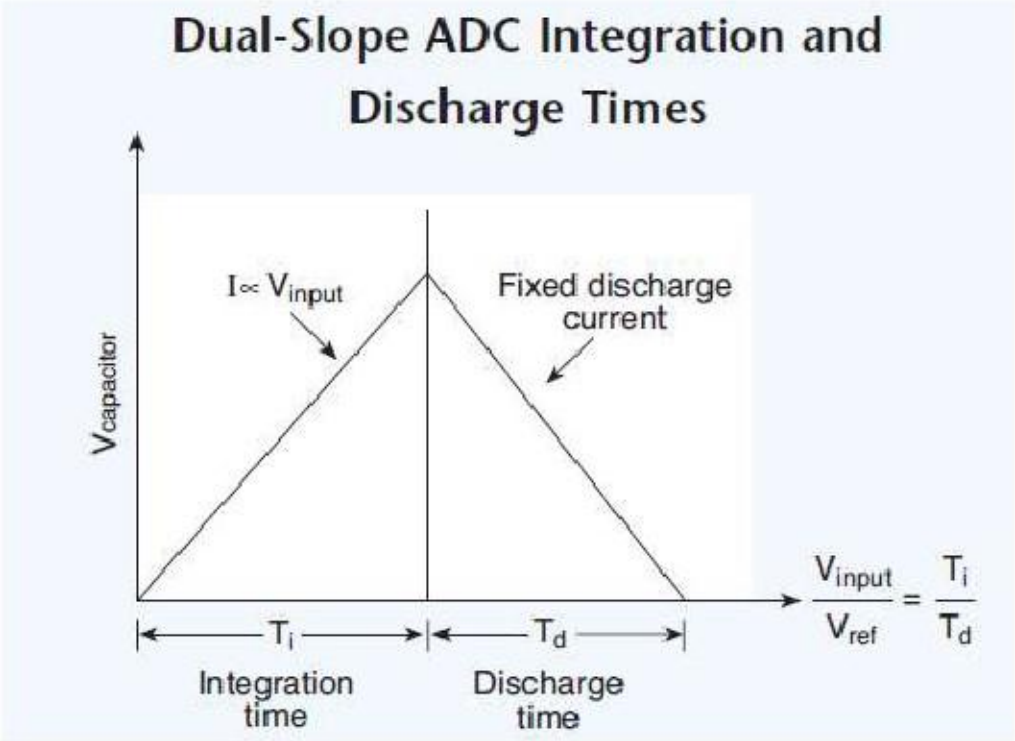


Fig. 17. Dual-slope integrating ADCs provide high-resolution measurements with excellent noise rejection.

They integrate upward from an unknown voltage and then integrate downward with a known source voltage. They are more accurate than single slope ADCs because component errors are washed out during the de-integration period. they have a single-bit DAC, but they can obtain high-resolution measurements using oversampling techniques. Although the ADC works best with low-bandwidth signals (a few kHz), it typically has better noise rejection than many others, and users can set the integration time (albeit below 100 samples/sec).

Sigma-delta ADCs also require few external components. They can accept low-level signals without much input-signal conditioning circuitry for many applications, and they don't require trimming or calibration components because of the DAC's architecture. The ADCs also contain a digital filter, which lets them work at a high oversampling rate without a separate anti-aliasing filter at the input. Sigma-delta ADCs come in 16 to 24-bit resolution, and they are economical for most data acquisition and instrument applications.

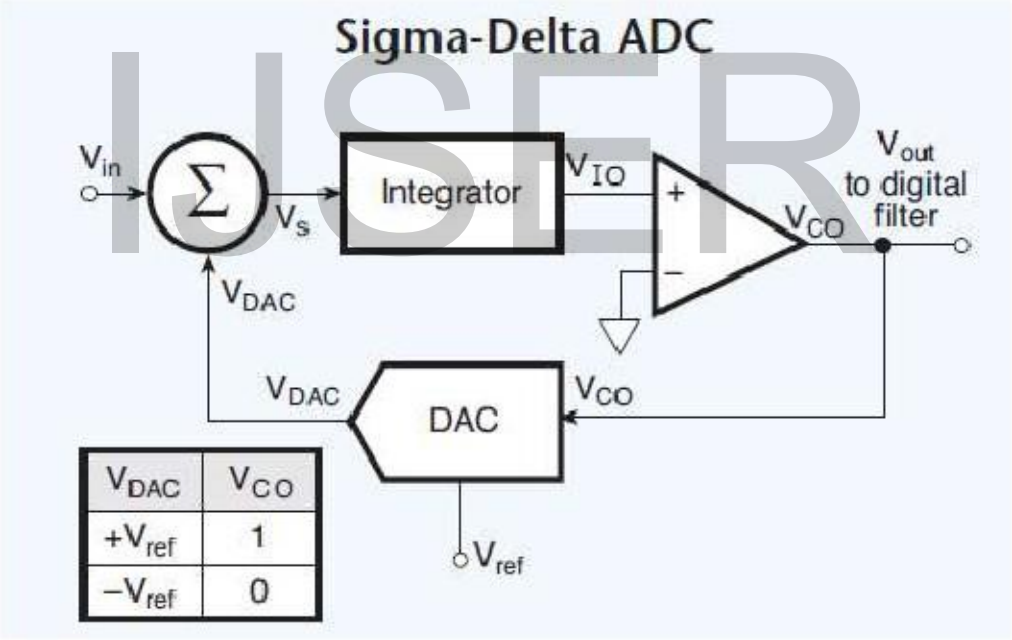


Fig. 18. Integrating converters such as the sigma-delta ADC have both high resolution and exceptional noise rejection.

They work particularly well for low-bandwidth measurements and reject high-frequency noise as well as 50/60 Hz interference.

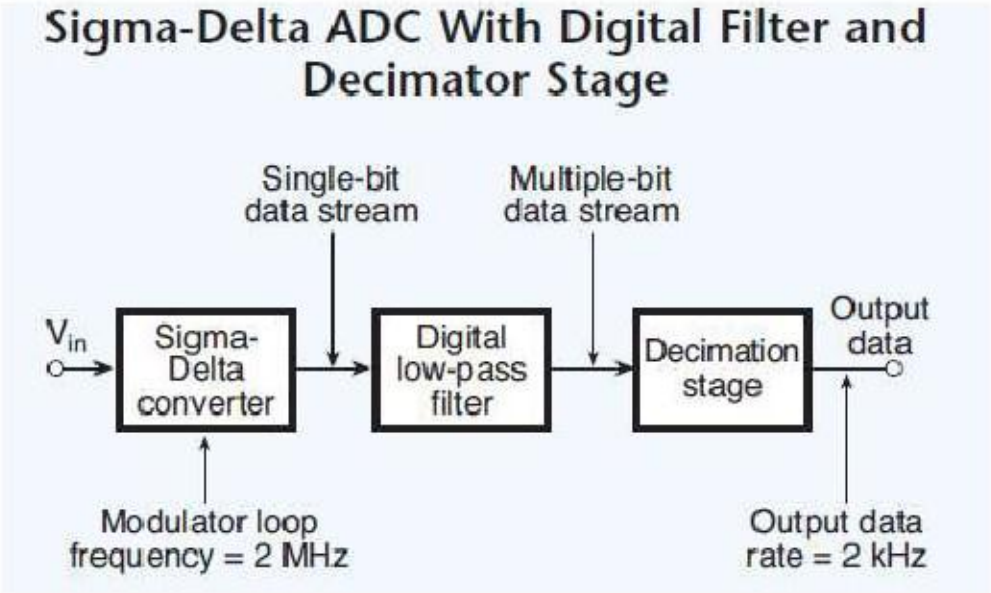


Fig. 19. Sigma-delta ADCs are well suited to high-resolution acquisition because they use oversampling and often combine an analog modulator, a digital filter, and a decimator stage.

The low-pass digital filter converts the analog modulator output to a digital signal for processing by the decimator. The principle of operation can be understood from the diagram. The input voltage Vin sums algebraically with the output voltage of the DAC, and the integrator adds the summing point output Vs to a value it stored previously. When the integrator output is equal to or greater than zero, the comparator output switches to logic one, and when the integrator output is less than zero, the comparator switches to logic zero. The DAC modulates the feedback loop, which continually adjusts the output of the comparator to equal the analog input and maintain the integrator output at zero. The DAC keeps the

integrator's output near the reference voltage level. Through a series of iterations, the output signal becomes a one-bit data stream (at a high sample rate) that feeds a digital filter. The digital filter averages the series of logic ones and zeros, determines the bandwidth and settling time, and outputs multiple-bit data. The digital low-pass filter then feeds the decimation filter, which in turn, decreases the sample rate of the multi-bit data stream by a factor of two for each stage within the filter. For example, a seven-stage filter can provide a sample-rate reduction of 128.

Improved Accuracy - The digital filter shown in Figure 19 inherently improves the ADC's accuracy for ac signals in two ways. First, when the input signal varies (sine wave input) and the system samples the signal at several times the Nyquist value (refer to page 17), the integrator becomes a low-pass filter for the input signal, and a high-pass filter for the quantization noise. The digital filter's averaging function then lowers the noise floor even further, and combined with the decimation filter, the data stream frequency at the output is reduced. For example, the modulator loop frequency could be in the MHz region, but the output data would be in the kHz region. Second, the digital filter can be notched at 60 Hz to eliminate power line frequency interference.

The output data rate from the decimation filter is lower than the initial sample rate but still meets the Nyquist requirement by saving certain samples and eliminating others. As long as the output data rate is at least two times the bandwidth of the signal, the decimation factor or ratio M can be any integer value. For example, if the input is sampled at fs, the output data rate can be fs/M without losing information. This technique provides more stable readings.

Table of ADC Attributes

ADC Type	Typical Resolution	Typical Conversion Rate*/Frequency
Sigma-Delta	16–24 bit	1 sps–128 ksps
Successive Approximation	8–16 bit	10 ksps–2 Msps
Voltage-to-Frequency	8–12 bit	1 Hz–4 MHz**
Integrating	12–24 bit	1 sps–1 ksps**

* sps = samples per second
** With line cycle rejection

Table 1. Table of ADC attributes.

A/D CONVERTER BUILDING BLOCKS

Sample-and-Hold -

Inherent to the A/D conversion process is a sample-and-hold (S/H) circuit that resides in the front-end of a converter (and also between stages in a pipeline converter). In addition to suffering from additive circuit noise and signal distortion just as the rest of the converter does, the S/H also requires a precision time base to define the exact acquisition time of the input signal. The dynamic performance degradation of an ADC can often be attributed to the deficiency of the S/H circuit (and the associated buffer amplifier).

The main function of an S/H circuit is to take samples of its input signal and hold its value until the A/D converter can process the information. Typically, the samples are taken at uniform time intervals; thus, the sampling rate (or clock rate) of the circuit can be determined. The operation of an S/H circuit can be divided into sample mode (sometimes also referred as acquisition mode) and hold mode, whose durations need not be equal. In sample mode, the output can either track the input, in which case the circuit is often called a track-and-hold (T/H) circuit or it can be reset to some fixed value. In hold mode an S/H circuit remembers the value of the input signal at the sampling moment and thus it can be considered as an analog memory cell. The basic circuit elements

that can be employed as memories are capacitors and inductors, of which the capacitors store the signal as a voltage (or charge) and the inductors as a current. Since capacitors and switches with a high off-resistance needed for a voltage memory are far easier to implement in a practical integrated circuit technology than inductors and switches with a very small on-resistance required for a current memory, all sample-and-hold circuits are based on voltage sampling with switched capacitor (SC) technique.

Figure 20 illustrates three common configurations for closed-loop switchedcapacitor S/H circuits. For simplicity, single-ended configurations are shown; however in circuit implementation all would be fully differential. In a mixed-signal circuit such as A/D converters, fully differential analog signals are preferred as a means of getting a better power supply rejection and immunity to common mode noise. The operation needs two non-overlapping clock phases – sampling and holding or transferring. Switch configurations shown in Fig. 20 are for the sampling phase, while configurations shown in Fig. 21 are for hold phase.

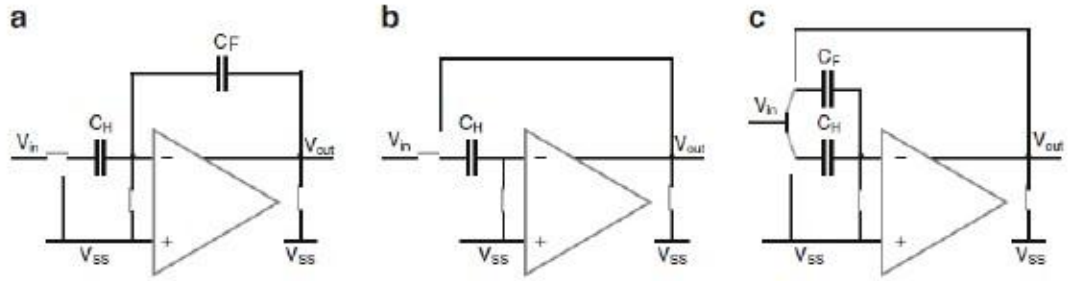


Fig. 20 Switched capacitor S/H circuit configurations in sample phase: (a) a circuit with separate CH and CF, (b) a circuit with one capacitor, and (c) a circuit with CF shared as a sampling capacitor.

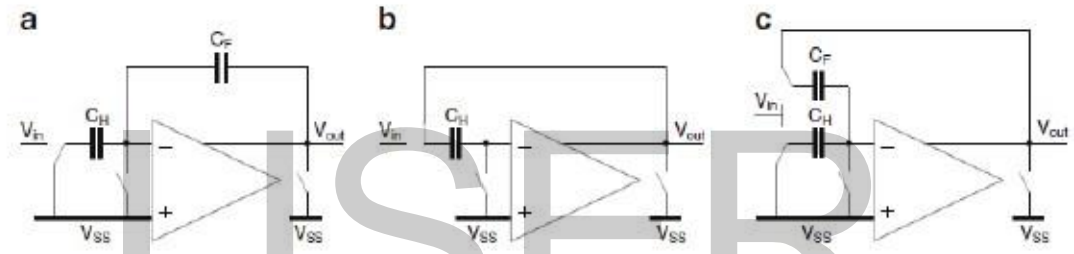


Fig. 21 Switched capacitor S/H circuit configurations in hold phase: (a) a circuit with separate CH and CF, (b) a circuit with one capacitor, and (c) a circuit with CF shared as a sampling Capacitor.

In all cases, the basic operations include sampling the signal on the sampling capacitor(s) C_H and transferring the signal charge onto the feedback capacitor C_F by using an op amp in the feedback configuration. In the configuration in Fig. 20a, which is often used as an integrator, assuming an ideal op amp and switches, the op amp forces the sampled signal charge on C_H to transfer to C_F. If C_H and C_F are not equal capacitors, the signal charge transferred to C_F

will display the voltage at the output of the op amp according to $V_{out} = (C_H/C_F)\, V_{in}$. In this way, both S/H and gain functions can be implemented within one SC circuit. In the configuration shown in Fig. 20b, only one capacitor is used as both sampling capacitor and feedback capacitor. This configuration does not implement the gain function, but it can achieve high speed because the feedback factor (the ratio of the feedback capacitor to the total capacitance at the summing node) can be much larger than that of the previous configuration, operating much closer to the unity gain frequency of the amplifier. Furthermore, it does not have the capacitor mismatch limitation as the other two configurations. Here, the sampling is performed passively, i.e. it is done without the op amp, which makes signal acquisition fast. In hold mode the sampling capacitor is disconnected from the input and put in a feedback loop around the op amp.

Figure 20c shows another configuration which is a combined version of the configurations in Fig. 20a and Fig. 20b. In this configuration, in the sampling phase, the signal is sampled on both C_H and C_F, with the resulting transfer function $V_{out} = (1 + (C_H/C_F))\, V_{in}$. In the next phase, the sampled charge in the sampling capacitor is transferred to the feedback capacitor. As a result, the feedback capacitor has the transferred charge from

the sampling capacitor as well as the input signal charge. This configuration has a wider bandwidth in comparison to the configuration shown in Fig. 20a, although feedback factor is comparable.

Operational Amplifier -

In front-end S/H amplifiers or multi-stage A/D converters, precision op amps are almost invariably employed to relay the input signal (or the residue signal) to the trailing conversion circuits. Operating on the edge of the performance envelope, op amps exhibit intense trade-offs amongst the dynamic range, linearity, settling speed, stability, and power consumption. As a result, the conversion accuracy and speed are often dictated by the performance of these amplifiers.

Amplifiers with a single gain stage have high output impedance providing an adequate dc gain, which can be further increased with gain boosting techniques. Single-stage architecture offers large bandwidth and a good phase margin with small power consumption. Furthermore, no frequency compensation is needed, since the architecture is self-compensated (the dominant pole is determined by

the load capacitance), which makes the footprint on the silicon small. On the other hand, the high output impedance is obtained by sacrificing the output voltage swing, and the noise is rather high as a result of the number of noise-contributing devices and limited voltage head-room for current source biasing.

The simplest approach for the one-stage high-gain operational amplifier is telescopic cascode amplifier of Fig. 22a. With this architecture, a high open loop dc gain can be achieved and it is capable of high speed when closed loop gain is low.

The number of current legs being only two, the power consumption is small. The biggest disadvantage of a telescopic cascode amplifier is its low maximum output swing, VDD_5VDS,SAT, where VDD is the supply voltage and VDS,SAT is the saturation voltage of a transistor. With this maximum possible output swing the input commonmode range is zero. In practice, some input common-mode range, which reduces the output swing, always has to be reserved so as to permit inaccuracy and settling transients in the signal common-mode levels. The high-speed capability of the amplifier is the result of the presence of only n-channel transistors in the signal path and of relatively small capacitance at the source of the cascode transistors.

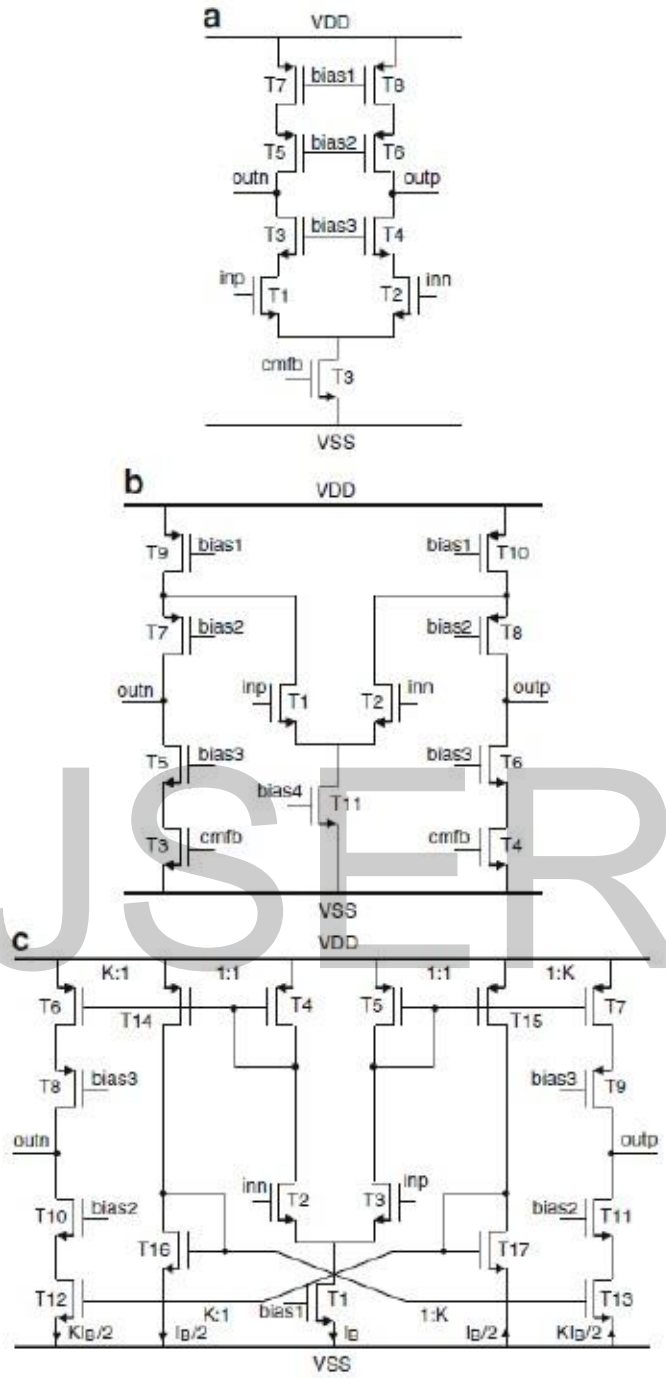


Fig. 22 One-stage amplifiers: (a) Telescopic cascade, (b) folded cascade, and (c) push–pull current-mirror amplifier with a cascade output stage.

The gain-bandwidth product of the amplifier is given by $\mathrm{GBW} = g_{m1}/C_L$, where g_{m1} is the transconductance of transistors T_1 and C_L is the load capacitance. Thus, the GBW is limited by the load capacitance. Due to its the simple topology and dimensioning, the telescopic cascode amplifier is preferred if its output swing is large enough for the specific application. The output signal swing of this architecture has been widened by driving the transistors T_7-T_8 into the linear region. In order to preserve the good common mode rejection ratio and power supply rejection ratio properties of the topology, additional feedback circuits for compensation have been added to these variations. The telescopic cascode amplifier has low current consumption, relatively high gain, low noise and very fast operation. However, as it has five stacked transistors, the topology is not suitable for low supply voltages.

The folded cascode amplifier topology is shown in Fig. 22b. The swing of this design is constrained by its cascoded output stage. It provides a larger output swing and input common-mode range than the telescopic amplifier with the same dc gain and without major loss of speed.

A push-pull current-mirror amplifier, shown in Fig. 22c, has much better slew-rate properties and potentially larger bandwidth and dc

gain than the folded cascade amplifier. The slew rate and dc gain depend on the current-mirror ratio K, which is typically between one and three. However, too large current-mirror ratio increases the parasitic capacitance at the gates of the transistors T12 and T13, pushing the non-dominant pole to lower frequencies and limiting the achievable GBW. The nondominant pole of the current mirror amplifier is much lower than that of the folded cascode amplifier and telescopic amplifiers due to the larger parasitic capacitance at the drains of input transistors. The noise and current consumption of the currentmirror amplifier are larger than in the telescopic cascode amplifier or in the folded cascode amplifier.

Latched Comparators -

The offset in preamps and comparators constitutes the major source of error in flash-type converters. Simple differential structure with thin oxide devices will keep dominating the preamp architecture in newer technologies. Dynamic performance is crucial at high sample rates with high input frequencies.

Because of its fast response, regenerative latches are used, almost without exception, as comparators for high-speed applications. An ideal latched comparator is composed of a preamplifier with infinite gain and a digital latch circuit. Since the amplifiers used in

comparators need not to be either linear or closed-loop, they can incorporate positive feedback to attain virtually infinite gain. Because of its special architecture, working process of a latched comparator could be divided in two stages: tracking and latching stages. In tracking stage the following dynamic latch circuit is disabled, and the input analog differential voltages are amplified by the preamplifier. In the latching stage while the preamplifier is disabled, the latch circuit regenerates the amplified differential signals into a pair of full-scale digital signals with a positive feedback mechanism and latches them at output ends.

Depending on the type of latch employed, the latch comparators can be divided into two groups: static, which have a constant current consumption during operation and dynamic, which does not consume any static power. In general, the type of latch employed is determined by the resolution of the stage. For a low-resolution quantization per stage, a dynamic latch is more customary since it dissipates less power than the static latch (the dynamic latch does not dissipate any power during the resetting period), even though the difference is negligible at high clock rates. While the latch circuits regenerate the difference signals, the large voltage variations on regeneration nodes will introduce the instantaneous large currents. Through parasitic gate-source and gate-drain capacitances of transistors, the instantaneous currents

are coupled to the inputs of the comparators, making the disturbances unacceptable. It is so-called kickback noise

influence. In flash A/D converters where a large number of comparators are switched on or off at the same time, the summation of variations came from regeneration nodes may become unexpectedly large and directly results in false quantization code output. It is for this reason that the static latch is preferable for higher-resolution implementations.

DESIGN OF LOW POWER SIGMA DELTA ADC

Advances in the integrated circuit (IC) technology have paved way for more compact and efficient implementation of digital logic on silicon. This indeed moved many types of signal processing to the digital domain. One of the major applications of this phenomenon is in data converters i.e., Analog-to-Digital converter (ADC) and Digital-to-Analog converter (DAC).

Among the various Analog-to-Digital data, converters usually successive approximation or dual slope ADCs are used when high resolution is desired. But to achieve higher accuracy, trimming is required. The main constraint using these architectures is the design of high precision sample and hold circuits. The over sampling converters use digital signal processing techniques in

place of complex and precise analog components, which, gives scope to achieve much higher resolution than the Nyquist rate converters. Sigma Delta ADC, a type of oversampling ADC is highly tolerant to analog circuit imperfections, thus making it a good choice to realize embedded ADC interfaces in modern systems-on-chip (SoCs).

The sigma-delta ADC works on the principle of sigma-delta modulation. The sigma-delta ($\Sigma\Delta$) modulation is a method for encoding high-resolution signals into lower resolution signals using pulse-density modulation. It falls under the category of oversampling ADC's as it samples the input signal at a rate much higher than the Nyquist rate. A sigma-delta ADC comprises of an analog block of modulator and a digital block of decimator. The modulator is used to sample the input signal at an oversampling rate, generating a one bit output stream and decimator is a digital filter or down sampler where the actual digital signal processing is done. The decimator which is a crucial part of a sigma-delta ADC converts this one bit stream from modulator to a N bit stream according to resolution of ADC. This relaxes the requirement for high precision analog circuits required for the modulator stage and also increases the final output resolution of the ADC .

In the present study, a modulator design in cadence analog environment and digital decimator design in verilog HDL in CADENCE mixed signal design environment is presented. The output of the modulator will be at the oversampling rate and its noise is shaped such that the signal is contaminated with quantization noise at higher (out of band) frequencies. This noise has to be filtered out using a digital filter.

There have been a number of approaches to realize low power Delta Sigma modulators . In this study, some low power optimization methods have been adopted in the design at both system and circuit level. A CIFB topology is used to design the system which ensures stable operation and low power consumption. A single-bit comparator and an advanced SC integrator topology based on Transmission Gates, which achieve high SNR is chosen.

Depending on the sampling rate, analog-to-digital converters are categorized into two types namely Nyquist rate converters and oversampling converters. Nyquist rate ADCs sample the analog input at the Nyquist frequency, fn such that $f_s = f_n = 2 \times f_b$, where f_s is the sampling frequency and f_b is the bandwidth of the input signal. Oversampling ADCs sample the analog input at much higher frequencies than the Nyquist frequency. Sigma-delta ADCs come under this category. In a sigma-delta ADC, the input signal is

sampled at an oversampling frequency $f_s = K \times f_n$ where K is defined as the oversampling ratio and is given by

$$K = f_s / 2f_b$$

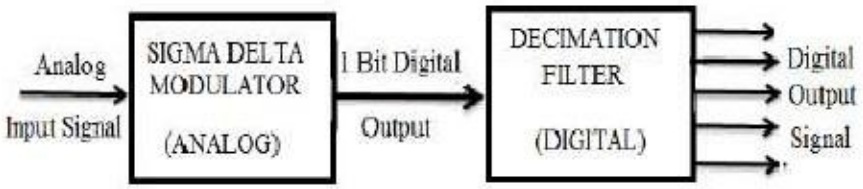


Figure 23: Block Diagram of Sigma-Delta ADC.

Figure 23 depicts the basic blocks of a sigma-delta ADC. It consists of a sigma-delta modulator and a decimation filter. The modulator will be implemented with analog technique to produce a single bit stream and a digital Decimation filter will be implemented to achieve a multi bit digital output thus completing the process of analog to digital conversion.

Quantization Noise -

The analog input signal can take any continuous value. But a digital n-bit signal can only settle to 2n discrete values. It is this difference between the analog value and its digital representation, which causes the distortion known as the quantization noise.

Quantization error is defined as a measure of an n-bit converter's failure to represent precisely an analog signal in the digital domain.

Oversampling, Noise shaping and Digital Filtering -

Oversampling is a process of sampling the input signal at a frequency much greater than the Nyquist frequency (Nyquist frequency, f_n is defined as twice the input signal bandwidth, f_b). This process greatly reduces the quantization noise in the required band. The sampling theorem or the basic Nyquist sample theory states that the sampling frequency of a signal must be at least twice the input signal frequency in order to reconstruct the sampled signal without distortion. Figure

24(a) shows the spectrum of an under sampled signal . Here the sampling frequency, f_s is less than twice the input signal frequency $2f_o$. The shaded portion of the figure shows the aliasing which occurs when the sampling theorem is not followed. We get a distorted signal at the output when a signal contaminated with aliasing is recovered. Figure 24(b) shows the spectrum of an oversampled signal . Here the sampled signal in the frequency domain appears as a series of band-limited signals at multiples of sampling frequency that are widely spaced. This process puts the entire input bandwidth at less than $f_s/2$ which reduces the aliasing.

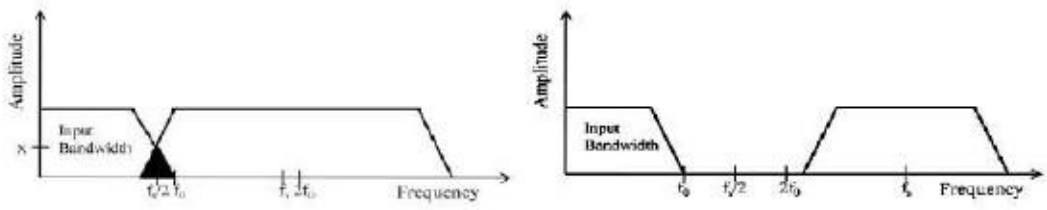


Figure 24(a): Under sampled signal 24(b) Oversampled signal spectrum.

Noise shaping is a property of sigma-delta ADCs resulting from the application of feedback that extends dynamic range. A closed loop modulator works as a high-pass filter for quantizationnoise and as a low-pass filter for the input signal. When the signal is oversampled, the quantization noise power in the Nyquist bandwidth ($f_s/2$) spreads over the wider bandwidth, $Kf_s/2$ where; K is the oversampling ratio, which is shown in Figure 25.The total quantization noise is still the same but the quantization noise in the bandwidth of interest is greatly reduced. The figure also illustrates the noise shaping achieved by using the oversampled sigma-delta modulator.

In a sigma-delta ADC, the analog modulator samples the input at oversampling ratio and after the input signal passes through the modulator it is fed into the digital filter or a decimator. The function of the digital filter is to provide a sharp cutoff at the

bandwidth of interest, which essentially removes out of band quantization noise and signals as shown in Figure 25.

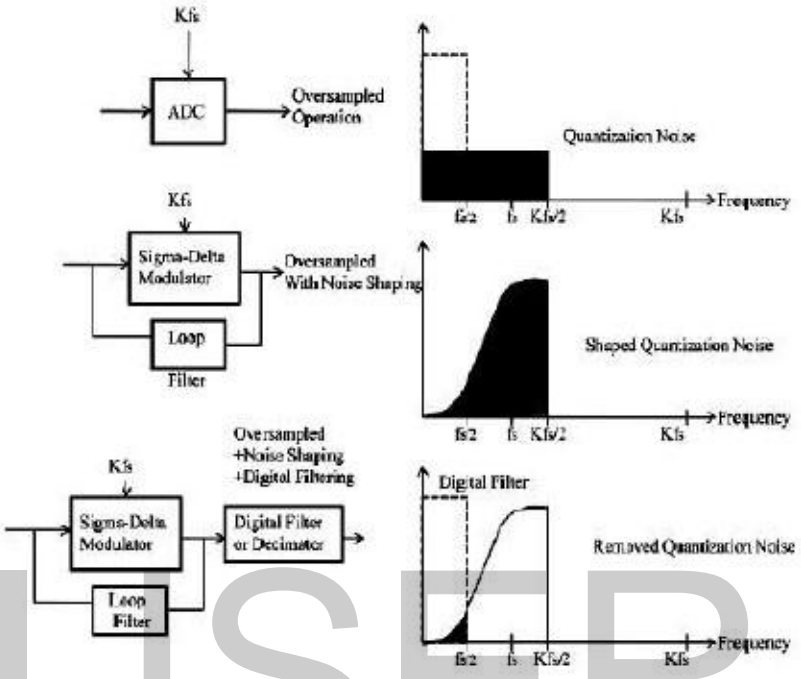


Figure 25: Effect of Noise shaping and Digital Filtering.

CHAPTER – 2

CONCEPT OF PIPELINED ADC

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (Msps) up to 100Msps. Compared to the two-step flash ADC which has just two stages, pipeline ADCs have multiple cascades stages.

Resolutions range from eight bits at the faster sample rates up to 16 bits at the lower rates. These resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (for example, HDTV), xDSL, cable modems, and fast Ethernet.

Applications with lower sampling rates are still the domain of the successive approximation register (SAR) and integrating architectures, and more recently, oversampling/sigma-delta ADCs. The highest sampling rates (a few hundred Msps or higher) are still obtained using flash ADCs. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power in recent years.

Each stage of the pipeline ADC consists of a sample-and-hold circuit, a sub-ADC, a DAC, a subtractor and an inter-stage gain amplifier. The block diagram of a pipeline ADC is illustrated in Figure 26.

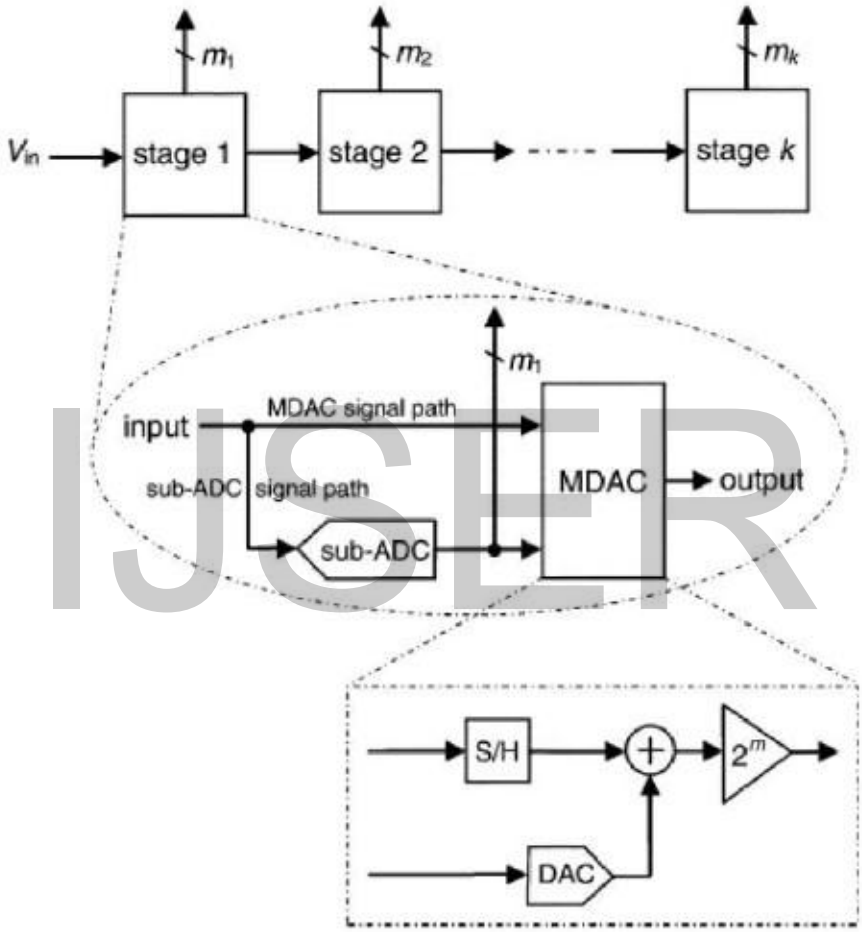


Figure 26 A Pipelined ADC.

In this schematic, the analog input, IN, is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage

one quantizes it to n_1 bits. The n_1 bit output is then fed to a n_1-bit DAC, and the analog output is subtracted from the input.

This "residue" is then gained up by a factor of G_1 and fed to the next stage (Stage 2). This gained-up residue continues through the pipeline, providing ni bits per stage until it reaches the nk-bit flash ADC, which resolves the last Bk bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error correction logic. Note when a stage finishes processing a sample, determining the bits, and passing the residue to the next stage, it can then start processing the next sample received from the sample-and-hold embedded within each stage. This pipelining action is the reason for the high throughput.

The concurrency of the pipeline ADC makes the maximum conversion rate almost independent of the number of stages because the first stage determines the conversion rate, but there is a delay time since the signal must work through all stages before the complete digital outputs are generated. This delay could be an issue if the pipeline ADC is part of a feedback system . In addition, the number of stages does have great impact on the noise performance, power dissipation, linearity and accuracy.

The pipelined ADC is a clocked converter, meaning that the input is sampled and then converted. It is comprised of a series of stages, where the sampled analog signal is clocked trough and gradually converted. Each stage produce a digital output from a sub-ADC of low resolution, which in most cases is based on the °ash structure.

This digital output is then stored in registers until the analog signal has passed through all the stages.

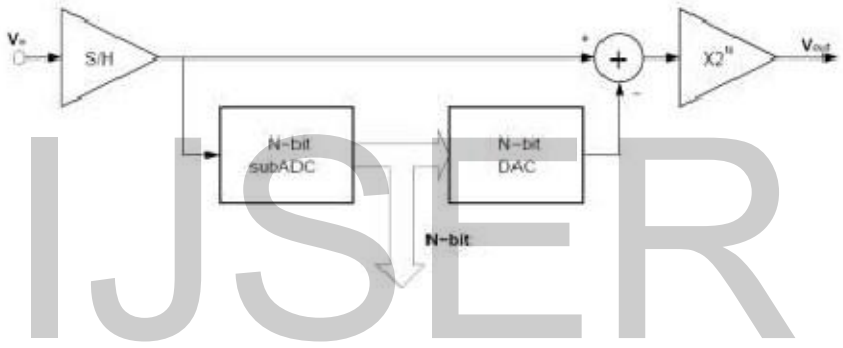


Figure 27: Pipeline stages.

The functionality each individual stage is(as seen in figure 27), first sampling and holding (S/H) the input signal, then preforming a low resolution conversion into digital signals. Which is done by the small °ash subADC. The digital signal is then stored in a delay component and also sent into a DAC and converted back into a analog signal. This analog signal is then subtracted from the original input signal, the resulting residue is lastly multiplied and

put on the output. The multiplication is determined by the number of bits resolution of the subADC.

The advantages of the pipelined structure lies in the predefined latency and high throughput. In most applications such as data transmission, the high latency is not a problem. The pipelined structure will not be a suitable solution if an application needs "near realtime" measurements.

The pipelined structure gives room for many design variations. It is therefore possible to realise an optimal implementation of the design, which meet the given requirements. The design has to balance the tradeoff between speed, power and area consumption. Stage resolution - The most obvious way to implement the 10-bit resolution, would be a two staged pipeline with 5-bit resolution in each stage. This will result in a very low latency, since the signal only has to pass through two stages. However since a predefined latency isn't a big concern in most applications, the advantage of low latency wouldn't compensate for the fact, that the gain bandwidth of the multiplier in each stage has to be very large, in order to realize a multiplication by 32 (2_5). Since it is generally hard to realise a high-gain high-speed amplifier, it would be more sensible to reduce the resolution of the stages.

The most well know implementation of a pipelined ADC is with 3-bit stages . This could be done with three 3-bit stages and a small 1-bit ADC at the end. A improvement of this is the 5-bit design. This however still has the issue with the speed requirements of the multiply by 8 (2_3), even though it is better than the multiply by 32. In relation to area consumption the 5-bit realisation has a smaller overall area consumption, though the individual stage is significantly larger. This is mostly because of the increase in the number of comparators in the subADC component. The overall power consumption will inadvertently be larger with more stages. It is therefore counterproductive in relation to the implementation of a low power design, to have more stages. To gain more speed the resolution of the stages has to be reduced.

A solution to the multiplier problem is to lower the resolution of each stage to 1.5-bit. Then the 1.5-bit stage is basically a 1-bit converter with some redundancy build into. Digital error correction is used in order to compensate for inaccuracies in the components, and give a larger tolerance. This will be covered later.

There is only need for a multiply-by-2 with this 1.5-bit structure. This will significantly lower the requirements for the amplifier, and thereby reducing the complexity of the implementation. Each stage will not take up much area on the wafer. But with a minimum of 6

stages plus a small 1-bit converter at the end of the pipeline, the overall area consumption will be larger than with higher stage resolutions. Also with the higher tolerance, the precision requirements will be less significant.

Design limitations and noise - Though this study does not directly deal with external noise, it cannot be ignored altogether in the overall design, especially when the limitations can end up effecting the final design.

In the pipelined structure, the noise generated in each stage will end up being amplified and feed through to the next state, and thereby lowering the signal to noise ratio (SNR) of the original signal. In a worst case scenario the signal in the later stages will be so degraded, that it is no longer useful. This in turn puts higher requirement upon the linearity of the S/H and the multiplier in each stage and the fact that the amplifiers have finite gain.

The most immediate limitation on this design is offset errors and unlinearity in the stages. In practical designs kT/C thermal-noise and noise from the power supply should also be considered. Charge injection is also something to consider, especially when dealing with transistors implemented as switches. Charge injection occurs when the parasitic capacitance of the transistor is transferred to the ordinary circuits.

General structure - Since inaccuracies in the design is an undeniable reality, there is a need to make the structure robust enough, to insure that these inaccuracies does not affect the functionality of the converter. There are several approaches that could solve most of the problems.

This study focuses on digital error correction and fully differential circuitry, as means of correcting the inaccuracies. In order to incorporate the low power aspect of the requirements, the design implementation will be realised with minimal transistor dimensions and low current flow. Also the use of lower accuracy comparators in the subADCs will reduce power consumption. Because of the pipeline structure most of the signals will not be continuous. The pipelined ADC circuit will therefore be a switch-capacitor implementation.

BASIC CONCEPT OF PIPELINE ADC

The principle of sub-ranging ADC can be pushed to the limit of having only one bit per stage. At this point, each flash ADC is nothing more than a simple comparator; also, the data is transferred in a pipeline fashion: when the data is sent to the second stage, another sampled data is fed to the first stage; the result is a latency delay equal to the

number of stages. Since the pipeline ADC is pipelining the subranging structure, and the binary search in the sub-ADCs runs just as the mathematic division, the first stage decides the MSBs and the last stage sets the LSBs. The MSBs divide the full reference range, while LSBs divide the sub reference range. The relationship between MSBs and LSBs is revealed in Figure 28.

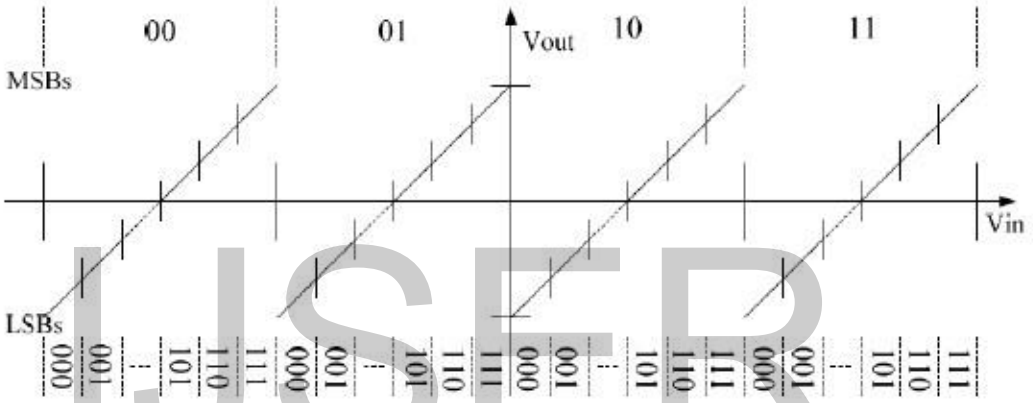


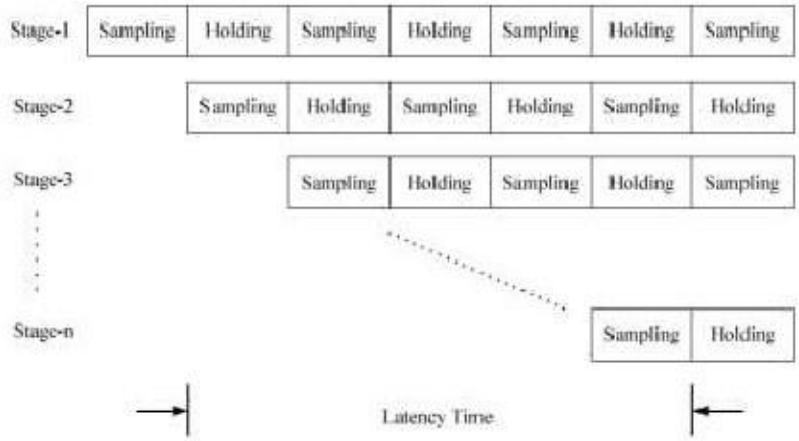
Figure 28 Pipeline ADC Transfer Curve.

A Pipeline ADC consists of a cascade of stages, each of which contains a low resolution ADC, DAC and amplifier, which successively convert the analog input into its digital representation, while processing the data in a pipe-lined manner.

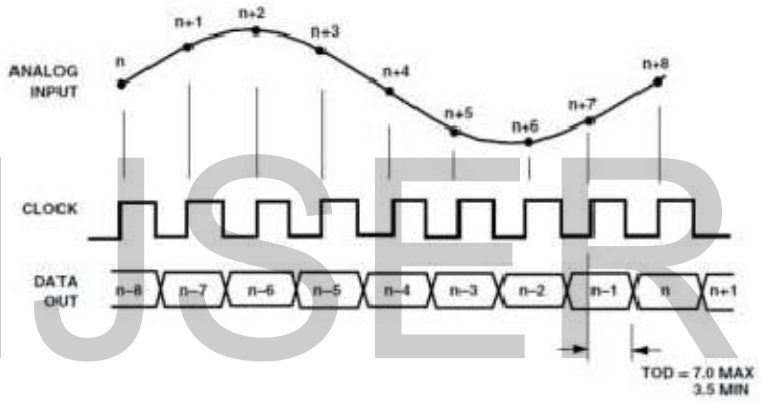
Pipeline ADCs are commonly used for power-efficient high-speed conversion of wide bandwidth input signals (e.g. 10 to 100 MHz). The ADC sampling frequency is usually the Nyquist frequency or

lower using small OSRs (e.g. 2 or 4) and the ADC output code resolution is typically between 8 and 14-bit.

As a well-organized data processing system, the operation of the pipeline ADCs is under stringent timing control. Each stage performs data conversion in sampling and holding modes serially. The sampling and holding modes interleave between two adjacent stages and the digital output is valid after some clock cycles, called latency time, decided by the number of stages. This process is illustrated in Figure 29(a). Because each sample must propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic, data latency is associated with pipelined ADCs. In the example in Figure 29(b), this latency is about seven cycles.



(a)



(b)

Figure 29 (a) Stage Operation Modes in Pipeline ADC (b) data latency in pipeline ADC.

This timing scheme of the pipeline ADC is built up by the sample and hold circuit in each stage. During sampling mode, the switch controlled by the sampling clock is connected to the residue generated from the preceding stage and the signal is sampled on the sampling capacitor. When the hold clock comes, the switch is

turned off and the signal stored on the sampling capacitor on one hand is converted to the thermometer codes by the sub-flash ADC, on the other hand, subtracts the estimated analog signal that is re-constructed by the D/A converter, to create the new residue as the input signal of the following stage. The thermometer codes from each stage are encoded to the binary ones and latched and added together to form the final m-bit digital output (where m is the resolution of the pipeline ADC) .The detailed pipeline architecture is shown in Figure 30.

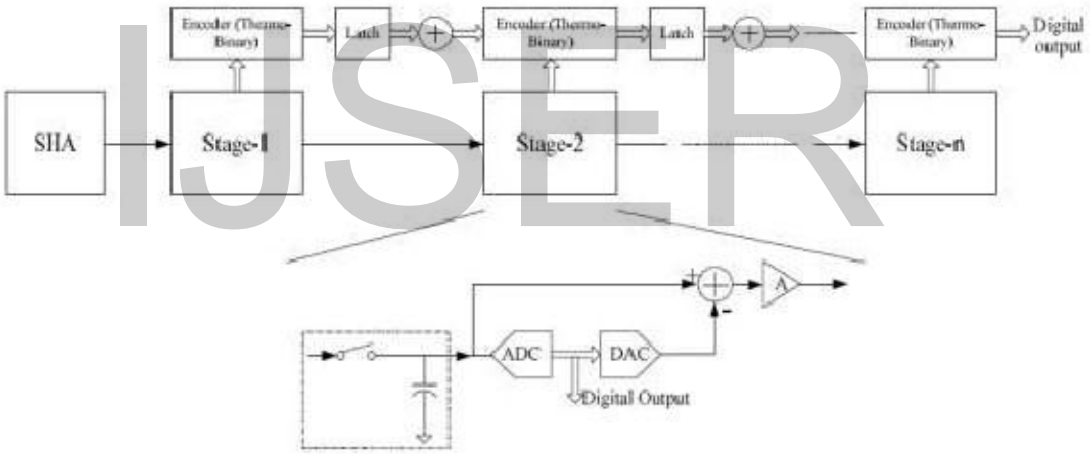


Figure 30 Detailed Pipeline ADC Architecture.

Pipeline ADC design includes system level design and block level design. For system level consideration, it consists of architecture, stages partition, power optimization, specification of sub-block circuits. Designer should consider what kind of architecture the pipeline ADC should be: op-amp sharing, S/H circuits, dithering or

not, how many bit one stage of MDAC should handle, how to minimize power and what the specification of sub-block should be, like op-amp DC gain and close-loop gain bandwidth.

So, it's a complex design trade-off matrix among resolution, thermal noise, power, input range, voltage supply, op-amp types, nonlinearity, and so on. It is shown on Figure 31. This work comes up with an optimized methodology of pipeline ADC design tradeoff and finds all the connection among these important features. For example, as resolution increase, the requirement of thermal noise, which is related to KT/C, also become tight (SNR also increase). So as to minimize thermal noise, the sample capacitance in MDAC will increase; however, it will burn more power. If the input range goes up, the requirement of thermal noise will drop, but the selection of op-amp becomes to be one dominant issue.

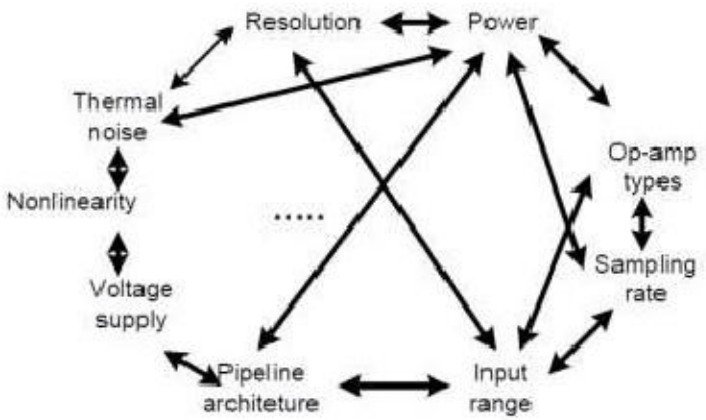


Figure 31 Pipeline ADC Design Matrix.

So, the methodology study of pipeline ADC design flow shows as following figures 32.

1.) Before designing pipeline ADC, first thing to know all the specification of ADC, like resolution, input signal range, maximum sampling rate, voltage supply and so on.

2.) Then, decide what kind of ADC architecture will be used, number of stages, sampling capacitor value.

3.) Define the block level circuits specification based on the first two steps. Like op-amp types, DC gain, closed-loop gain bandwidth, switch selections and so on.

4.) Design and simulation the block level circuits to beat the specification.

5.) Design and simulation the top level ADC.

6.) Run post simulation and corner, Monte Carlo simulation.

7.) If everything passes, the layout could be tape-out.

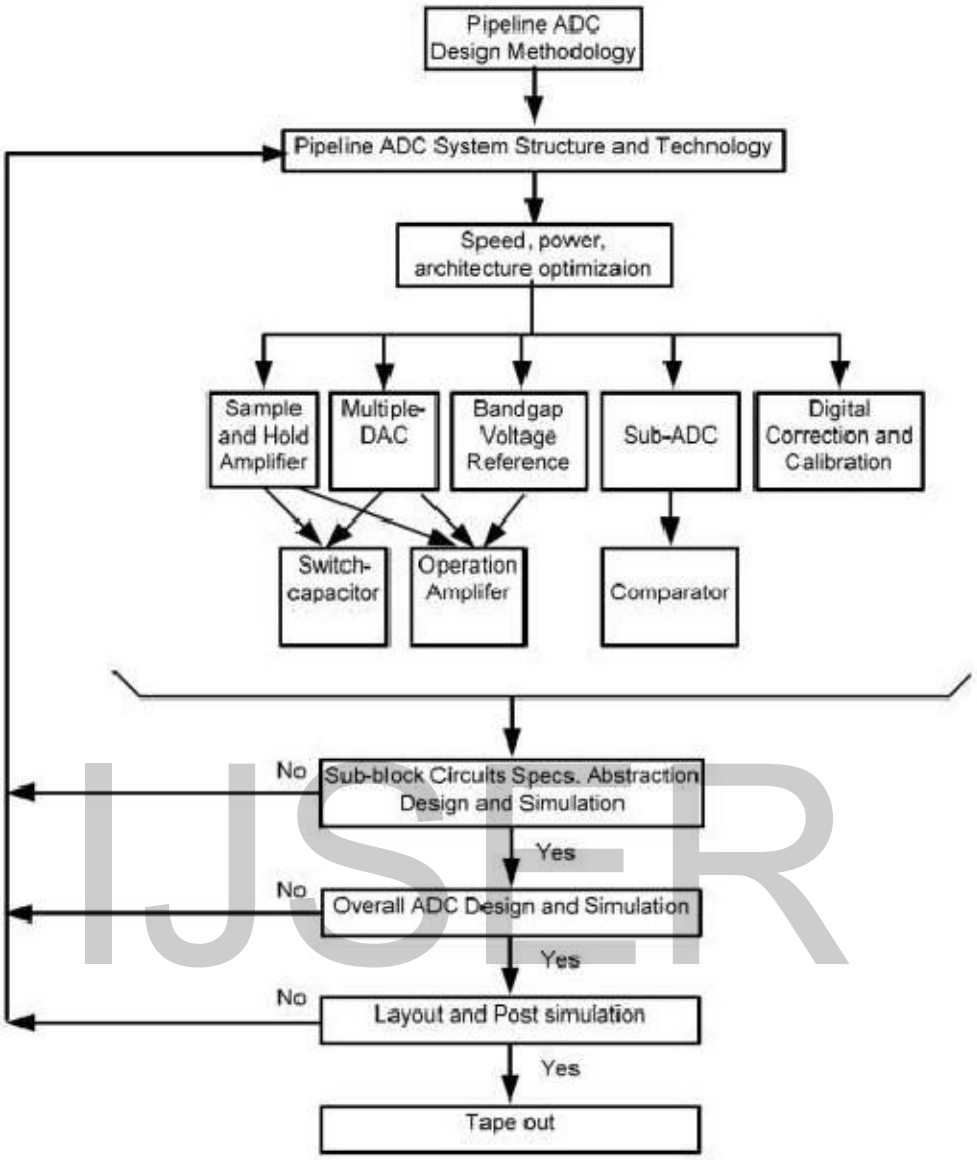


Figure 32 Pipeline ADC Design Flow.

PIPELINED ADC DESIGN REQUIREMENTS

A pipelined ADC architecture offers good trade-off between conversion rate, resolution and power consumption. In this section shows a conventional pipelined ADC architecture. It consists of

several cascaded stages (each resolve n – bit), timing circuits and digital correction block. The concurrent operation of all pipelined stages makes this architecture suitable to achieve very high conversion rates. The overall speed is determined by the speed of the single stage.

MDAC Design Requirements -

MDAC consists of four parts - sample and hold stage, sub-ADC, sub-DAC and subtracting and amplifying stage. All these parts are sources of non-idealities. It is necessary to know important blocks, which have indispensable influence onto overall properties, to achieve good parameters such as resolution, power consumption and speed.

MDAC Resolution - It is a difficult optimization problem to determine the optimal number of bits resolved in each stage. Typically a multi-bit first stage results in lower power consumption and matching and also amplifier gain requirements of the following stages. However the implementation of multi-bit stage possesses two major challenges. First, low feedback factor limits the maximum sampling frequency to low-to-mid rates. Secondly, and more importantly, multi-bit DAC requires several floating switches. These floating switches are a serious impediment to the design of low-voltage SC circuits. Due to this reason a conventional 1.5-bit

stage was employed. The SC technique was utilized in the design of the MDAC to obviate the need for floating switches.

Thermal Noise - Thermal noise is caused by random movement of electrons in resistors. The thermal noise of resistor appears as white noise and its spectral power is

$$\overline{e_R^2} = 4kTR \cdot \Delta f$$

where k is Boltzmann constant, T is the temperature and R is the resistor value.

All particles at temperatures above absolute zero are in random motion. Since elections carry charge, the thermal motion of elections results in a random current that increases with temperature. This noise current is in all circuits and corrupts any signals passing through. The sample and hold circuit is the most important source of noise in pipelined .ADC. Two noise sources are significant in the sample and hold circuit: the sampling switches and the sample and hold amplifier. The sampling switch is used to sample the input signal onto a sampling capacitor. When the input signal is sampled, noise from the sampling switch is sampled by the sampling capacitor as well.

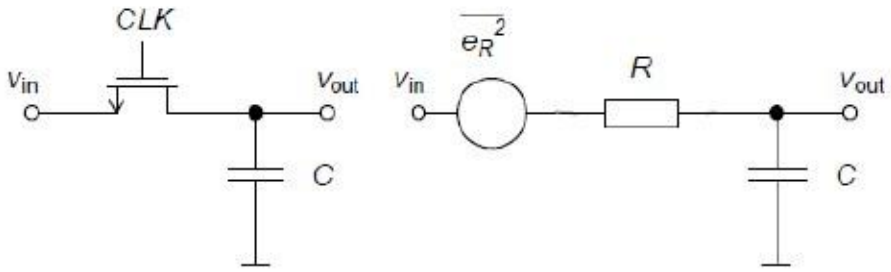


Fig. 33. Simple MOS sampling circuit and its equivalent circuit with on-resistance and thermal noise.

Comparator Offset - The offset voltage of comparators (Fig.34) is main source of errors in the sub-ADC of pipelined ADC.

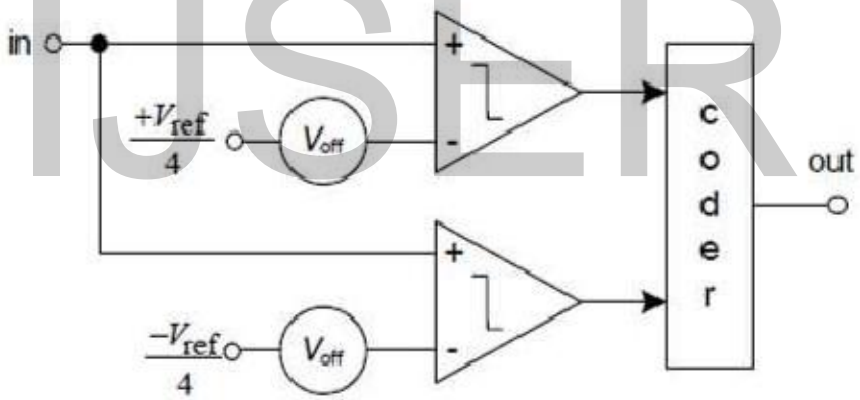


Fig. 34. Comparator offset in sub-ADC'.

A comparator produces an output signal indicating whether or not an input signal is larger than a reference level. When the comparator computes the difference between two input signals, an internal offset voltage is added to this difference. Thus, when the two inputs are close together, the comparator may make an

incorrect decision. When the comparator makes wrong decision, the output code is incorrect, and the incorrect reference is subtracted from the input. The result is residue that is out of range of the next stage of the pipeline when amplified.

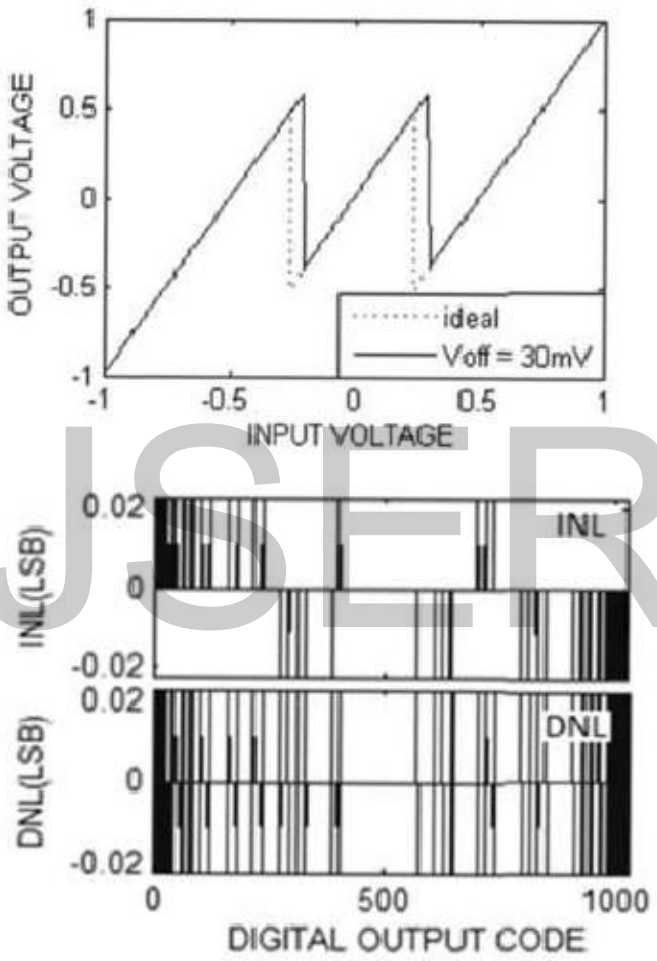


Fig. 35. The effect of comparator offset.

The effect of offset error in comparator on 1.5-bit stage transfer function is shown in Fig. 35. The clotted line represents ideal transfer function and the full line shows transfer function with

offset voltage in comparator. The INL and DNL of the 10-bits pipelined ADC are small for comparator offset 30 mV (all comparators in ADC) thank to RSD (redundant signed digit) collection .

PIPELINED ADC ERROR MODELS

There are many different circuit effects that can create static non-linearities in pipelined ADCs. Following is a discussion of the dominant sources.

Finite Opamp Gain-

When an opamp-based architecture is used to realize the charge transfer in a pipelined ADC, there will be an error in the virtual ground condition due to the finite DC gain A of the opamp. This error can be expressed as

$$v_X = -\frac{v_O}{A}.$$

Substituting this into Equation 1.2 and solving for v_G when $C_1=C_2$yields

$$v_O = \frac{2v_I - dV_{ref}}{1+\frac{2}{A}}.$$

This can be rewritten as

$$v_O = \frac{2v_I - dV_{ref}}{1 + \epsilon_{op}},$$

where $\epsilon_{op} = \frac{2}{A}$. Finite opamp gain causes a gain reduction in pipeline stage transfer function as shown in the plot of Figure 36. The solid line represents the transfer function with finite opamp gain and the dashed line is the ideal transfer function where the gain is exactly 2. In the second plot of Figure 36, the ADC transfer

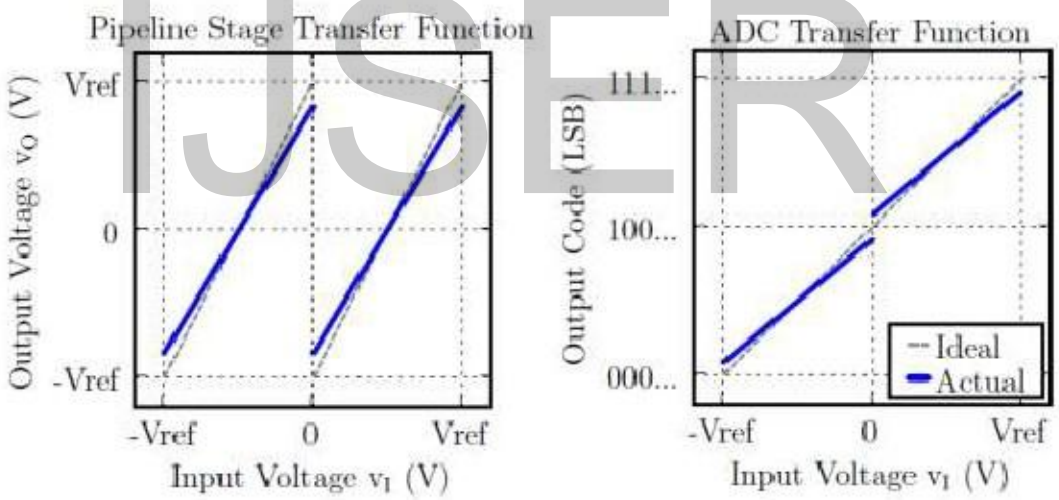


Figure 36: Single stage and ADC transfer function from finite op-amp gain or finite current source output impedance.

function is shown for the case of finite opamp gain only effecting the first stage. The result is a static non-linearity in the form of a missing code gap at the bit decision boundary. The amount of gain

reduction and thus the size of the missing code gap is a function of the DC gain A of the opamp, and thus one must design the opamp with sufficient gain to meet the desired resolution.

Finite Current Source Output Impedance -

When CBSC circuits are used to realize the charge transfer then the finite output impedance of the current source and the finite delay of the comparator will produce an effect that is very similar to finite gain in an opamp based circuit.

Capacitor Mismatch -

Capacitor mismatch results when the capacitor ratios deviate from their desired value due to variation inherent in manufacturing. Capacitor mismatch can cause both dieto-die variation from random etching variation and systematic variation from mask and structural density variation.

Bit Decision Comparator Offset -

When the bit decision comparator has positive offset, it produces the result plotted and negative offset produces the results. Because the stage output voltage goes out of range, the ADC transfer function has a wide code and missing codes at the bit decision boundary.

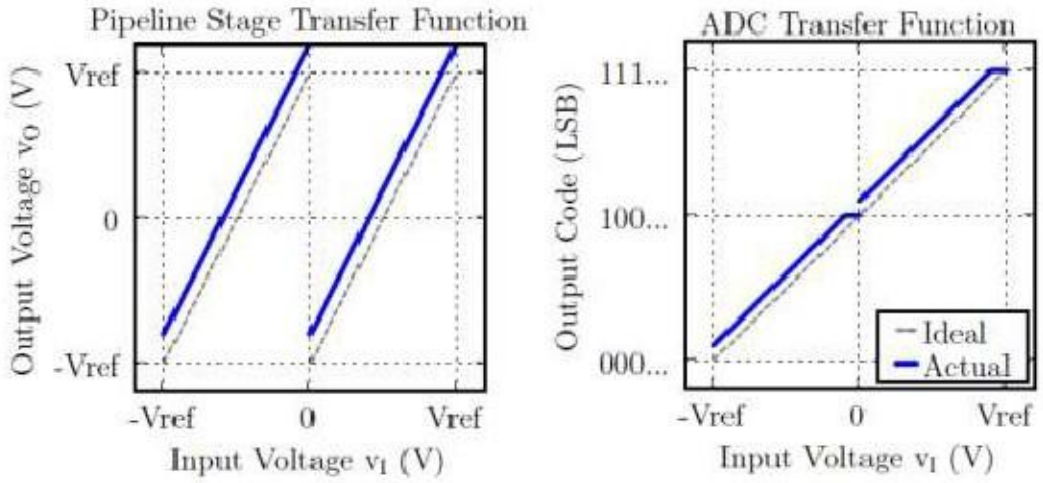


Figure 37: Single stage and ADC transfer function from positive charge injection or stage transfer offset.

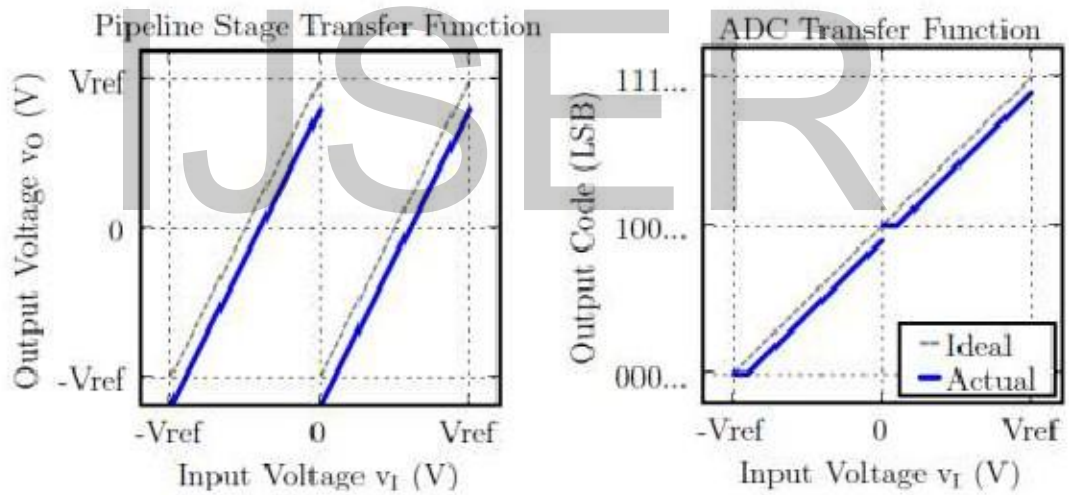


Figure 38: Single stage and ADC transfer function from negative charge injection or stage transfer offset.

Errors from Multiple Stages -

The preceding examples showed the ADC transfer function when only the first stage had the static non-linearity and assumed the remaining stages were ideal. The effect of each additional stage, however, will also manifest itself as shown in the ADC transfer function where the first two stages are given the same low finite opamp gain. The missing code gap from the first stage is the largest and in the middle. The missing code gap from the second stage further divides each segment

and produces a gap half the size of that from the first stage. The missing code gap from each additional stage will continue to be half that of the previous stage and further subdivide each segment.

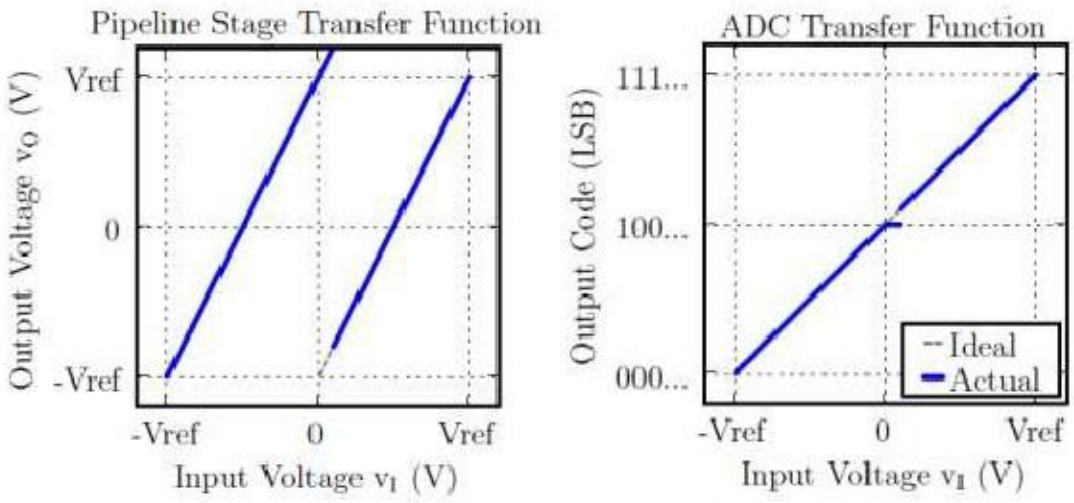


Figure 39: Single stage and ADC transfer function from a positive bit decision comparator offset.

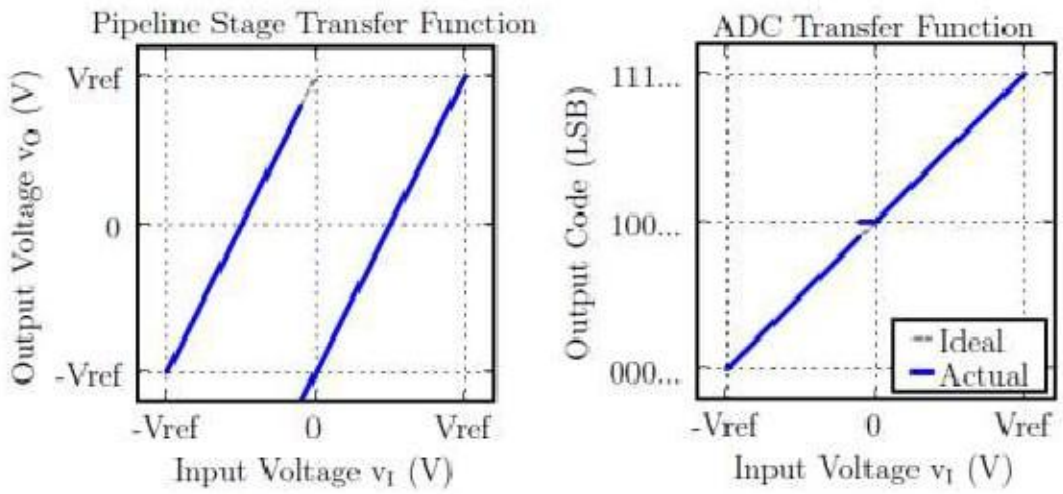


Figure 40: Single stage and ADC transfer function from a negative bit decision comparator offset.

PIPELINED ADC VERSUS OTHER ADCS

Versus SAR –

In a successive approximation register (SAR) ADC, the bits are decided by a single high-speed, highaccuracy comparator bit by bit, from the MSB down to the LSB. The SAR ADC compares the analog input with a DAC, whose output is updated by previously decided bits and successively approximates the analog input. This serial nature of SAR limits its operating speed to no more than a few Msps, and still slower for very high resolutions (14 to 16 bits). A pipelined ADC, however, employs a parallel structure in which each stage works on 1 to a few bits (of successive samples) concurrently. Although there is only one comparator in a SAR, this

comparator must be fast (clocked at approximately the number of bits x the sample rate) and as accurate as the ADC itself. In contrast, none of the comparators inside a pipelined ADC needs this degree of speed or accuracy.

A pipelined ADC, however, generally requires significantly more silicon area than an equivalent SAR. A SAR also displays a latency of only one cycle (one cycle = 1/Fsample), versus about three or more cycles in a typical pipeline ADC. As with a pipeline, a SAR with more than 12 bits of accuracy usually requires some form of trimming or calibration.

Versus Flash -

Despite the inherent parallelism, a pipelined ADC still requires accurate analog amplification in DACs and interstage gain amplifiers, and thus significant linear settling time. A purely flash ADC, however, has a large bank of comparators, each consisting of wideband, low-gain preamps followed by a latch. The preamps, unlike those amplifiers in a pipelined ADC, must provide gains that do not need to be linear or accurate; only the comparators' trip points must be accurate. As a result, a pipelined ADC cannot match the speed of a well-designed flash ADC.

Extremely fast 8-bit flash ADCs (or their folding/interpolation variants) do exist with sampling rates as high as 1.5Gsps (for example, the MAX104/MAX106/MAX108). It is much harder to find a 10-bit flash, while 12-bit (or above) flash ADCs are not commercially viable products. This is simply because in a flash ADC the number of comparators increases by a factor of 2 for every extra bit of resolution; simultaneously, each comparator must be twice as accurate. In a pipeline, however, to a first order the complexity only increases linearly, not exponentially, with the resolution.

At sampling rates obtainable by both pipeline and flash converters, a pipelined device usually has much lower power consumption than a flash. A pipeline ADC is typically less susceptible to comparator metastability. Comparator metastability in a flash can lead to sparkle-code errors, a condition in which the ADC provides unpredictable, erratic conversion results.

Versus the Sigma-Delta Converter -

Traditionally, oversampling/sigma-delta-type converters commonly used in digital audio have a limited bandwidth of about 22kHz. Recently some high-bandwidth sigma-delta converters reached a bandwidth of 1MHz to 2MHz with 12 to 16 bits of resolution. These specifications indicate very high-order sigmadelta modulators (for

example, fourth or even higher) incorporating a multi-bit ADC and multi-bit feedback DAC. Their main applications are in ADSL. A sigma-delta converter needs no special trimming/calibration, even for 16 to 18 bits of resolution. They also require no steep rolling-off anti-alias filter at the analog inputs, because the sampling rate is much higher than the effective bandwidth. The backend digital filters take care of that task. The oversampling nature of the sigma-delta converter also tends to "average out" any system noise at the analog inputs.

Sigma-delta converters trade speed for resolution. The need to sample many times (for example, at least 16 times, but often much higher) to produce one final sample causes the internal analog components in the sigma-delta modulator to operate much faster than the final data rate. The digital decimation filter is also nontrivial to design, and consumes a lot of silicon area. The fastest, high-resolution sigma-deltatype converters are not expected to have more than a few MHz of bandwidth in the near future. Like pipelined ADCs, sigma-delta converters also have latency.

Versus Half- (Two-Step) Flash -

A two-step flash converter can be generalized as a two-stage pipeline device. As the number of bits increases (for example, 12 bits or higher) with digital error correction, however, each stage

would need to incorporate a 6- to 7-bit flash ADC. The interstage gain amplifier would also need very high gain. Therefore, for higher resolution, it is wiser to use more than two stages.

PARALLEL PIPELINE ARCHITECTURE

When even higher conversion speed is desired, parallelism needs to be applied. Figure 41 shows a system view of the architecture for parallel pipeline A/D. If N channels are used, each channel is operated at frequency of fs/N, where fS is the system overall sampling frequency. An analog multiplexor and a digital multiplexor are used at the input and the output of the system. This way throughput of the system is increased by N times at the cost of increasing hardware. Since the DAC reference can be shared by all the channels, the hardware increase in less than the first order linear dependence. Sharing DAC reference is also desired to improve the matching of the channels.

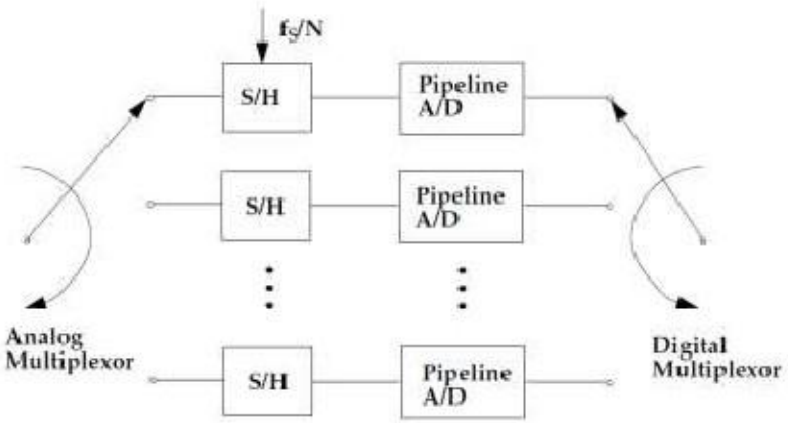


Fig. 41. A System View of Parallel Pipeline A/D Architecture.

In Figure 42, an example of the clock scheme of a 4-channel parallel pipelined A/D system is shown. It's based on the concept of time-interleave. The sampling instant of each S/H in each channel is shifted by a quarter of the clock period. The arrows show a full cycle of the operation through the four channels.

The most critical problem that needs to be solved in parallel pipeline structure is how to improve the matching between channels. This directly affect the highest resolution we can achieve. Past work shows 8-bit resolution at 85Mhz sampling rate can be achieved.

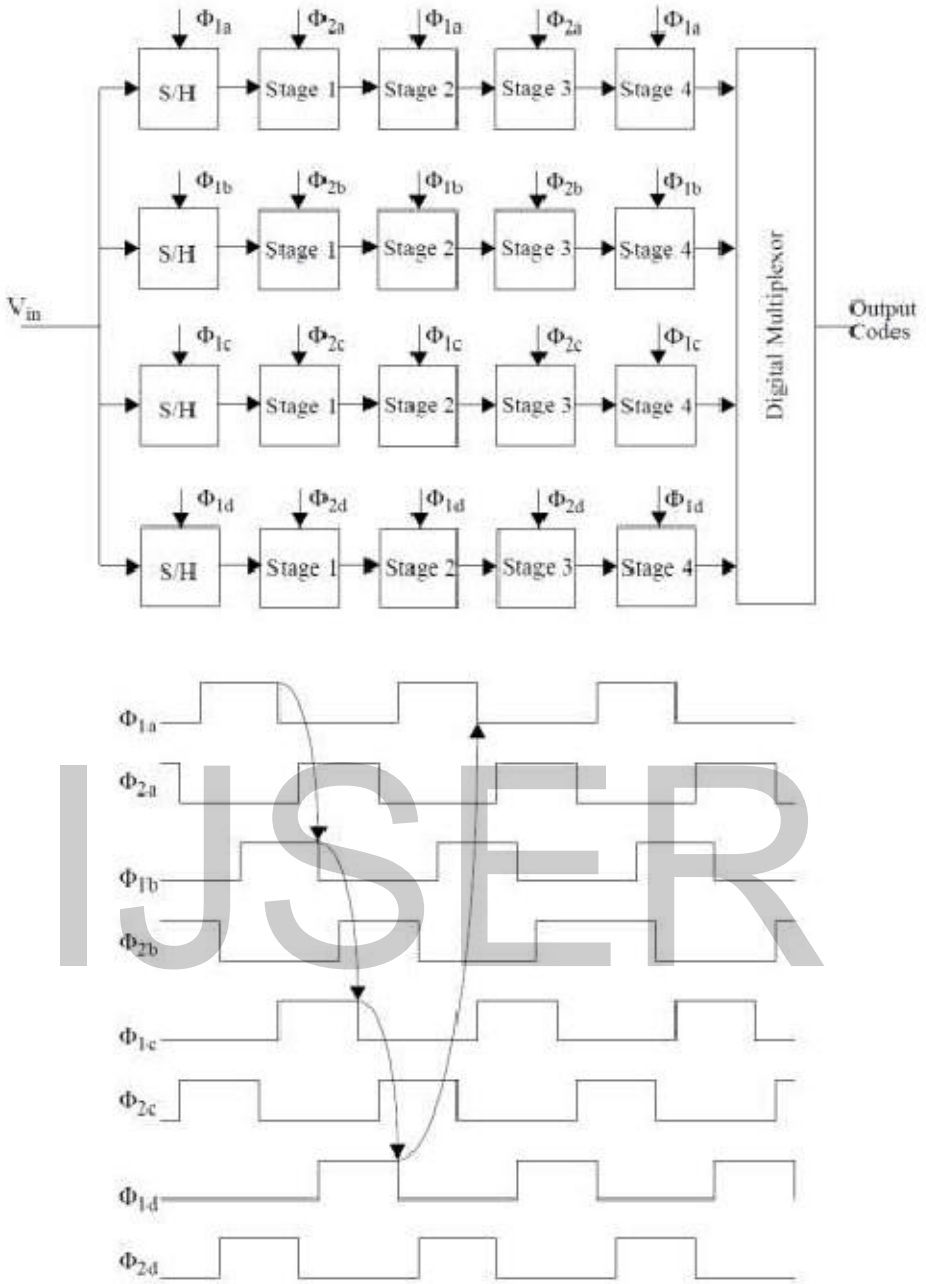


Fig. 42. A four-channel parallel pipeline A/D clocking example.

CHAPTPER – 3

DESIGN FACTORS FOR HIGH PERFORMANCE SAR ADC

Successive-approximation-register (SAR) analog-to-digital converters (ADCs) are frequently the architecture of choice for medium-to-high-resolution applications with sample rates under 5 megasamples per second (Msps). Resolution for SAR ADCs most commonly ranges from 8 to 16 bits, and they provide low power consumption as well as a small form factor. This combination of features makes these ADCs ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition.

As the name implies, the SAR ADC basically implements a binary search algorithm. Therefore, while the internal circuitry may be running at several megahertz (MHz), the ADC sample rate is a fraction of that number due to the successive-approximation algorithm. The two critical components of a SAR ADC are the comparator and the DAC. As we shall see later, the track/hold can be embedded in the DAC and, therefore, may not be an explicit circuit. A SAR ADC's speed is limited by:

The settling time of the DAC, which must settle to within the resolution of the overall converter, for example, ½ LSB. The comparator, which must resolve small differences in V_{IN} and V_{DAC} within the specified time

The DAC -

The maximum settling time of the DAC is usually determined by its MSB settling. This is simply because the MSB transition represents the largest excursion of the DAC output. In addition, the linearity of the overall ADC is limited by the linearity of the DAC. Therefore, because of the inherent componentmatching limitaions, SAR ADCs with more than 12 bits of resolution will often require some form of trimming or calibration to achieve the necessary linearity. Although it is somewhat process-and-designdependent, component matching limits the linearity to about 12 bits in practical DAC designs.

Many SAR ADCs use a capacitive DAC that provides an inherent track/hold function. Capacitive DACs employ the principle of charge redistribution to generate an analog output voltage. Because these types of DACs are prevalent in SAR ADCs, it is beneficial to discuss their operation.

A capacitive DAC consists of an array of N capacitors with binary weighted values plus one "dummy LSB" capacitor. Figure 43 shows

an example of a 16-bit capacitive DAC connected to a comparator. During the acquisition phase, the array's common terminal (the terminal at which all the capacitors share a connection, see Figure 43) is connected to ground and all free terminals are connected to the input

signal (analog in or VIN). After acquisition, the common terminal is disconnected from ground and the free terminals are disconnected from VIN, thus effectively trapping a charge proportional to the input

voltage on the capacitor array. The free terminals of all the capacitors are then connected to ground, driving the common terminal negative to a voltage equal to -VIN.

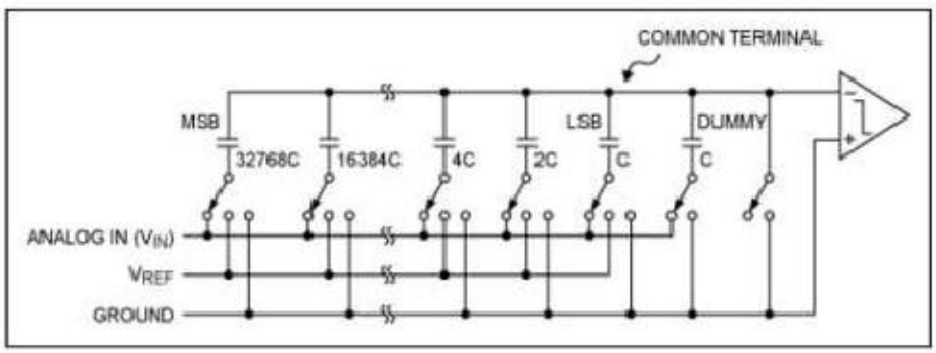


Figure 43. A 16-bit example of a capacitive DAC.

As the first step in the binary search algorithm, the bottom plate of the MSB capacitor is disconnected from ground and connected to

VREF- This drives the common terminal in the positive direction by an amount equal to $\frac{1}{2}V_{REF}$ Therefore,

$$V_{COMMON} = -V_{IN} + \frac{1}{2} \times V_{REF}$$

The comparator output yields a logic 1 if $V_{COMMON} < 0$ (i.e., $V_{IN} > \frac{1}{2} \times V_{REF}$). The comparator output yields logic 0 if $V_{IN} < \frac{1}{2} \times V_{REF}$ If the comparator output is logic 1, then the bottom plate of the MSB capacitor stays connected to VREF. Otherwise, the bottom plate of the MSB capacitor is connected back to ground.

The bottom plate of the next smaller capacitor is then connected to VREF and the new VCOMMON voltage is compared with ground.

This continues until all the bits have been determined. In general,

$$V_{COMMON} = -V_{IN} + B_{N-1} \times V_{REF}/2 + B_{N-2} \times V_{REF}/4 + B_{N-1} \times V_{REF}/8 + \ldots + B0 \times V_{REF}/2^{N-1}$$

(B_ comparator output/ADC output bits).

DAC Calibration -

In an ideal DAC, each of the capacitors associated with the data bits would be exactly twice the value of the next-smaller capacitor. In high-resolution ADCs (for example, 16 bits), this results in a range of values too wide to be realized in an economically feasible size. The 16-bit SAR ADCs like the MAX195 use a capacitor array that actually consists of two arrays capacitively coupled to reduce the LSB array's

effective value. The capacitors in the MSB array are production trimmed to reduce errors. Small variations in the LSB capacitors contribute insignificant errors to the 16-bit result. Unfortunately, trimming alone does not yield 16-bit performance or compensate for changes in performance due to changes in temperature, supply voltage, and other parameters. For this reason, the MAX195 includes a calibration DAC for each capacitor in the MSB array. These DACs are capacitively coupled to the main DAC output and offset the main DAC's output according to the value on their digital inputs.

During calibration, the correct digital code to compensate for the error in each MSB capacitor is determined and stored. Thereafter, the stored code is provided to the appropriate calibration DAC whenever the corresponding bit in the main DAC is high. This compensates for errors in the associated capacitor. Calibration is

usually initiated by the user or done automatically on power-up. To reduce the effects of noise, each calibration experiment is performed many times (about 14,000 clock cycles in the MAX195), and the results are averaged. Calibration is best performed when the power-supply voltages are stable. High-resolution ADCs should be recalibrated any time that there is a significant change in supply voltages, temperature, reference voltage, or clock characteristics, because these parameters

affect the DC offset. If linearity is the only concern, much larger changes in these parameters can be tolerated. Because the calibration data is stored digitally, there is no need to perform frequent conversions to maintain accuracy.

The Comparator -

The requirements of the comparator are speed and accuracy. Comparator offset does not affect overall linearity as it appears as an offset in the overall transfer characteristic. In addition, offset-cancellation techniques are usually applied to reduce the comparator offset. Noise, however, is a concern, and the comparator is usually designed to have input-referred noise less than 1 LSB. Additionally, the comparator needs to resolve voltages within the accuracy of the overall system. It needs to be as accurate as the overall system.

Digital control systems are extensively used in the field of motion control. High performance digital control systems have created a need for high speed and high resolution ADCs with extremely wide dynamic range. Typically highresolution ADCs have been based either on self-calibrated SAR or over sampling architectures . But both of these architectures are unsuitable for high speed applications. Two step flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation . However, beyond such resolution, the area and power dissipation of two-step flash ADCs nearly double for each additional bit of resolution . Different architectures like pipelined convertor , SAR convertor , Sigma-Delta convertor , folding ADCs , reported recently for high speed applications. But these architectures have significant amount of complexity. In this study a simple technique for enhancing conversion

speed of SAR ADC is proposed.

With the improvement of system-on-chip (SoC) technology, A/D converters are widely used. SAR A/D converters are especially popular for SoC design due to their simple architectures, small areas and eaziness to be integrated with other IC blocks. Either charge redistribution or voltage scaling method can be used to

implement the internal D/A converter, which is an essential part of the SAR A/D converter. However, for these two types of SAR A/D converters, with the resolution increasing, the total number of passive components in their D/A converters will also increase exponentially. So many resistors or capacitors make it difficult for them to occupy a small area. For a voltage scaling SAR A/D converter with more than 8-bit resolution, high performance is always hard to achieve due to the correspondingly bad matching performance of resistors, which makes it unpopular for embedded SoC applications .810•. For a charge redistribution SAR A/D converter, to reduce the chip area, small capacitors must be used. But additional calibration techniques should be utilized to guarantee the linearity of the converter, thus increasing the total power dissipation and circuit complexity. With silicon feature dimensions downscaling into the nanometer scale, more stringent requirements such as low power and small area must be satisfied simultaneously for data converters in SoC applications. But for most previous works, it is hard for them to satisfy these requirements simultaneously.3; 5•. Therefore, research is still needed on high performance SAR A/D converters.

In this study, by using an R-C hybrid architecture D/A converter, pseudo-differential comparison architecture, and low power voltage level shifters, a 10-bit SAR A/D converter is realized based on 90

nm CMOS logic process. With the combination of a 7-bit resistor ladder and an 8:1 capacitor pair, 10-bit resolution is achieved. Due to the inherent sample and hold function of the capacitor, no additional S/H circuit is needed.

Good matching performance is achieved by careful layout design where the resistor ladder is sided by dummies, and the capacitor array is routed with a common-central symmetry method. The measurement results show that this proposed converter achieves high performance and it is very suitable for multi-supply embedded SoC applications.

SAR ADC ARCHITECTURE

Although there are many variations for implementing a SAR ADC, the basic architecture is quite simple (see **Figure 44).** The analog input voltage (VIN) is held on a track/hold. To implement the binary search

algorithm, the N-bit register is first set to midscale (that is, 100... .00, where the MSB is set to 1). This forces the DAC output (V_{DAC}) to be VREF/2, where VREF is the reference voltage provided to the ADC.

A comparison is then performed to determine if VIN is less than, or greater than, V_{DAC}. If VIN is greater than VDAC, the comparator output is a logic high, or 1, and the MSB of the N-bit register remains at 1. Conversely, if VIN is less than V_{DAC}, the comparator output is a logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the N-bit digital word is available in the register.

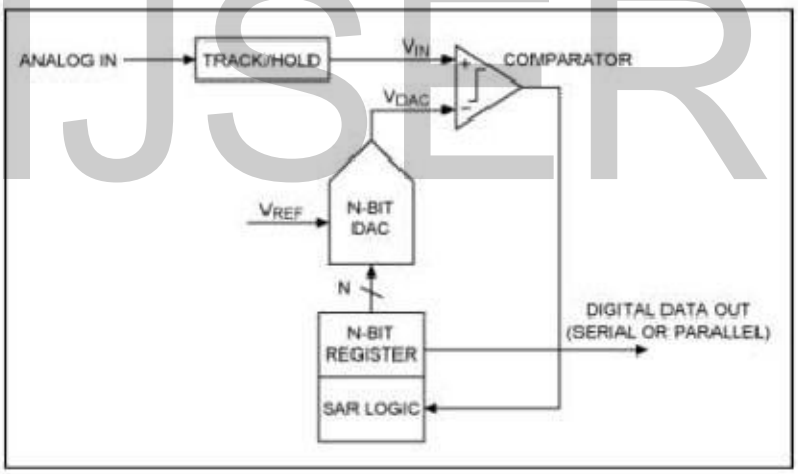


Figure 44. Simplified N-bit SAR ADC architecture.

Figure 45 shows an example of a 4-bit conversion. The y-axis (and the bold line in the figure) represents the DAC output voltage. In the example, the first comparison shows that $V_{IN} < V_{DAC}$. Thus, bit 3 is set

to 0. The DAC is then set to 0100_2 and the second comparison is performed. As $V_{IN} > V_{DAC}$, bit 2 remains at 1. The DAC is then set to 0110_2, and the third comparison is performed. Bit 1 is set to 0, and the DAC is then set to 0101_2 for the final comparison. Finally, bit 0 remains at 1 because $V_{IN} > V_{DAC}$.

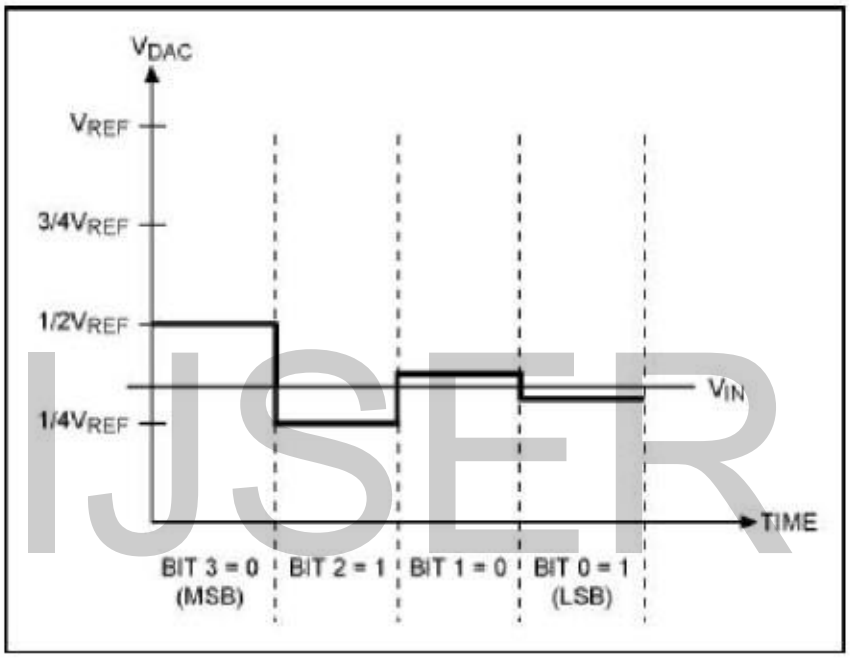


Figure 45. SAR operation (4-bit ADC example).

Notice that four comparison periods are required for a 4-bit ADC. Generally speaking, an N-bit SAR ADC will require N comparison periods and will not be ready for the next conversion until the current one is complete. This explains why these ADCs are power- and space-efficient, yet are rarely seen in speedand-resolution combinations beyond a few mega-samples per second (Msps) at 14

to 16 bits. Some of the smallest ADCs available on the market are based on the SAR architecture. The MAX1115/MAX1116 and MAX1117/MAX1118 8-bit ADCs and their higher resolution counterparts, the MAX1086 and the

MAX1286 (10 and 12 bits, respectively), fit in tiny SOT23 packages measuring 3mm x 3mm.

There is another notable feature of SAR ADCs: power dissipation scales with the sample rate. This contrasts with flash or pipelined ADCs which usually have constant power dissipation versus sample rate. This scaled power dissipation is especially useful in low-power applications or applications where the data acquisition is not continuous (for example, PDA digitizers).

BASIC PRINCIPLE OF SAR ADC

A typical SAR A/D converter is illustrated in Fig. 46. It consists of an S/H circuit, a comparator, a SAR control unit and a D/A converter. Its operation is based on a “binary search” algorithm. The analog input is sampled and compared with the output of the D/A converter, which is under the control of the logic circuit. The reference voltage at particular stages depends on the value of the calculated bit. The reference voltage is calculated with the formula:

$$b_{n-1}V_{ref}/2^1 + b_{n-2}V_{ref}/2^2 + b_{n-3}V_{ref}/2^3 + \cdots + b_0 V_{ref}/2^n$$

, where n is the resolution of the convener. The digital outputs can then be sequentially generated by these comparisons.

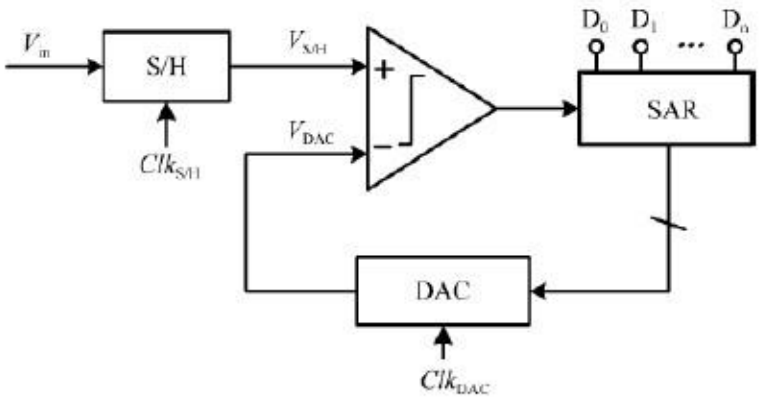


Fig. 46. Typical SAR ADC architecture.

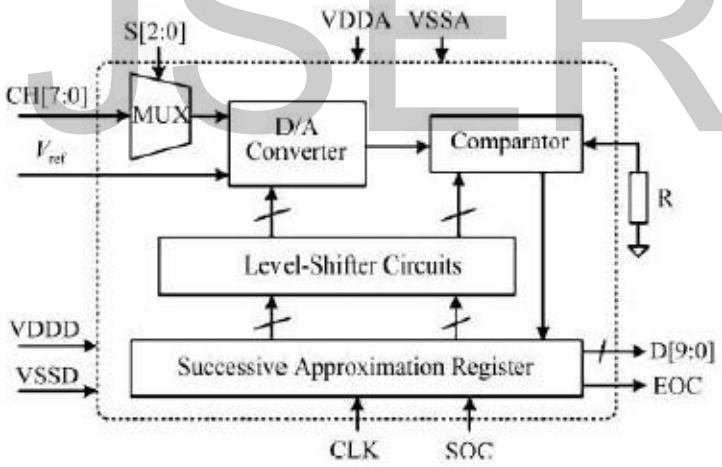


Fig. 47. Functional block diagram of the proposed SAR ADC.

CALIBRATION TECHNIQUES

Comparator offset calibration have been widely researched by the academic and industry. Among recent comparator offset calibration

techniques, an approach using capacitors with dynamic collection to adjust the output loads of comparators degrades the response. Another approach using capacitors to control current for offset cancellation requires refreshing for the capacitors to maintain the charge against the leakage. This work proposes a dynamic offset control technique based on charge compensation by timing adjustment. The charge injection and clock feed- through results from turning off the latch reset transistor are investigated. These two effects are generally considered as limitations to the accuracy performance of the analog CMOS circuits since they introduce error voltages to the surrounding sampling node.

As for the CD AC. the calibration technique is also required for most of the ADC blocks. Analog calibration techniques use analog components in the signal path to generate higher linearity at the expense of conversion speed. On the other hand, digitally assisted calibration techniques, which compensate for ADC mismatch, are reported. For example, is able to correct the linearity as well as radix error,

but it needs two times conversion, resulting in the conversion rate into half. The trade off between compensated performance and the costs, area, power, sacrificed performance and convergent time, needs to be considered. This work proposed an on chip histogram-

based digitally assisted technique to compensate for CDAC mismatch with a minimum cost. The calibration is performed using the input signal, watching the data stream to find the missing or wide code at ADC output, judge and feed back to the compensation capacitor so as to relax the nonlinearity suffer from the CDAC mismatch. The calibration does not require special input signal and extra analog hardware and offset-free comparator as well.

On the other hand, digital calibration techniques, which can realize the benefit of technology scaling in terms of energy efficiency and speed, have also been developed. They can be classified into two groups: foreground calibration and background calibration. Foreground calibration is done during a calibration phase at startup, measuring nonlinearity by driving the inputs with specific calibration signals to extract the mismatch information. For example, Lee et al developed a self-calibrated capacitor array in a SAR ADC, exploiting a binary weighted capacitor array. During calibration, the ratio errors of the capacitors are measured sequentially from the MSB capacitor to the LSB capacitor. The mismatch data is stored in a RAM. During the normal operation, the mismatch data is used to correct matching errors of the capacitor array. Other calibration schemes use statistically-based methods to extract nonlinearities based on histogram measurements or code density. Because these calibration schemes

require collection of measurement data at the beginning of the operation, they interrupt the normal operation of the ADC. To minimize the effect, it is typical to run these calibration schemes during manufacturing or at startup, meaning that they cannot track parameter drifts.

In contrast, digital background calibration runs transparently in the background so it does not interrupt the normal conversion process. A common approach is to inject a known calibration signal, δ_a, onto the signal path. Assuming the corresponding digitized output for the injected calibration signal δ_a is δ_d, with an ideal linear transfer function, a constant shift of δ_d in its output, independent of the input signals, is expected. In other words, when δ_d is subtracted from the final digitized output, there should be no correlation between the injected signal and the output signal. The calibration engine is, therefore, designed to null such correlation by adjusting the calibration parameters. Using this approach, because the signal path must accommodate the addition of the calibration signal, the signal range and the over-range protection is reduced in the design, in which the headroom may be already limited. Moreover, the effectiveness of calibration also depends on the matching between δ_a and δ_d Rather than tampering

with the input signal path, another approach uses the input signal itself to estimate the static errors without using a calibration signal. Adaptive equalization techniques, prevalent in the digital communication community, are used to resolve nonlinearity problems for pipelined and SAR ADCs, respectively. These techniques typically require an accurate reference ADC to estimate and correct the errors. Even though the reference ADC may run at a slower speed compared with the core ADCs, the added complexity associated with the implementation translates into either higher power consumption or reduction in conversion speed. In summary, the previous techniques are to different degrees either hardware or algorithmically expensive.

SELF CALIBRATION OF SAR ADC

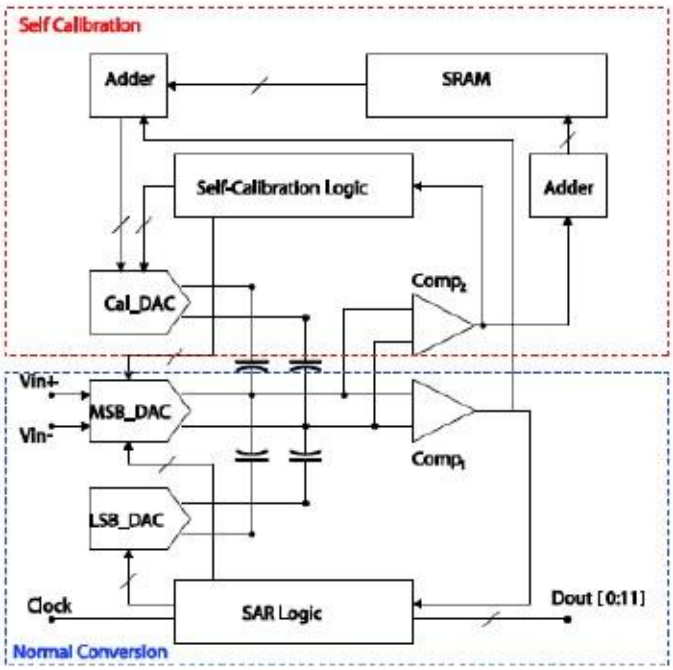


Fig. 48. The architecture of self-calibrated ADC.

Fig. 48 shows the block diagram of the self-calibrated SAR ADC. The ADC consists of two comparators, a main DAC (splitting to MSB DAC and LSB DAC), a calibration DAC, SAR logic, self-calibration logic, adders and SRAM. The modules in the bottom of Fig. 48 are responsible for normal SAR conversion while those in the top are in charge of the self calibration.

Once the ADC is powered on, the measurement of the mismatch is started under the control of self-calibration logic. The measurement begins from the MSB capacitor in the MSB DAC and ends at the LSB capacitor. To begin with, all capacitors except the capacitor ready for the measurement in the main DAC samples reference voltage Vref and then redistribute the charge with the capacitor ready for the measurement, resulting in the residual voltage related to the mismatch.

Then the calibration DAC digitizes the residual voltage in a SAR conversion making use of the precise comparator Comp2.

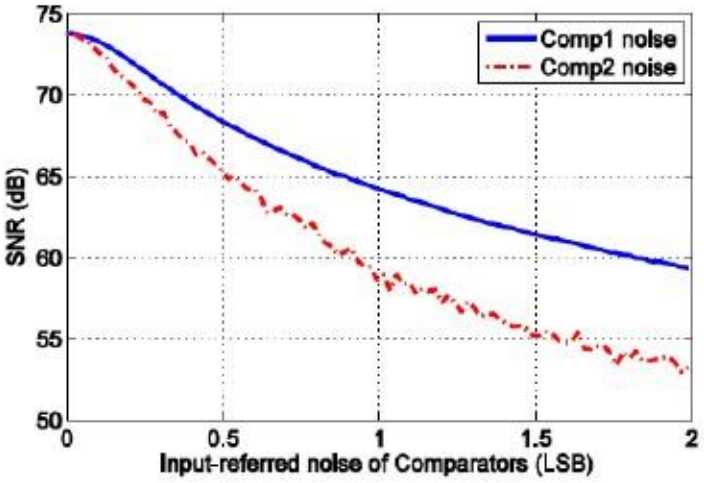


Fig. 49. SNR of 12bit self-calibrated ADC as functions of the comparators'noises.

The digital code of the residual voltage is processed by adders and stored in the on-chip SRAM, thus the measurement of one capacitor's mismatch is accomplished. This procedure repeats subsequently until the LSB capacitor in MSB DAC is completed. After the measurement of the mismatch, the normal conversion begins and the mismatch-measurement block is powered off. During the normal conversion, the calibration DAC adjusts its connection according to the output of Comp1 and the accumulation result of the data read from the SRAM. Effectively, the error voltage caused by capacitors' mismatches is compensated by the calibration DAC and the accurate successive approximation could be established.

SAR ADCS COMPARED WITH OTHER ADC ARCHITECTURES

Versus Pipelined ADCs -

A pipelined ADC employs a parallel structure in which each stage works on 1 to a few bits (of successive samples) concurrently. This inherent parallelism increases throughput, but at a trade-off of power consumption and latency. Latency in this case is defined as the difference between the time when an analog sample is acquired by the ADC and the time when the digital data is available at the output.

For example, a five-stage pipelined ADC will have at least five clock cycles of latency, whereas a SAR has only one clock cycle of latency. Note that the latency definition applies only to the throughput of the ADC, not the internal clock of a SAR which runs at many times the frequency of the throughput.

Pipelined ADCs frequently have digital error-correction logic to reduce the accuracy requirement of the flash ADCs (i.e., comparators) in each pipeline stage. However, a SAR ADC requires the comparator to be as accurate as the overall system. A pipelined ADC generally requires significantly more silicon area than an equivalent SAR. Like a SAR, a pipelined ADC with more than 12

bits of accuracy usually requires some form of trimming or calibration.

Versus Flash ADCs -

A flash ADC is comprised of a large bank of comparators, each consisting of wideband, low-gain preamp(s) followed by a latch. The preamps must only provide gain but do not need to be linear or accurate. This means that only the comparators' trip points have to be accurate. As a result, a flash ADC is the fastest architecture available.

The primary trade-off between a flash ADC's speed is the SAR ADC's significantly lower power consumption and smaller form factor. While extremely fast 8-bit flash ADCs (or their folding/interpolation variants) exist with sampling rates as high as 1.5Gsps (e.g., the MAX104, MAX106, and MAX108), it is much harder to find a 10-bit flash ADC. Moreover, 12-bit (and above) flash ADCs are not commercially viable products. This is simply because the number of comparators in a flash ADC increases by a factor of two for every extra bit of resolution. Meanwhile, each comparator must be twice as accurate. In a SAR ADC, however, the increased resolution requires more accurate components, yet the complexity does not increase exponentially. Of course, SAR ADCs are not capable of the speeds of flash ADCs.

Versus Sigma-Delta Converters -

Traditional oversampling/sigma-delta converters used in digital audio applications have limited bandwidths of about 22kHz. Recently, some high-bandwidth sigma-delta converters reached bandwidths of 1MHz to 2MHz with 12 to 16 bits of resolution. These are usually very-high-order sigma-delta modulators (for example, 4th-order or higher), incorporating a multibit ADC and multibit feedback DAC.

Sigma-delta converters have the innate advantage over SAR ADCs: they require no special trimming or calibration, even to attain 16 to 18 bits of resolution. Because their sampling rate is much higher than the effective bandwidth, they also do not require anti-alias filters with steep rolloffs at the analog inputs. The backend digital filters take care of this. The oversampling nature of the sigma-delta converter can also tend to "average out" any system noise at the analog inputs.

Sigma-delta converters trade speed for resolution. The need to sample many times (at least 16 times and often more) to produce one final sample dictates that the internal analog components in the sigmadelta modulator operate much faster than the final data rate. The digital decimation filter is also a challenge to design and consumes considerable silicon area. The fastest high-resolution

sigma-delta converters are not expected to have significantly higher bandwidth than a few MHz in the near future.

CALIBRATION OF COMPARATOR THRESHOLDS

Comparators are at the heart of nearly all ADC architectures, as they are required to perform quantization. Their accuracy is limited by offset and noise, but not all architectures are affected equally by these non-idealities. SAR ADCs, for example are generally quite robust to offset since in a conventional SAR ADC a comparator offset does not introduce any non-linearity. However, they are highly sensitive to comparator noise, as this noise is added directly to the input. Redundancy, which is nearly omnipresent in pipelined ADCs and gaining popularity fast in SAR ADCs, can reduce sensitivity to both offset and noise. In flash-based architectures, however, comparator accuracy is still key, and calibration is an extremely useful technique.

Indeed, the stringent requirements on offset can be all but completely avoided by adding threshold calibration. This is illustrated in Fig. 50 for comparators with a dynamic input pair followed by a latch. These comparators are activated on a falling clock edge and generate a rising slope at the drains of the input pair, depending on the input voltage. This slope is then resolved into digital levels by a latch in different configurations. Threshold

calibration can be added by controlling the capacitance to the drain of the input pair , by controlling the body terminals of the input pair or by controlling the voltage on the gates of a redundant input pair , among others. These calibration schemes have different advantages and disadvantages: using load capacitance is low-noise but slightly degrades speed, using body voltage tracks environmental changes reasonably well but requires a separate N-well and using a redundant input pair is probably the highest speed solution but slightly degrades noise.

Assuming comparator offset is calibrated, the final comparator accuracy is limited by noise. In nearly all cases, for a given power consumption and speed comparator noise spread is significantly lower than comparator offset spread, which implies a significant reduction in power consumption. In addition to these power savings, offset calibration typically significantly reduces comparator input capacitance. This is especially useful in flash-based architectures, where many parallel comparators are required, and target speeds are typically high.

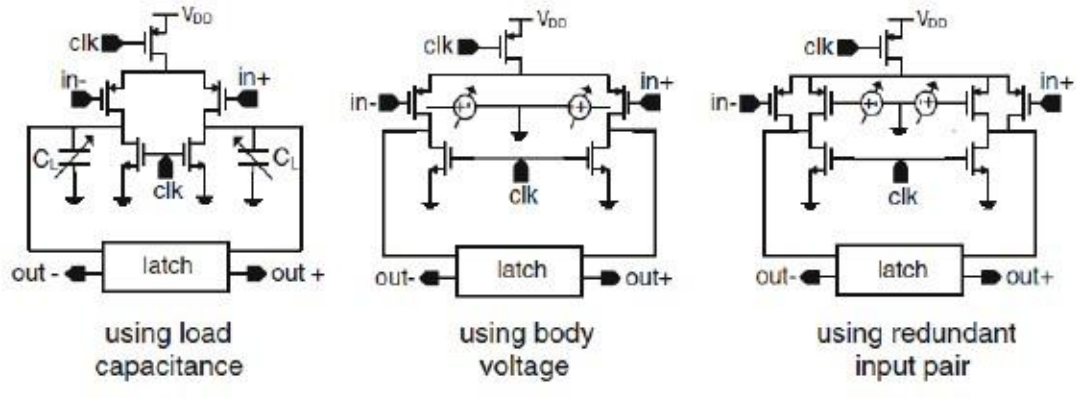


Fig. 50 Popular methods for comparator calibration.

Comparator calibration also enables a few architectural changes. One example is the noise-tolerant SAR ADC shown in Fig. 51 . This design uses two offsetcalibrated fully dynamic comparators in parallel: one of these is designed for low power and consequently has fairly high noise (HN), whereas the other is optimized for low noise (LN) at a power penalty. In the HN comparator is activated for the first eight SAR cycles, after which the LN comparator resolves two final cycles. By giving the final cycles 1b redundancy with respect to the first eight, the ADC can tolerate a fairly large r.m.s. noise in the HN comparator without an SNR penalty. Since only two low noise comparisons are required instead of nine, comparator power can be significantly reduced. Without offset calibration, this scheme would need far more redundancy to compensate for differences in offset between the two comparators.

Another example is the comparator-controlled SAR ADC proposed in and illustrated for a 4b example in Fig. 52. In this example, the input is tracked on two pseudo-differential 3b DACs and the input of 4 dynamic comparators. At a rising edge of the clock, the tracking switch opens and the first comparator is activated.

When this comparator decides, either the positive or negative DAC MSB is discharged and a ready signal is generated. This ready signal is delayed to allow time for DAC settling, and then activates the second comparator. This comparator in turn generates feedback and asynchronously activates the next comparator in line.

When all comparators have decided, the outputs of the 4 comparators can simply be latched to obtain the final output code. This arrangement thus implements a conventional SAR algorithm without the need for a controller, but in the absence of comparator calibration, this configuration would be crippled by offset. Regardless of how comparator offset calibration is implemented and leveraged, a method for controlling the calibration codes is required. The most straightforward choice is foreground calibration: applying the desired threshold at the comparator input and changing the calibration code until the comparator outputs as many zeroes as ones , or some variation on this scheme .

Background schemes also exist but vary wildly depending on architecture: adding a redundant ADC channel and averaging a rotating set of comparator pairs in a flash architecture , observing output code density or using redundancy to detect erroneous decisions.

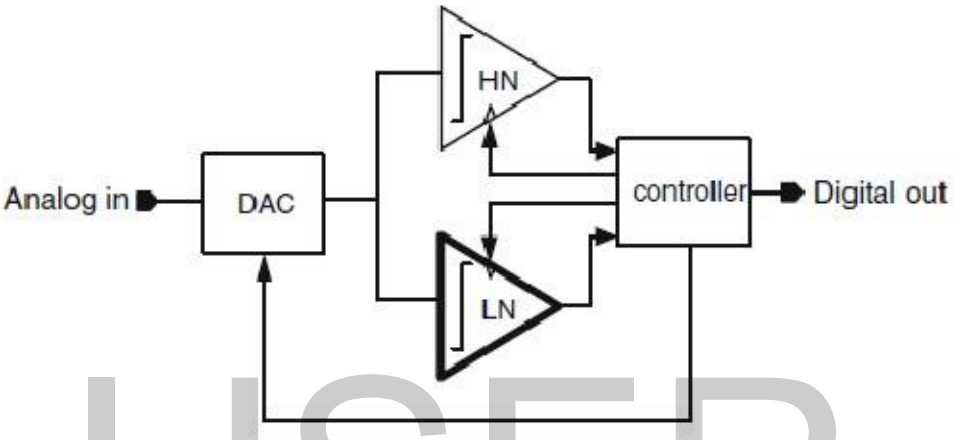


Fig. 51 Simplified block diagram of noise-tolerant SAR ADC.

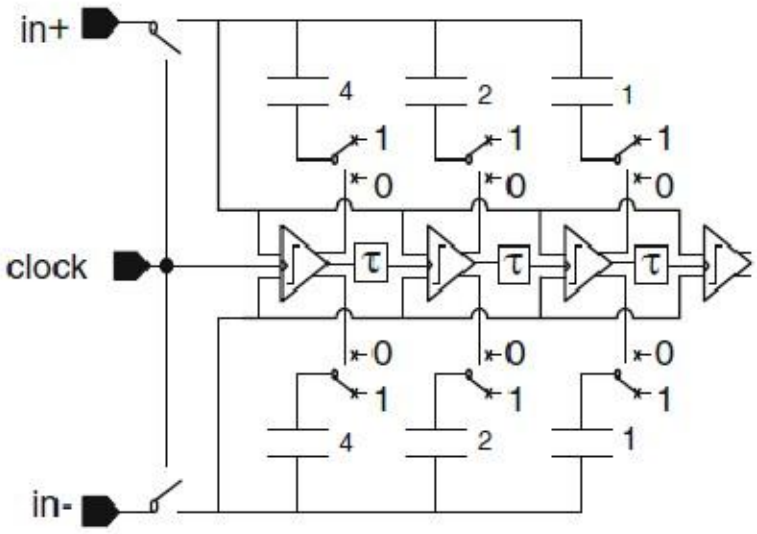


Fig. 52 Simplified block diagram of comparatorcontrolled SAR.

CHAPTER – 4

METHODOLOGY

DESIGN OF A PROTOTYPE ADC

The proposed ADC is designed in a 0.18 μm CMOS technology with five metal layers, two poly-silicon layers and is operated with a 1.8-V supply voltage.

SHA - Most pipelined ADCs need an SHA to acquire a high-frequency input signal. Without it, a pipeline ADC will have an error caused by clock skew between a sampling network of a first-stage MDAC and comparators in a first-stage sub-ADC. This error will have the same effect on a pipeline ADC as if it were a comparator offset voltage, and the error becomes larger as the input frequency gets higher. If a SHA exists in a pipelined ADC, an input signal is sampled and is kept constant during a holding clock phase. Since the sampled input remains constant, a small timing difference between an MDAC and a sub-ADC is no longer a problem. Because a SHA is placed at the front in a pipeline ADC, its design is crucial to the overall performance of an ADC. Hence, the design requirement of an SHA must be at least equal or be even more stringent than the overall design requirement of an ADC. Two SHA topologies are widely used in pipelined ADCs. One is known as

a charge-transferring SHA, the other is known as a flip-around . The latter was chosen for this prototype design because of its advantages over the charge-sharing topology. The fully differential circuit implementation of a flip-around SHA is shown in Figure 53.

When parasitic capacitance is ignored, the feedback factor β of a flip-around SHA is 1, whereas the feedback factor of a charge-transferring SHA is 0.5. Because the feedback factor of a flip-around SHA is twice as large, it only requires a half of op-amp gain bandwidth to produce the same closed-loop bandwidth. Thus, the same performance can be achieved with much less power by using a flip-around topology. A flip-around topology also has lower noise than a charge-transferring topology. The total input- referred noise power of a flip-around SHA can be written as

$$\overline{v_{n,t}^2} = \frac{KT}{C_S} + \frac{8\pi \cdot KT}{3 \cdot C_L}$$

where C_L is the output load capacitance of an op-amp. The first-term of total noise power is wideband $\frac{KT}{C}$ noise from the channel resistance of the sampling switches and the second-term is thermal noise from an op-amp. The total input referred noise power of a charge-transferring SHA is twice as large as that of a flip-around

SHA. Since a flip-around SHA has lower noise, it needs smaller capacitor size to achieve the same input referred noise power. This results in power saving for a flip-around SHA.

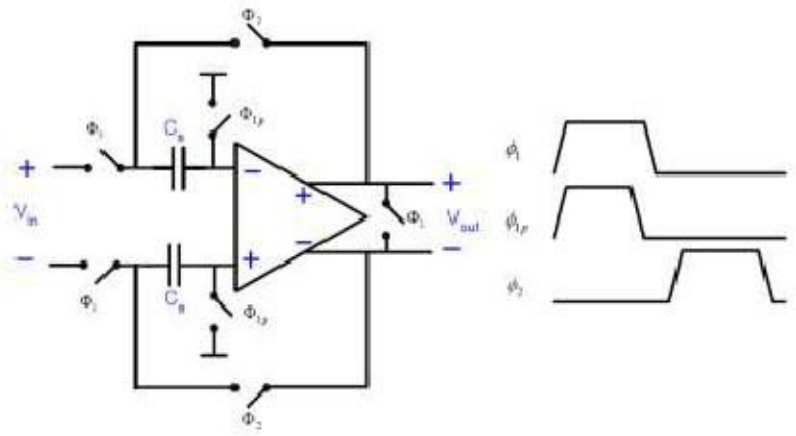


Figure 53: Fully differential flip-around SHA and its clock phases.

During $\Phi 1$ clock phase, an input signal is applied to a sampling capacitor C_s. At the falling edge of Φ_{1p} clock phase, the applied input signal is captured on the sampling capacitor C_s, During Φ_2 clock phase, the bottom plate of the sampling capacitor is connected to the output of an amplifier holding the sampled input voltage. A11 amplifier for a flip-around SHA should have a large input common-mode range when the input common-mode level is different from the output common-mode range. Since in this design both the input and the output common-mode level is set to the middle of a supply voltage, there is no concern about the input common-mode range of an amplifier.

MP AC - Two different MDACs are used in this prototype ADC One is a 2.5-bit MDAC and the other is a 1.5-bit. The 2.5-bit MDAC is used only for the first stage of the pipeline and the 1.5-bit MDAC is used for the rest of pipeline stages that are from the 2nd stage to the 7th stage. The circuit implementations of the 2.5-bit and the 1.5-bit MDAC are illustrated in Figure 54 and Figure 55, respectively. Basically, both MDACs consist of an op-amp, capacitors and switches. The two non-overlapping clocks, Φ_1 and Φ_2 are required to drive the switches. The two extra clocks. Φ_{1p} and Φ_{2p} are used to reduce charge injection errors from switches.

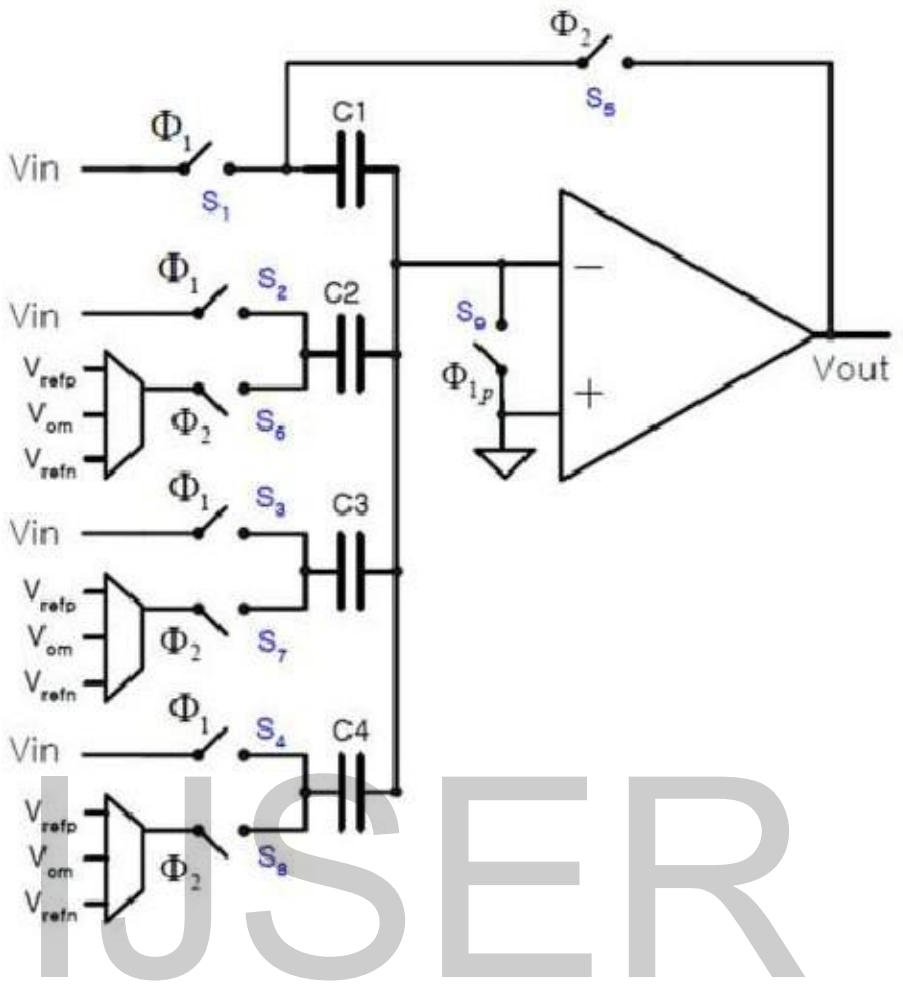


Figure 54: Switched-capacitor circuit implementation of the 2.5-bit MDAC

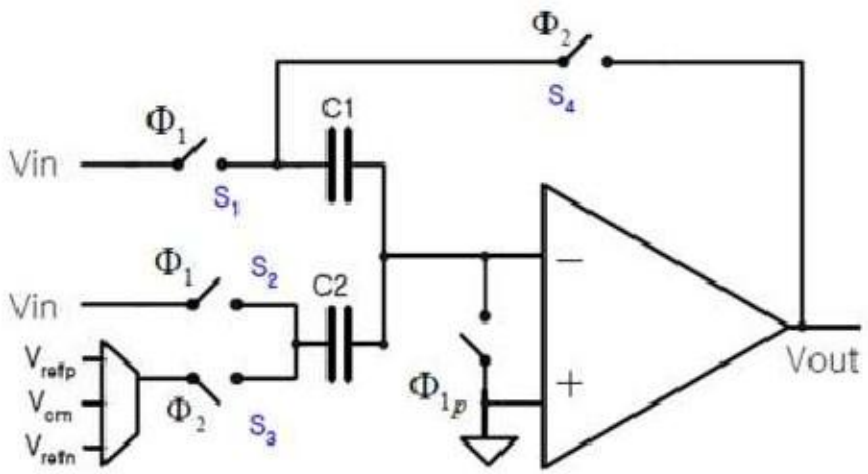


Figure 55: Switched-capacitor implementation of the 1.5-bit MDAC.

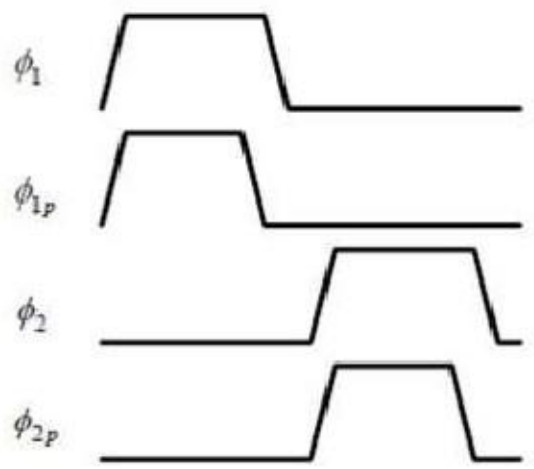


Figure 56: Non-overlapping clock phases

The operation of the 2.5-bit MDAC is as follows. During a sampling phase. Φ_1 and Φ_{1p} clocks are high turning 011 switches $S_1 \sim S_4$. All of capacitors are connected to an

input signal and the inputs of the op-amp are connected to a common-mode voltage. The sampling process is completed at the falling edge of clock Φ_{1p}. The input signal is sampled 011 all capacitors. Then. Φ_1 goes low. and switches $S_1 \sim S_4$ are off. The charge

injection from these switches does not change the charge 011 the capacitor since there is no DC path. During a holding phase, Φ_2 clock is high. The capacitor C_1 is now connected to the

output of the op-amp and the rest of the capacitors are connected to V_{refp} or V_{refn} or V_{cm} depending on the output of the sub-ADC.

SUB-ADC AND COMPARATOR - This design uses three different sub-ADCs. They are all flash-type sub-ADCs. A 2.5-bit sub-ADC is used in a first-stage and a 1.5-bit sub-ADC is used from the 2nd to 7th - stage. For the last stage, a 2-bit sub-ADC is used. The single-ended version of a 2.5-bit sub-ADC is illustrated in Figure 57. It consists of six comparators, six reference tap voltages generated from a resistor string and a decoding logic that converts a thermometer code into a binary code. This type of architecture usually has a problem called "bubble" or "sparkle" . This is caused by timing differences between comparators with offset voltages. For example, the output of comparators with a '"bubble" problem can be 000101 instead of 000111. Three-input digital NOR gates are used to suppress the effect of the bubble problem.

Each comparator consists of a preamplifier, a latch and a switched-capacitor circuit for processing a differential signal and offset cancellation. The preamplifier used in the 2.5-bit sub-ADC is shown in Figure 58. It is implemented with a NMOS differential input pair with diode-connected and cross-connected PMOS loads.

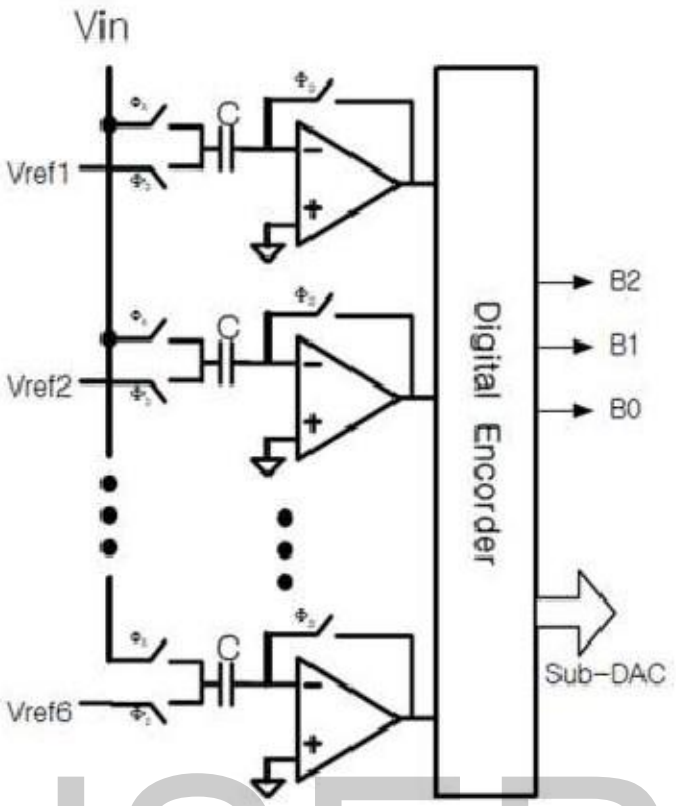


Figure 57: A single-ended version of the 2.5-bit sub-ADC

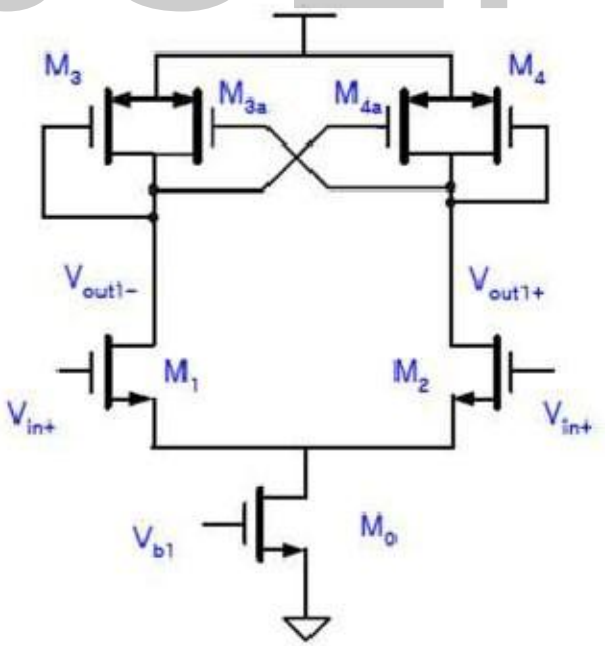


Figure 58: Preamplifier used in 2.5-bit sub-ADC

CLOCK GENERATOR - A schematic of the clock generator circuit is shown in Figure 59. It is driven by a reference clock provided from an external source. Two non-overlapping clocks are generated from it to operate switched-capacitor circuits. The non-overlapping interval is created by a propagation delay in inverter chains. An additional pair of delayed clock phases is also generated for a bottom-plate sampling technique to reduce charge injection errors. Clock phases are distributed by four local clock generators instead of one global clock generator. This is done to reduce the effect of clock skew due to interconnections in the layout. Each local clock generator is driven by a single master clock to synchronize between stages. To minimize clock skew, the length of the clock lines are matched as much as possible and the tree structure of the inverter chain is used to distribute the clock from the master clock to improve speed and accuracy. The timing diagram of the clock generator is shown in Figure 60.

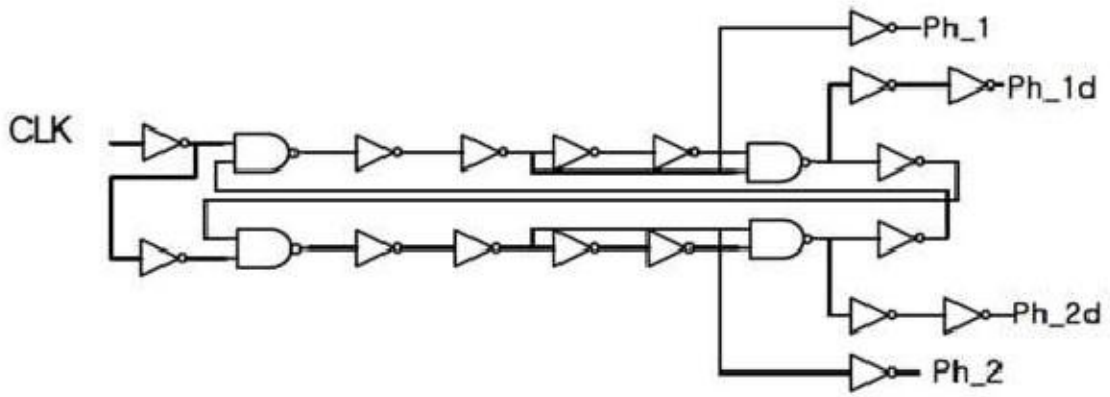


Figure 59: Non-overlapping clock generator.

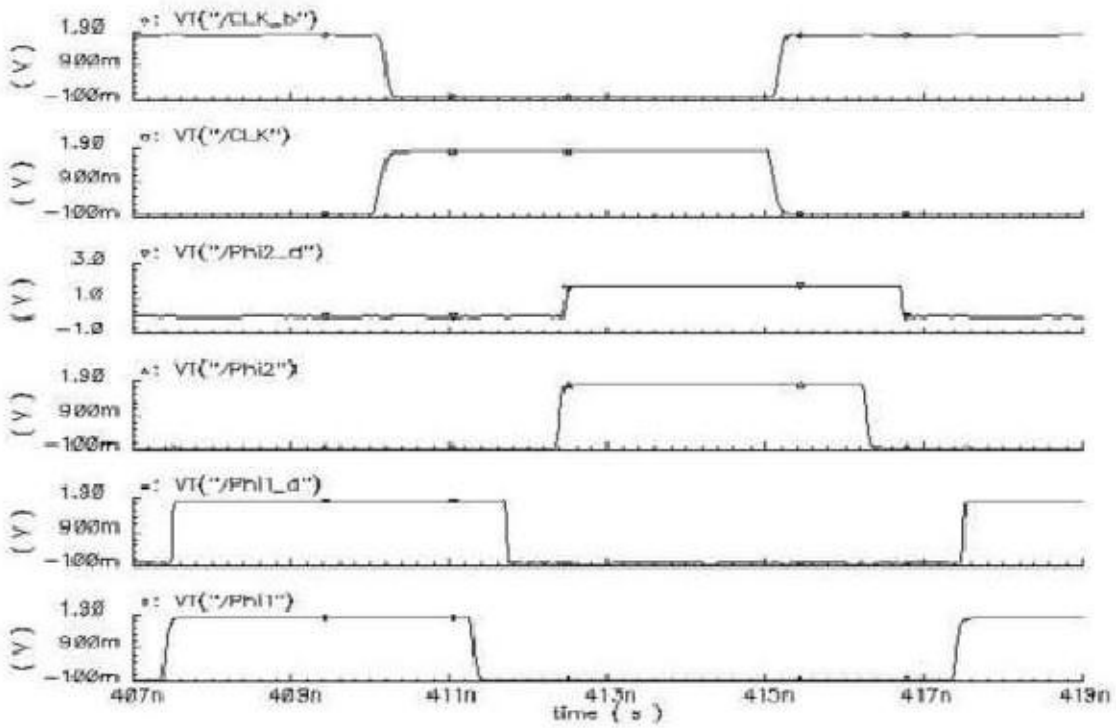


Figure 60: Timing diagram of the clock generator.

PIPELINE ADC DESIGN

The pipeline ADC architecture combines the benefits of high throughput and an input capacitance bound by noise constraints. Typical pipeline architecture is illustrated in Figure 61. Each stage has the four elements of Comparator, a summer, multiplier, mux and transmission gate.

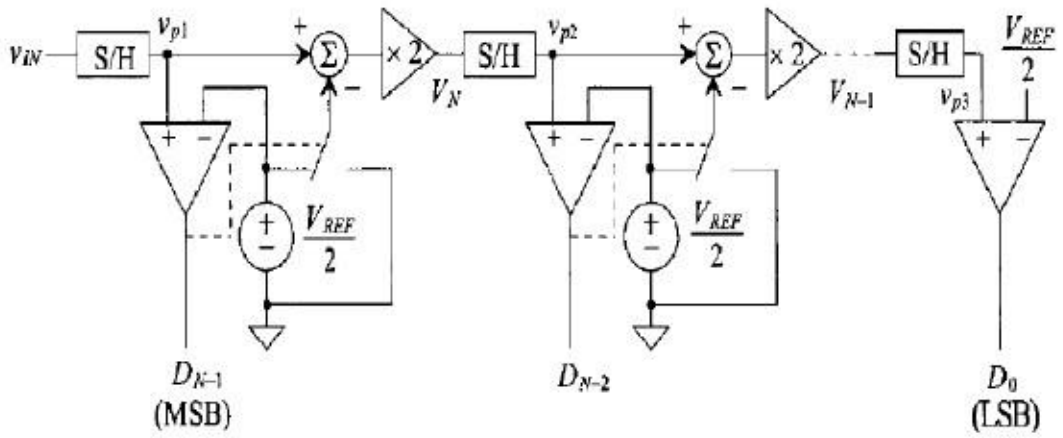


Fig 61 pipeline A/D converter

The pipeline ADC is an N-step converter, with 1 bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists ofN stages connected in series (Fig.). Each stage contains a 1-bit ADC (a comparator), a sample-and-holcl, a summer, and a gain of two amplifiers. Each stage of the converter performs the following operation:

1. After the input signal has been sampled, compare it to vref72. The output of each comparator is the bit conversion for that stage.

2. If vm > vref '2 (comparator output is 1). vref 2 is subtracted from the held signal and pass the result to the amplifier. If vIN < vref/2 (comparator output is 0). then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the residue.

3. Multiply the result of the summation by 2 and pass the result to the sample and- hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial latency of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on the next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions. The disadvantage is having the initial N clock cycle delay before the first digital output appears. The severity of this disadvantage depends, of course, on the application. One interesting aspect of this converter is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages. The Pipelined ADC can be thought of as an amplitude- interleaved topology where errors from one stage are correlated with errors from previous stage. The basic block diagram implementation of an N-bit Pipelined ADC using the cyclic stages is as shown in Figure 62. Instead of cycling the analog output of the 1 bit/stage section back to its input, we feed the output into next stage. The stages are clocked with

opposite phases of the master clock signal. The comparator outputs are labelled digital in figure.

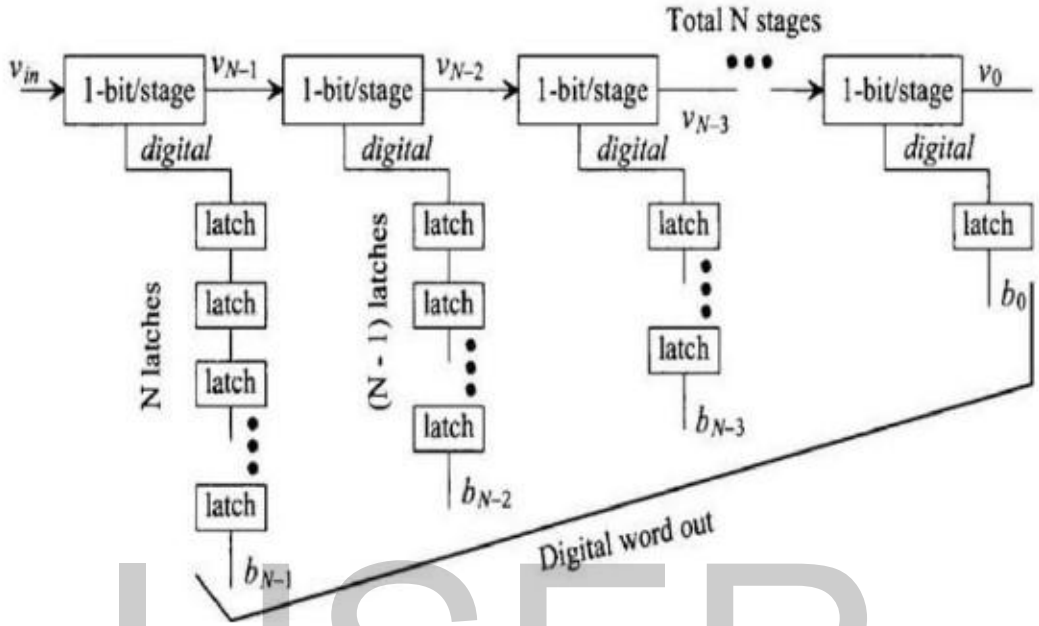


Fig 62. Pipeline ADC based on cyclic stages.

The digital comparator outputs are delayed through latches so that the final digital output word corresponds to the input signal sampled N clock cycles earlier. The first stage in figure must be N-bit accurate. It must amplify its analog output voltage, VN-1 to within 1 LSB of the ideal value. The second stage output, VN-2 must be an analog voltage within 2 LSB of its ideal value. The third stage output, VN-3 must be an analog voltage within 4 LSB of its ideal value.

SAR ADC CIRCUIT DESIGN

The main blocks of this proposed SAR ADC are level shifters, D/A converter, comparator and SAR control logic circuit. VDDA represents a 3.3 V analog supply while VDDD is the 1.0 V digital supply. CLK is the clock of this converter and SOC (start of conversion) represents the signal that controls sampling. CH [7:0] represents the eight input channels which are controlled by the selecting signal S [2:0]. Vref represents the voltage reference of the converter. A 25 $k\Omega$ external resistor R is used to provide bias current for the comparator. EOC is used for ending the conversion and D [9:0] is the 10-bit digital output. The level shifters are used to convert the low voltage control signals to a higher level for the analog circuit application.

Low power voltage level shifter - The level shifter is an important building block for multi supply SoC applications. As we know, with a given noise floor, a low operating voltage makes high dynamic range design difficult.

To overcome the problem, operation under multiple supplies is a selection for nanometer scale SoC applications. In this design, to achieve high input dynamic range and high signal to noise ratio, a 3.3 V analog supply and 3.3 V voltage reference are used and the

digital circuits operate under the 1.0 V digital supply. This makes the level shifters very important in this design, because many control signals generated by the SAR control logic should be used to control the operation of the internal DAC and comparator. Therefore, some low to high voltage level shifters should be utilized to convert these digital control signals to a higher analog voltage level. Low power level shifter design is also significant for reducing the power dissipation of the ADC.

Figure 63(a) is the traditional voltage level shifter structure. The disadvantages of this approach are low speed and high power dissipation. Due to their low speed of the input transistors M3 and M4, the PMOS M_7 cannot be turned off immediately when the node A0 needs to discharge. Thus, a long time delay exists and it consumes too much power. In this study, low power architecture is utilized, as shown in Fig. 63(b). The gate control voltages of M_9 and M_{10} are lower than those of M6 and M7 in Fig. 63(a). Then, when the node A_1 needs to discharge, M10 can be turned off with a higher speed. Therefore, this approach is characterized by high speed and low power dissipation. Figure 64 shows the simulation results based on 90 nm CMOS 3.3 V/1.0 V technology. From Fig. 64(a), the delay time of the level shifter with low power structure is very small.

Figure 64(b) shows the variation of the current flow through the cross-coupled PMOS transistors in both structures. Since more transistors are stacked between the VDDA and VSSA, and conversion time has been dramatically reduced, the dynamic current and its duration are both less than the traditional approach.

In this SAR A/D converter, eighteen voltage level shifters are utilized to convert the low voltage (1.0 V) control signals to a higher level (3.3 V) for analog circuit application.

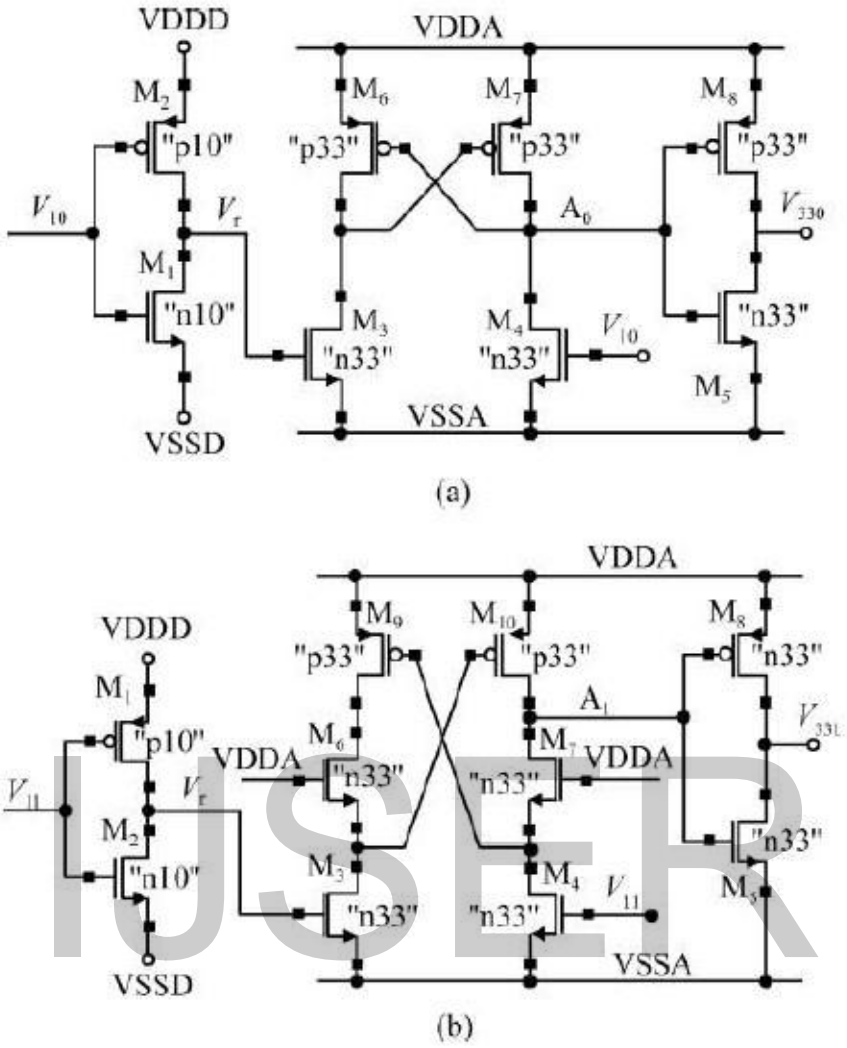


Fig. 63. Voltage level shifter. (a) Traditional structure. (b) Low power structure.

Internal DAC design and discussion - In the SAR A/D converter, the D/A converter is one of the most critical blocks. As in the description in this section, either charge redistribution or voltage scaling method can be used to implement the internal D/A converter. But both of these two approaches cannot easily realize

low power dissipation and small area simultaneously. In this SAR A/D converter, a hybrid architecture D/A converter is utilized, as shown in Fig. 65.

Compared with traditional topologies, this approach can obviously reduce the number of passive components and chip area, which is more significant in embedded SoC applications. In Fig. 65, a 7-bit resistor ladder and an 8 : 1 capacitor pair are combined to realize 10-bit resolution. V_M represents the output of the 7-bit voltage scaling D/A converter while V_L is

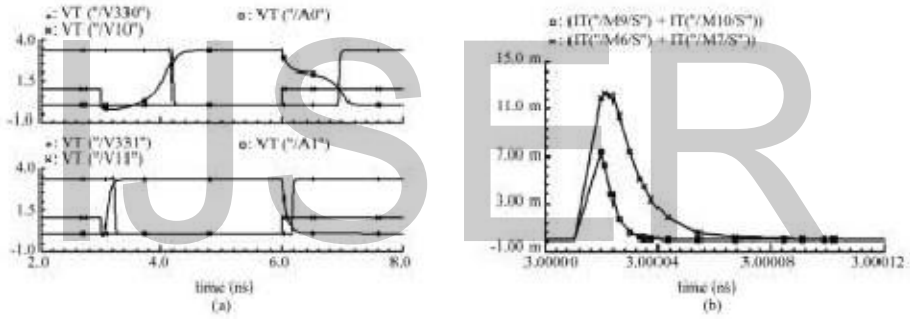


Fig. 64. Voltage level shifter simulation results with (a) speed and (b) power.

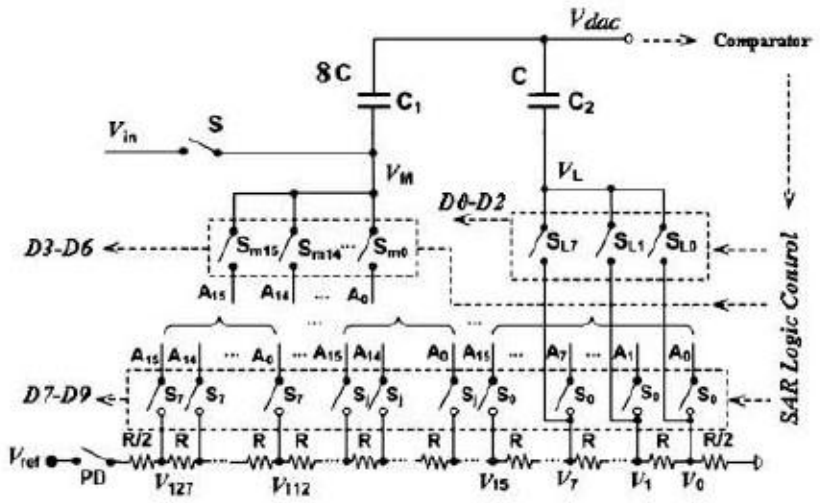


Fig. 65. Architecture of the internal D/A converter.

the output value of its last three bits, and $C_1 = 8C$, $C_2 = C$. Here. C represents the unit capacitor. In the sampling phase, with the switch S turned on. the analog input V_m is sampled by capacitor C_1 while V_L is connected to V_5 which has a voltage value of $9K_{ref}/256$. In the conversion phase, K_M is connected to C_1 and V_L is comiected to C_2. Then, with the approximation principle of the SAR A D converter, at the end of the conversion phase, we have:

$$V_{\text{in}} \times 8C + V_5 \times C = V_{\text{M}} \times 8C + V_{\text{L}} \times C.$$

After a rearrangement, we can set:

$$V_{\text{in}} = V_{\text{M}} + \frac{1}{8}(V_{\text{L}} - V_5).$$

With the substitution of $V_M = \frac{V_{ref}}{128}\left(\sum_{i=3}^{9} D_i \times 2^{i-3} + \frac{1}{2}\right)$ and $V_L = \frac{V_{ref}}{128}\left(\sum_{i=0}^{2} D_i \times 2^{i} + \frac{1}{2}\right)$ into Eq. (2). we can approx imate V_m as below:

The speed of the SAR A/D converter is mainly limited by the settling time of the D/A converter and the comparator. Within a specified time, they must settle to within the resolution of the overall A D converter. For the topology, attention has been paid to ensuring that the capacitances of the lower plate switches do not affect the accuracy of the conversion because every node is driven to a final voltage, but the switch- on resistances of these switches can affect the conversion rate. Therefore, these switches should be optimized to avoid errors caused by long delay times.

Logic circuit design - The control logic block is used to realize the binary search algorithm, store the intermediate results and generate control signals for the analog block. Figure 66 shows some control signals employed in the SAR A/D converter, where SOC represents the start signal of the conversion and EOC represents the end signal of the conversion.

After the sample-and-hold process is completed in the first clock pulse, ten periods are subsequently used to realize the SAR algorithm and generate the outputs. Eleven clock cycles are required to complete one A/D conversion. At the 11th clock cycle, EOC turns to a high level, and the 10-bit output is avail able. Before the converter begins to work, a RESET pulse is suggested to put before the first SOC pulse.

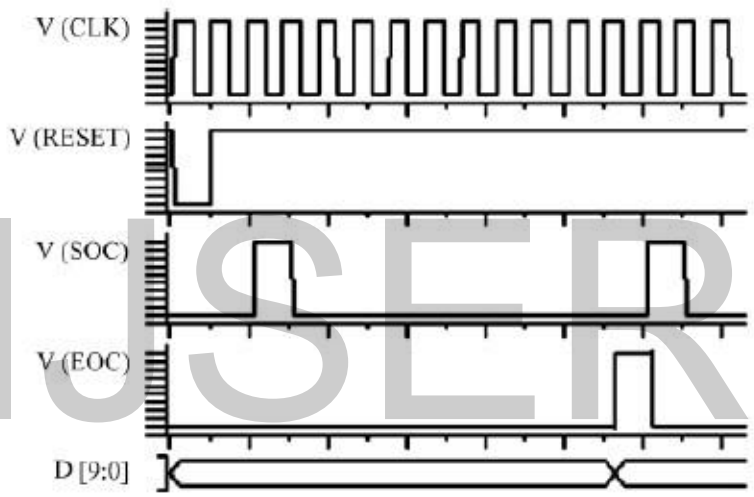


Fig. 66. Control signals in the SAR A/D converter.

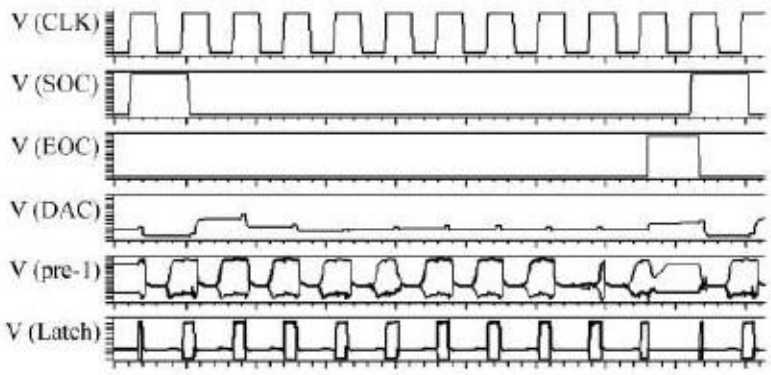


Fig. 67. Post-simulation result of the SAR A/D converter.

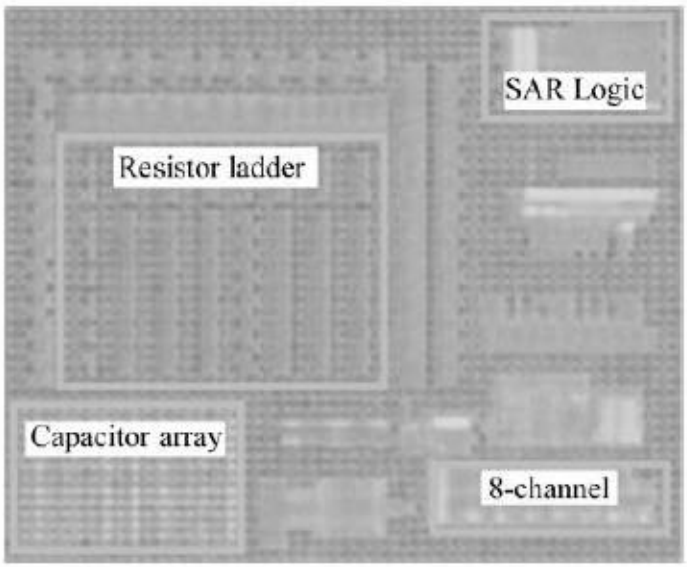


Fig. 68. Microphotograph of the proposed converter.

CIRCUIT IMPLEMENTATION

With ADS and various designed components we have designed complete Pipeline Architecture shown in fig 69. And we got the simulation results shown in fig 70. And table 2 shows digital values for given analog voltage.

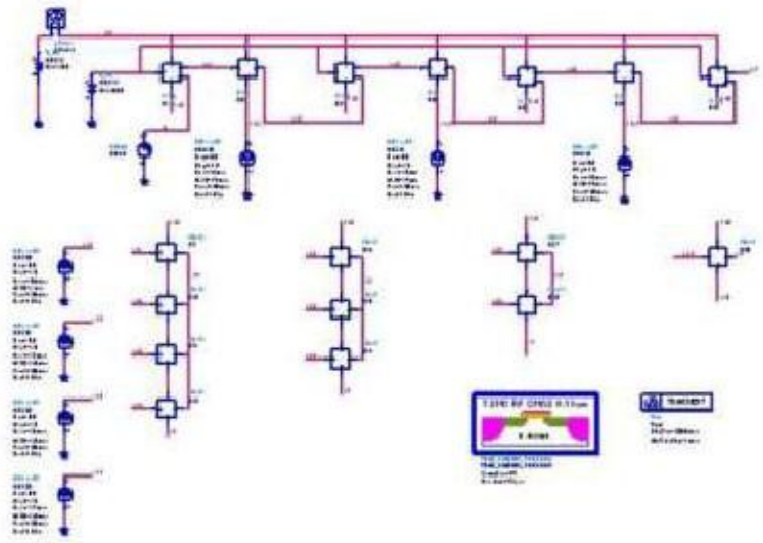


Fig 69 Pipeline Architecture.

For our Design of 4 bit resolution ADC digital code we are getting is as follows

Input analog voltage	Q3	Q2	Q1	Q0
0000	0	0	0	0
0.0625	0	0	0	1
0.125	0	0	1	0
0.1875	0	0	1	1
0.25	0	1	0	0
0.3125	0	1	0	1
0.375	0	1	1	0
0.4375	0	1	1	1
0.5	1	0	0	0
0.5625	1	0	0	1
0.625	1	0	1	0
0.6875	1	0	1	1
0.75	1	1	0	0
0.8175	1	1	0	1
0.875	1	1	1	0
0.9375	1	1	1	1

Table 2 Digital Codes

The ADC is fabricated in 0.18µm standard CMOS process with 4 bit rsolution. The value of the unit capacitor is 100fF. The static performance of the ADC is shown in Fig. 69. ADC operats at 1.2v. The DNL and INL of the ADC are a measurement factor of linearity.

THE DESIGN OF HIGH FREQUENCY LOW POWER OPAMP

OPAMP being a key element in an analog processing system, as proposed in our previous work , a high frequency CMOS operational amplifier (Op-Amp) shown in figure 70 which operates at 3V power supply using tsmc 0.18 micron CMOS technology was designed. As compared to the conventional approach, the proposed compensation method results in a higher unity gain frequency under the same load condition. The design parameters along with the electrical parameters yielded. This circuit operates efficiently in a closed loop feedback system, with a current buffer compensation circuit while high bandwidth makes it suitable for high speed applications. The circuit operating conditions includes the room temperature as the operating temperature with a power supply of 3V and a load of 10pF.

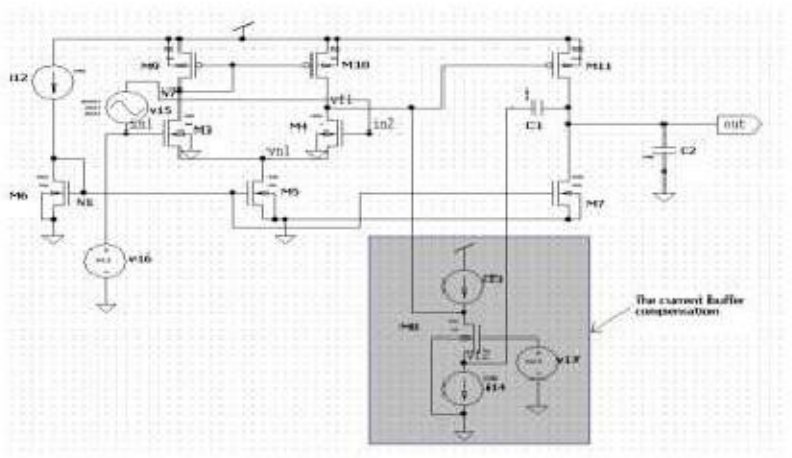


Figure 70: The complete schematic of the two-stage op amp

For the frequency response plot, an ac signal of 1V is swept with 5 points per decade from a frequency of 10KHz to 4GHz. Fig.71 illustrates the frequency response which shows a dc gain in dB versus frequency in Hz (in log scale) and phase margin of OPAMP in open loop. The dc gain is found to be 49.02dB and phase margin 60.5$_0$ which is good enough for an OPAMP operating at a high frequency. A unity gain frequency of 2.02GHz is excellent for an OPAMP when all the other parameters are also set at an optimized value.

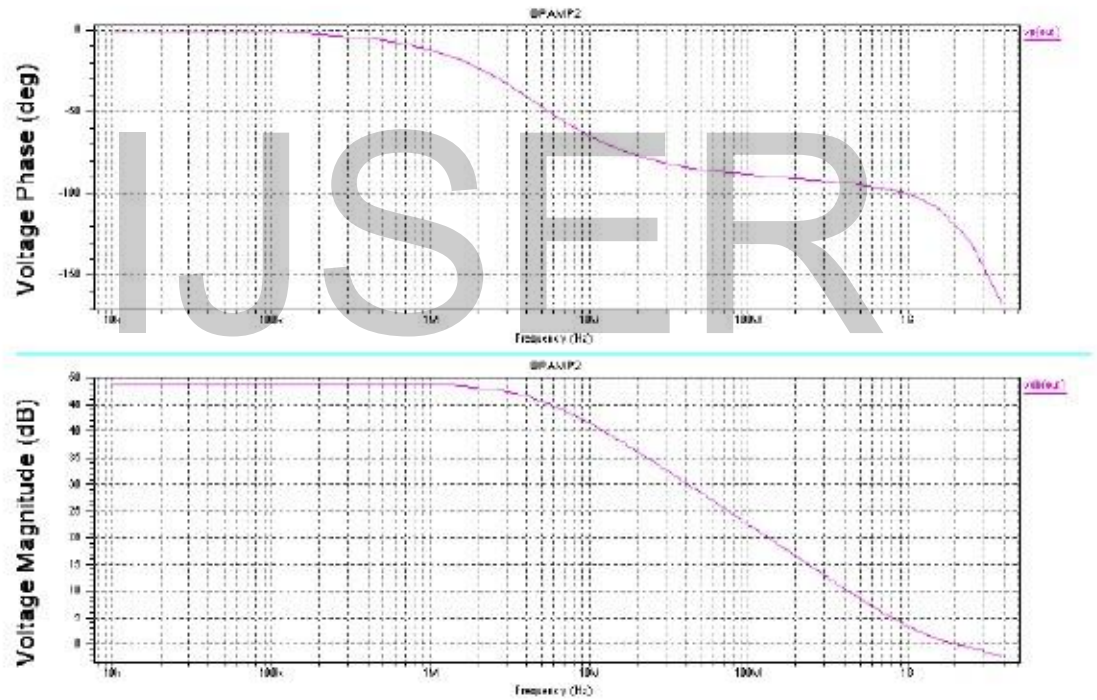


Figure 71: Frequency response of the OPAMP.

The slew rate simulation is carried out performing a transient analysis using a pulse waveform of 1mV for a pulse period of 0.5nsec. The slew rate (+ve and –ve) are found to be 1.41V/µs and

1.42V/µs respectively, which is quite good as compared to other low power, low voltage OPAMPs. The slew rate response is as shown in figure 72.

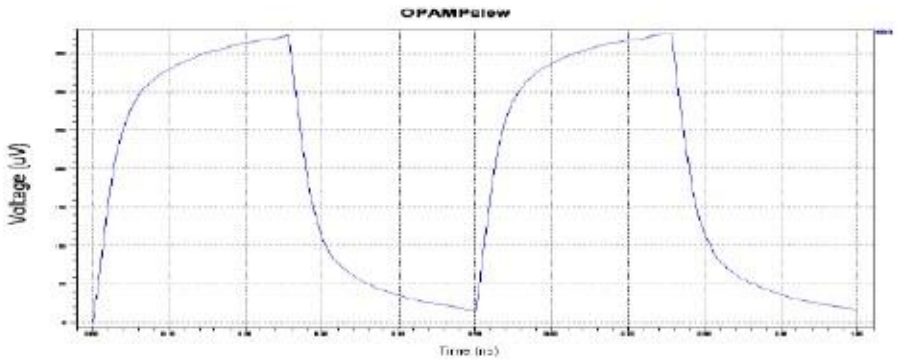


Figure 72: Slew rate (+ve and –ve) of OPAMP.

The graph of output noise of the OPAMP is given below, yielding an output noise of 1.64µV/sqrt(Hz).

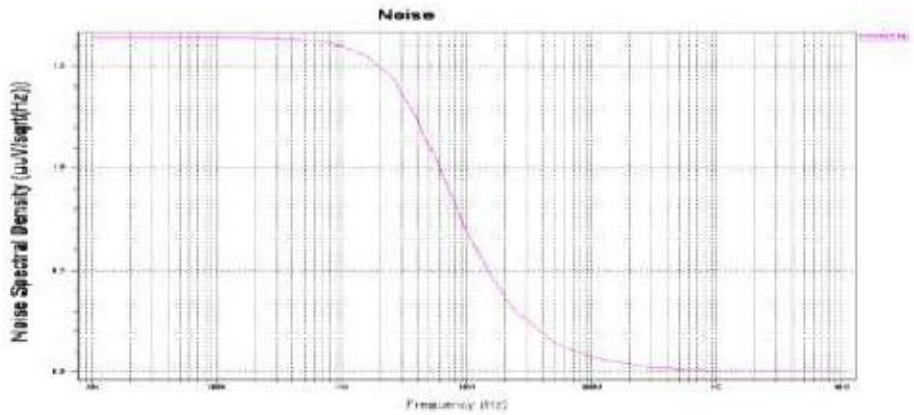


Figure 73: Output noise characteristics.

The graph evaluating power supply rejection ratio (PSRR) in dB is shown in the following figure 75. PSRR measures the influence of power supply ripple on the OPAMP output voltage. It is the ratio of voltage gain from the input to output (open loop) to that from the supply to the output. PSRR can be calculated by putting the OPAMP in the unity gain configuration with the input shorted. The Miller compensation capacitance allows the power supply ripple at the output to be large enough. The PSRR (+ve) of the OPAMP in this design is calculated to be 154 dB . The circuit for PSRR calculation is shown below:

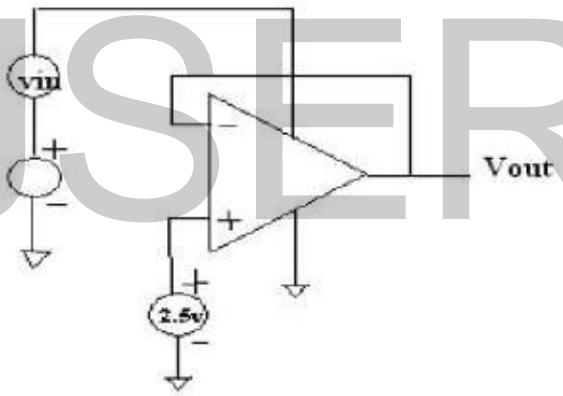


Figure 74: Circuit for PSRR measurement.

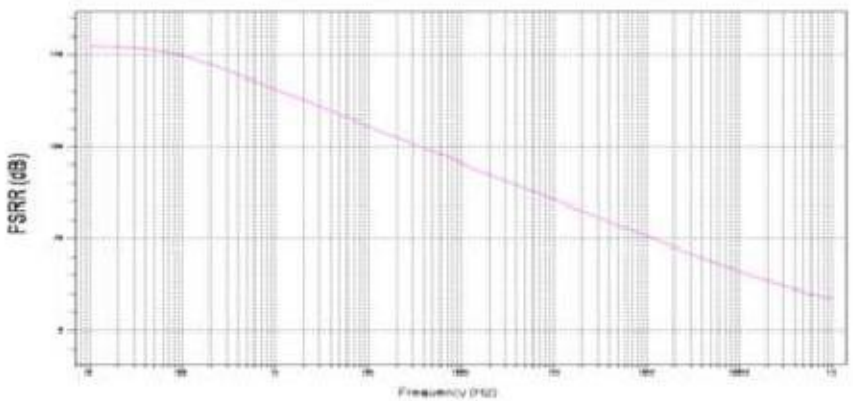


Figure 75: PSRR of the OPAMP.

The waveform below shows the location of the poles in the voltage magnitude waveform.

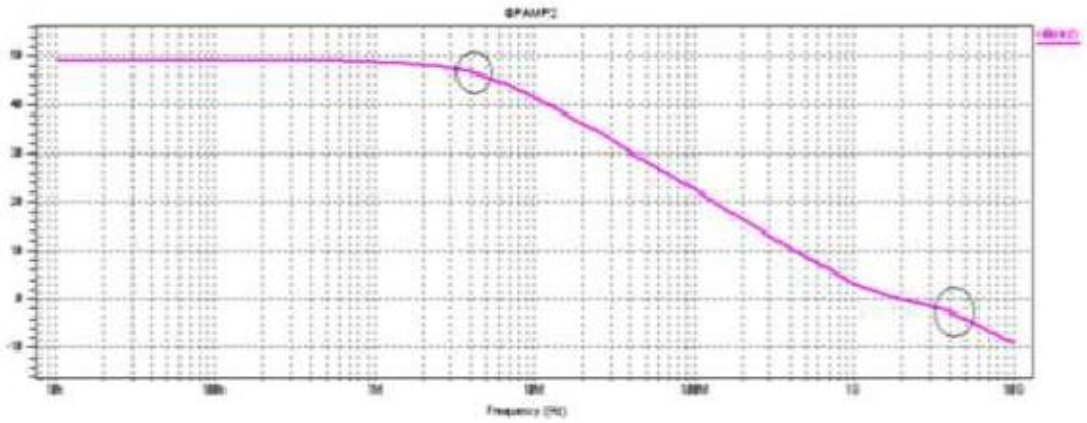


Figure 76: The waveform showing the location of poles in the voltage magnitude waveform

The design parameters		The electrical parameters yielded	
M1	15/0.2 µm/ µm	g_{mI}, g_{mII}	806µ, 537µ
M2	15/0.2 µm/ µm	Phase margin, O	60.5^{0}
M3	3.2/0.4µm/ µm	C_{01}	24.8fF
M4	3.2/0.4µm/ µm	Unity gain frequency, f_T	2.02GHz
M5	6.2/0.2µm/ µm	DC Gain	49.02dB
M6	1.2/0.2µm/ µm	PSRR(+ve)	154dB
M7	0.8/0.2µm/ µm	Settling time	0.5nsec
M8	0.4/0.2µm/ µm	Slew rate (+ve,-ve)	1.41V/µs; 1.42V/µs
Mb	3.2/0.2µm/ µm	Common mode gain	0.54957dB
I_{ref}	50µA	CMRR	39dB
Vdd	3V	Noise	1.64µV/sqrt(Hz)
C_L	10pF	Power consumption	39.6µW

Table 3 The geometrical dimensions incorporated and the electrical parameters yielded

CMOS COMPARATOR DESIGN

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator design plays an important role in high speed ADCs. The function of comparison is a crucial, and often a limiting component in the design of high speed data conversion systems due to its finite accuracy, comparison, speed and power consumption. Using the same OPAMP of our previous work with the same parameters , a comparator is designed which consists by using current mirrors, current sinks, active load & constant current source. Transistor W/L ratios are as selected which gives accurate & optimum results. Parasitic effects which influences in the comparators performance is minimized in this design. This help to get the desired output for a high speed & low power consumption. The comparator circuit is depicted in Figure 77 has been simulated using tanner tool with tsmc 0.18 micron CMOS technology.

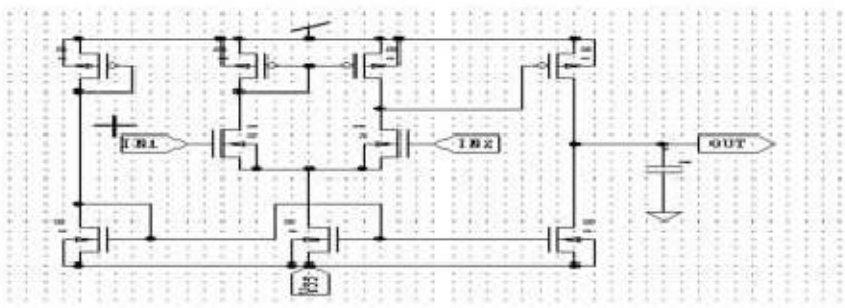


Figure 77: Proposed design of CMOS comparator.

THE SAR CONTROL LOGIC

Of the several SAR designs presently in use, the most common design uses a separate sequencer and code register made from D-type flip-flops. The function of the sequencer (performed by the shift register) is to control the enable of the code register and sequentially setting each flip-flop in the register to a “trial” state such that on the next clock pulse, the flip-flop is conditionally set by the present information on the data line, i.e the data from comparator output. The advantage of this design lies in its simplicity and ease of layout which consists of reproducing each bit cell. The output of the shift register is fed to the enable input of the code flip-flop, while the complementary output of the shift register is fed as one of the input to the NAND gates. The complementary output of the code register is fed as the other input to

the NAND gates. The comparator output is directly fed to the input of the code register which either sets or resets the output bits of the SAR in accordance to the binary search algorithm. The comparator output is compared with the bit at the clock when the particular code register is enabled. The output of the NAND gates provides the output of the SAR. The 8-bit SAR schematic is shown in the figure 78.

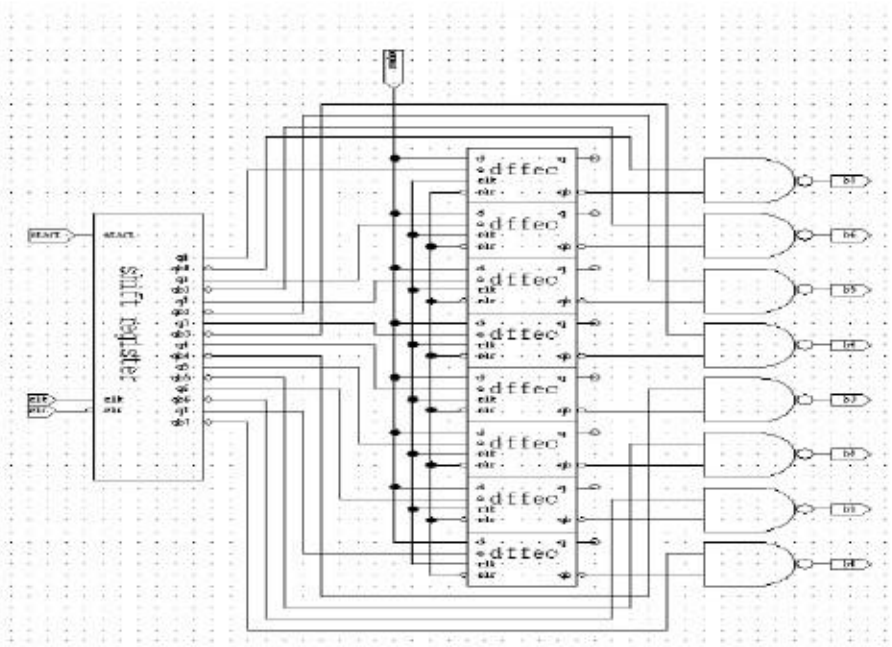


Figure 78: The successive approximation register (8-bit).

CHAPTER – 5

CONCLUSION

ADC is the key design Block in modern microelectronics digital communication system. With the fast advancement of CMOS fabrication technology and continued proliferation of mixed analog and digital VLSI systems, the need for small sized, low-power and high-speed analog-to-digital converters has increased. With an increasing trend to a system-on-chip, an ADC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other digital circuits. So we have proposed low power ADC. From different ADC architectures available Flash ADC is having the drawback of large chip area n high power dissipation and Pipeline ADC has complex circuit. The Pipeline ADC is best suitable for low power application. For designing purpose we have used Advanced Designing System. The Pipeline ADC core is composed by comparator, Transmission Gate, and pipeline control logic; these components have been designed targeting to fulfill several constraints on requirements such as low power dissipation, the offsets due to mismatch. From the results presented we could conclude that conversion is performed without missing codes and a

low-power high speed 4-bit Pipeline ADC in a 0.18µm CMOS process with a 1.2 V supply voltage is designed.

The primary goal of this work is to choose and optimize or develop an ADC topology with fast conversion time. For that purpose, a simple and fast successive approximation analog to digital converter design technique is proposed. Among the most conventional ADC, SA-ADC, that follows the principle of a binary search algorithm, have proven to

exhibit a faster conversion and very efficient for the target resolution. The entire binary search in the ADC is based upon some digital logic that is implemented using the SAR, DAC and the comparator. These components are made up of flip flops and logic gates and are connected in a feedback manner. Successive approximation ADC is more suitable for interleaving. In this work, SA-ADC of 8-bits is designed, which can also be extended up to more number of bits. In

the design, the only possible obstacle in high speed conversion is if the comparator had a limited gain-bandwidth product. But this difficulty is overcome with the use of the high speed comparator designed with the high frequency OPAMP.

The thesis presents a comprehensive pipeline ADC design methodology. The pipeline ADC design methodology provides a comprehensive and quantitative mapping matrix between system level ADC performance specs (e.g., power optimization, sampling rate, resolution, input voltage range, etc.) and the critical design parameters at block levels, such as, thermal noise limitation, op-amp selection in S/H and MDAC, DC gain and closed-loop gain bandwidth of op-amps requirement, sampling capacitor selection criterion etc.

The design methodology was verified by designing a 10-bit 40Msample/second hybrid ADC using TSMC 90nm IO device process. This hybrid ADC uses op-amp sharing method to save half number of stages, and, it can work in two modes: pipelined ADCs for high speed, cyclic ADC for low speed (only last stage runs, other stages are power off to save power).It also adapts dynamic biasing methods, so, for pipeline mode, the total power consumption decrease as the sampling frequency drops.

The pipelined ADC is the architecture of choice for sampling rates from a few Msps up to 100Msps+. Design complexity increases only linearly (not exponentially) with the number of bits, thus providing converters with high speed, high resolution, and low power at the same time. Pipelined ADCs are very useful for a wide range of

applications, most notably in digital communication where a converter's dynamic performance is often more important than traditional DC specifications like differential nonlinearity (DNL) and integral nonlinearity (INL). The data latency of pipelined ADCs is of little concern in most applications. Maxim continually develops new converters for its portfolio of pipelined ADCs.

These pipelined ADCs nicely complement its ADC families designed with other architectures. The pipelined ADC design was achieved by initially analysing the different options regarding the overall structure. The 1.5-bit stage resolution is chosen in order to accommodate the speed requirements. The final overall structure is with 8 1.5-bit stages and one 2-bit stage, so that digital error correction can be applied. Further analysis of the structure of the stage structure concluded that an redesign of the traditional structure into a subADC/MDAC structure would be advantages. Generally the design is fully differential in order to compensate for offset errors and other limitations.

Modem portable and wireless applications are driving ADC design towards higher resolution and data rates with dramatically low power in scaled CMOS technology. Pipelined ADCs have been facing significant challenges with technology scaling since accurate residue amplification in each pipelined stage based on op-

amplifier's property is required. SAR ADC can benefits from the scaled CMOS because it does not need amplifier and most of the parts, switched capacitors and comparator, are digitally operation. In the view point of power and area efficiencies, SAR ADC is better than pipelined ADC.

Comparators are crucial building blocks in most ADCs system. Mismatches due to feature scaling, process variation and input-referred supply noise cause offset that directly affects the resolution of a comparator and thus has a crucial influence on the overall performance of the ADCs. This work explores a dynamic offset control technique that employs charge compensation by timing control. The charge injection and clock feed-through by turning off the latch reset transistor are investigated. A simple method is proposed to generate offset compensation voltage by implementing two source-drain shorted transistors on each regenerative node with timing control signals on their gates. The principle of timing based charge compensation approach for comparator offset control is described. The relationship between the offset control and slew rate of the timing control is analyzed based on simulation results. Proposed technique is confirmed by a 1GHz comparator fabricated in 65mn CMOS with 1.2V power supply. The comparator occupies 25 x 65 μm^2 and consumes 380 μW. 40mV offset is controlled. Proposed timing based dynamic

offset control technique for regular comparators has also been utilized by designing a 9-bit 50MHz split CDAC based SAR ADC with a foreground calibration. This technique might be used in isolation or in combination with the other offset techniques in ADC design. On the other hand, the proposed technique has some limitation since is sensitive to the timing control. Carefully design efforts is needed for the timing control circuits, since timing jitter and timing mismatch caused by PVT variation will affects the offset control range, resolution and degrades the dynamic performance.

The conventional architectural implementation of a SAR ADC and its switching algorithm are reviewed and discussed. Even though the SAR architecture is very energy efficient and has high compatibility with deeply scaled digital technologies, the accuracy and speed of the conversion process is still limited by capacitor mismatch and incomplete DAC settling clue to its high switching activities. Redundancy has been introduced to resolve both issues. We are able to show that redundancy (or sub radix-2) search is able to provide the additional information needed for digital calibration. Conditions for digital calibratability are also discussed and derived. In general, missing codes in the input-output transfer function can be digitally corrected while missing levels cannot. Smaller radix and more conversion steps are needed to tolerate

larger expected mismatch. Moreover, using redundancy, the DAC and comparator pre-amplifier settling errors made in the earlier conversion steps can be corrected in the later step. This means that if designed correctly, even though redundancy requires more conversion steps, each step takes much less time and the overall conversion speed can be improved.

We have designed and developed a high-performance SAR ADC architecture that achieves both high speed and high reliability – ideal for automotive, high speed controls and signal processing applications such as hard-disk-drive read channel wireless receivers and digital audio applications etc. ADC results of 12 bit prototype are presented.

Implementation of SAR algorithm in Microcontroller has reduced the hardware requirement and cost. We further plan to implement this architecture and algorithm efficiently on an IC.

It has been shown that digital assistance significantly changes the design tradeoffs in analog to digital converters. Comparator calibration shifts accuracy constraints from offset to noise which significantly reduces comparator power consumption and input capacitance. In addition, comparator calibration allows some alternative architectures that potentially further increase power efficiency. In amplifiers, digital assistance relaxes requirements on

linearity and gain precision and shifts the critical requirement to input referred noise. In addition to lowering power consumption in conventional amplifiers, this opens up many alternative amplifier topologies. In DACs, digital assistance can be used to reduce required area for a matching level, which is potentially useful at high resolutions.

Some of these concepts have been illustrated in the design of an interleaved 410 MS/s 11 bit pipelined SAR ADC enabled by digital assistance. A SAR architecture leveraging comparator offset calibration, residue amplifier gain calibration, channel gain calibration and channel offset compensation are assumed during the design phase to relax analog requirements.

In summary, the primary advantages of SAR ADCs are low power consumption, high resolution and accuracy, and a small form factor. Because of these benefits, SAR ADCs can often be integrated with other larger functions. The main limitations of the SAR architecture are the lower sampling rates and the requirements that the building blocks, the DAC and the comparator, be as accurate as the overall system.

Further research will focus on optimization design of real A/D converter from both the architecture and the circuit standpoints alone with the calibration techniques, interleave and interpolation

techniques to achieve high linearity, high dynamic range, and high sampling speed simultaneously under low supply voltages in deep-submicron CMOS technology with low power consumption.

Although this prototype SAR ADC is able to achieve the best FoM for any ADC reported to date that has higher than 10MS/s sampling rate with more than 10b ENOB, there are still many opportunities for improvement. The main goal is to push the SAR architecture to achieve higher resolution with higher sampling rates, while still being able to achieve low power consumption. Using the same calibration technique and design principles, we are able to demonstrate, in simulation, that the calibration algorithm can calibrate for ADCs with resolution between 12b and 16b.

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