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VLSI Implementation of Digital Keying Techniques Using VHDL

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Abstract— VHDL implementation of digital keying techniques is presented here. The blocks needed for generating binary amplitude shift keying (BASK), binary frequency shift keying (BFSK) and binary phase shift keying (BPSK) were designed, coded and simulated. A programmable read only memory (PROM) is also designed to store binary data. The blocks were coded in VHDL language and simulated using ModelSim tool. The proposed designs are focused at an academic objective of a course in digital communication.

Index Terms— BASK, BFSK, BPSK, digital data, multiplexer, parallel in serial out shift register, programmable read only memory, VHDL, VLSI.

1 Introduction

Nowadays very large scale integration (VLSI) is gaining appreciable attention in communication areas. Communication devices are now fabricated using VLSI technology which makes those devices portable, power efficient and small in size [5]. Digital keying techniques play an important role in communication. The binary message signal is modulated using sinusoidal carrier and is transmitted for long distance communication.

Modulation is the process of changing the characteristics of a high frequency carrier signal with respect to the amplitude of a low frequency message signal. The characteristics can be amplitude, frequency or phase. In digital keying process the message signal will be a binary data (0 or 1) and the carrier will be a sinusoidal one. In this modulation technique the characteristics (amplitude, frequency or phase) of high frequency sinusoidal carrier varies in accordance with the digital data, depending on whether the binary data is logic 0 or logic 1.

Digital modulation is preferred to analog one because it is simple, efficient and more secure compared to analog techniques [1].

The aim of this paper is to design and simulate three digital keying techniques; BASK, BFSK and BPSK. The demonstration of these digital keying techniques is important in academic curriculum of a technical course especially in a course for digital communication [4].

2 Theory of Digital Keying Techniques

2.1 Binary Amplitude Shift Keying

Binary amplitude shift keying (BASK) is a digital modulation technique in which the amplitude of the carrier is varied in accordance with the instantaneous value (amplitude) of the message signal (digital data), while the frequency and phase are kept constant.

A sample of the binary data and the corresponding BASK waveform is shown in figure.1

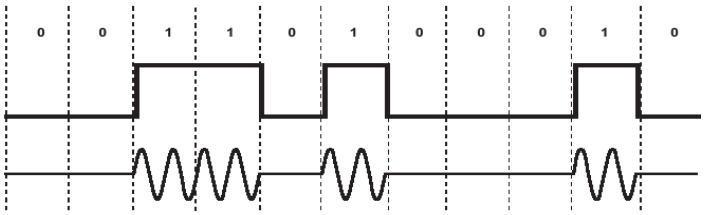

Figure.1 The digital data (00110100010) and the corresponding BASK waveform

2.2 Binary Frequency Shift Keying

Binary frequency shift keying (BFSK) is a digital modulation technique in which the frequency of the carrier is varied in accordance with the instantaneous value (amplitude) of the message signal (digital data), while the amplitude and phase are kept constant.

A sample of the binary data and the corresponding BFSK waveform is shown in figure 2.

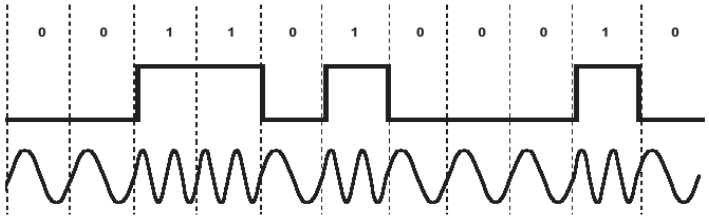

Figure.2 The digital data (00110100010) and the corresponding BFSK waveform

2.3 Binary Phase Shift Keying

Binary phase shift keying (BPSK) is a digital modulation technique in which the phase of the carrier is varied in accordance with the instantaneous value (amplitude) of the message signal (digital data), while the amplitude and frequency are kept constant.

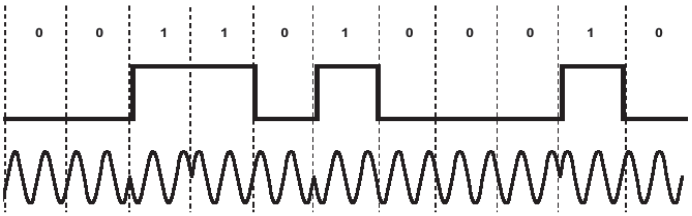

Figure.3 The digital data (00110100010) and the corresponding BPSK waveform

A sample of the binary data and the corresponding BPSK waveform is shown in figure 3.

3 Design of Digital Keying Techniques

3.1 BASK Design

The building blocks of binary amplitude shift keying (BASK) constitutes a sine wave generator [3], a programmable read only memory (PROM), a parallel in serial out shift register (PISO) and a 2:1 multiplexer (MUX). The proposed design for generating BASK signal is shown in figure 4.

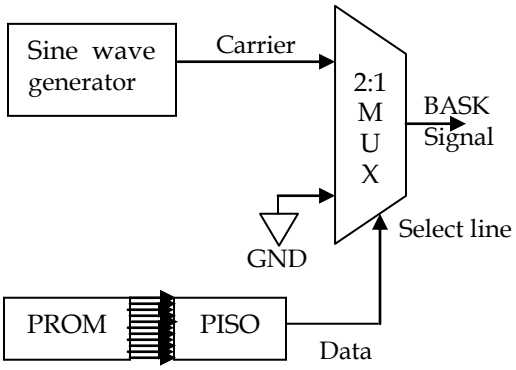

Figure.4 BASK Signal Generation

The sine wave generator will generate the 16-bit carrier and is given to one of the inputs of the 2:1 multiplexer and the other input is grounded. A programmable read only memory (PROM) is designed to store the 16-bit digital data (modulating signal). The data is moved from PROM to a PISO register which will convert the 16-bit parallel data into serial one. Now these serially out bits can be applied to the select line of the multiplexer. Depending on this digital data the multiplexer selects either the analog carrier or the grounded input and forwards it to the output. Hence the output of the multiplexer will be the carrier itself when the data is logic 1 and will be zero when the data is logic 0 [2]. Thus the carrier gets modulated depending on the digital data at the select line of the multiplexer.

3.2 BFSK Design

The building blocks of binary frequency shift keying (BFSK) constitutes two sine wave generators of different frequencies, say F_1 and F_2, a programmable read only memory (PROM), a parallel in serial out shift register (PISO) and a 2:1 multiplexer (MUX). The proposed design for generating BASK signal is shown in figure 5.

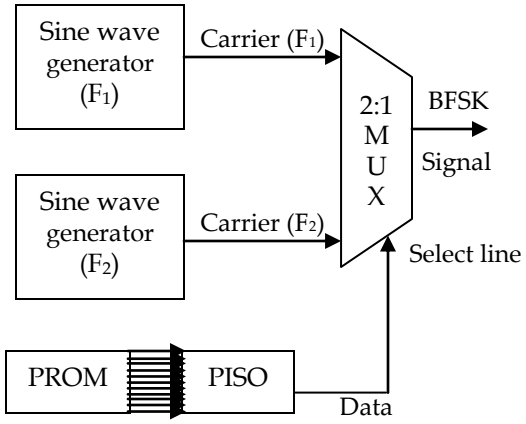

Figure.5 BFSK Signal Generation

The sine wave generators will generate two 16-bit carriers of frequencies say F_1 and F_2. The carrier with frequency F_1 is given to one of the inputs of the 2:1 multiplexer and the carrier with frequency F_2 is given to the other input. The programmable read only memory (PROM) will store the 16-bit digital data (modulating signal). The data is moved from PROM to a PISO register which will convert the 16-bit parallel data into serial one. Now these serially out bits can be applied to the select line of the multiplexer. Depending on this digital data the multiplexer selects either the analog carrier with frequency F_1 or the carrier with frequency F_2 and forwards it to the output. Hence the output of the multiplexer will be the carrier with frequency F_1 when the data is logic 1 and will be the carrier with frequency F_2 when the data is logic 0. Thus the carrier gets modulated depending on the digital data at the select line of the multiplexer.

3.3 BPSK Design

The building blocks of binary phase shift keying (BPSK) constitutes a sine wave generator, an inverter, a programmable read only memory (PROM), a parallel in serial out shift register (PISO) and a 2:1 multiplexer (MUX). The inverter is used to generate a signal with 180^o phase shift. The proposed design for generating BASK signal is shown in figure 6.

The sine wave generator will generate the 16-bit carrier with 0^o phase shift and is given to one of the inputs of the 2:1 multiplexer. The same 16-bit carrier is given to an inverter to produce 180^o phase shift and the inverter output is given to the other input terminal of the multiplexer. A programmable read only memory (PROM) is designed to store the 16-bit digital data (modulating signal). The data is moved from PROM to a PISO register which will convert the 16-bit parallel data into serial one. Now these serially out bits can be applied to the select line of the multiplexer. Depending on this digital data

the multiplexer selects either the analog carrier with 0º phase shift or the carrier with 180º phase shift and forwards it to the output. Hence the output of the multiplexer will be the carrier with 180º phase shift when the data is logic 1 and will be the carrier with 0º phase shift when the data is logic 0. Thus the carrier gets modulated depending on the digital data at the select line of the multiplexer.

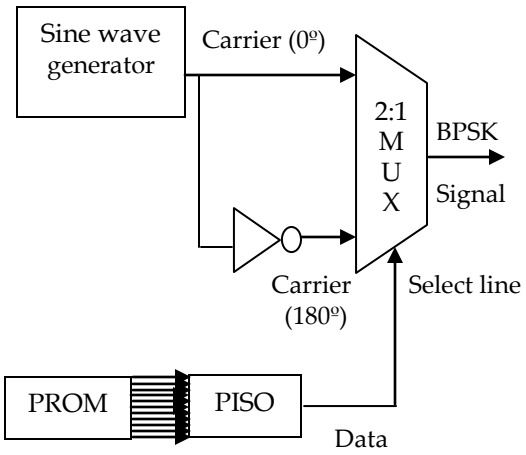

Figure.6 BPSK Signal Generation

4 Simulation Results

4.1 BASK Simulation Result

The simulation result of binary amplitude shift keying is shown in figure.7. From the figure it is clear that the output is zero when the data is low and the output is the sinusoidal carrier itself when the data is high.

Figure.7 BASK Simulation Result

4.2 BFSK Simulation Result

The simulation result of binary frequency shift keying is shown in figure.8. It can be seen from the figure that the output is a particular frequency say F_1 when the data is low and the output is another frequency F_2 when the data is high.

Figure.8 BFSK Simulation Result

4.3 BPSK Simulation Result

The simulation result of binary frequency shift keying is shown in figure.9. It can be visualized from the figure that the output is the carrier with 0º phase shift when the data is low and the output is carrier with 180º phase shift when the data is high.

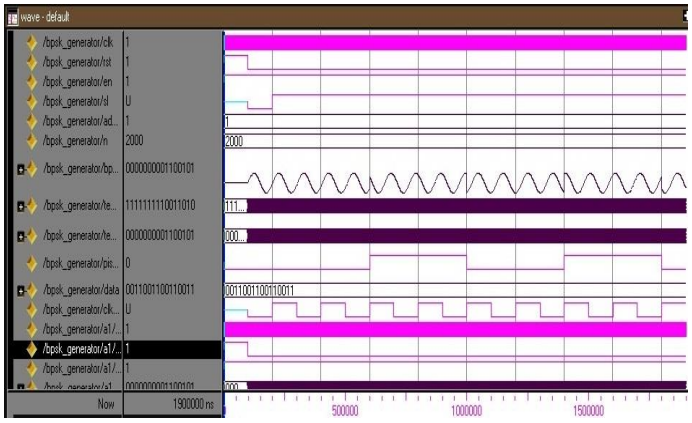

Figure.9 BPSK Simulation Result

5 Conclusion

In this proposed method the 16-bit digital data is stored in a programmable read only memory. This data is then converted into serial bits with the help of a parallel in serial out shift register. These serial data bits are applied to the select line of the multiplexer based on each clock pulse. Depending on these

data bits the 16-bit carrier gets modulated. Here we do not have to enter the data manually. The data is automatically taken from the designed memory. Hence the time required to enter the 16-bit data manually is saved.

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