The Study of ESD Robustness of Integrated Circuits with Standard TLP

M. Lally, M. Ahuja, B. Mehria

Abstract— In this work the ESD performance of BCD technology will be investigated at circuit level. Different types of structures and the layout effect on ESD robustness will be addressed. The correlation between ESD robustness obtained with different test methods (HBM and TLP) will be also presented.

Index Terms— ESD, ruggedness, protection, integrated circuit

1 INTRODUCTION

Electrostatic discharge (ESD) is one of the major issues in the reliability of sub-micron electronics devices [1]. A very large body of research has been done in the development of suitable structures capable of protecting the integrated circuits from the ESD event. Semiconductor industry has been using transmission-line pulse (TLP) testing to characterize on-chip electrostatic discharge (ESD) protection structures since 1985. This TLP ESD testing technique was introduced by Maloney and Khurana as a tool to test the many single elements used as ESD protection structures [2]. Since then, the technique has been shown to be most useful as a means for fast development of protection circuits, as well as other applications such as the study of fast transient effects like the diode's reverse recovery [3], [4]. A TLP test unit employs a rectangular pulse that resembles those used in human body model (HBM) ESD qualification testing. The length of the transmission line is the factor that controls the pulse width of the TLP. The pulse width is chosen to provide the same current-amplitude damage levels chosen to provide the same current-amplitude damage levels (electrical) as is found in HBM ESD stress testing. This allows for correlation between TLP (that usually has a pulse width of 75-200 ns) and HBM (with a a 150 ns, double exponential pulse width) [5]. The correlation is established through the TLP current and the assumed HBM peak current, i.e. Vhbm [V] + 1500O [6].

Several data sets have been published in the past concerning the properties and robustness of protection structures based on diodes, grounded gate nMOS Iransistors (gg-nMOST) and SCRs [2] suitable for digital circuit applications. Few data however are available concerning Smart-Power technologies which deal with high output voltages. The correlation between the results obtained by means of the more standard methods like Human

Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM) and TLP is still under discussion [7]. In this work a berif study of power protection structures that might be suitable for integrated circuits will be presented. The comparison of the ESD robustness of different structures (devices with the base located either in a p-body layer in a p-well layer, see Fig.l) and the influence of layout parameters on the ESD performances will be presented. It will be shown that, if the failure criteria address hard failures only, a good correlation between ESD robustness obtained with HBM and the TLP is verified.

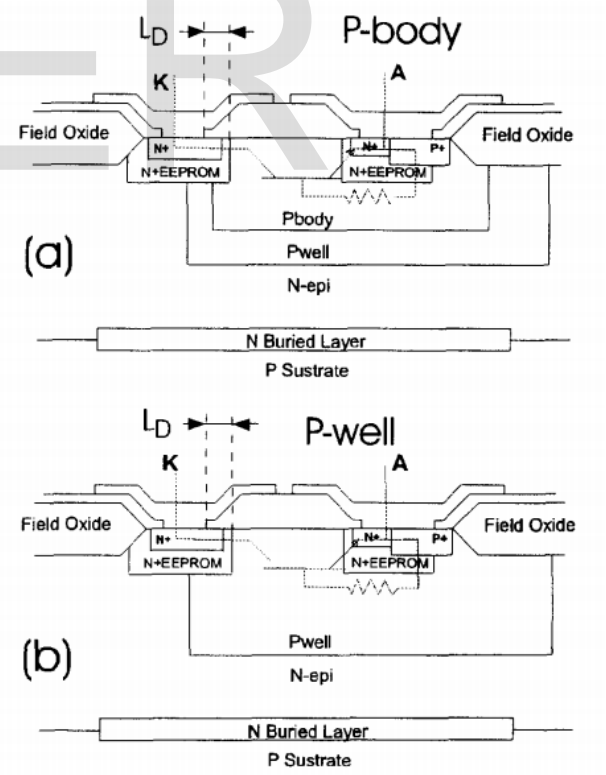

Fig. 1. Schematic cross section of the tested devices: (a) p-body base npn lateral bipolar transistor, (b) pwell base npn lateral bipolar transistor.

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2 EXPERIMENTAL

A schematic cross section of the devices studied in this work is

demonstrated in Fig. l (a) and (b). These structures are processed with a 1 um smartpower BCD technology (BCD is for Bipolar, CMOS and DMOS). The active protection device is a lateral NPN bipolar transistor with the base corresponding to the p-body region in one case, see Fig. l (a), or with the p-well region in the other one, see Fig.l (b). The two layout parameters investigated are: devices width, W, and the, distance between the collector contact to the end of the n-EEPROM collector diffusion, LD. (see Figs l (a) and (b)). Values for W are 50, 100, 150 and 200 #m, values for LD are: 7, 10 and 15 ~xm. The ESD robustness of the studied devices has been tested by means of the Human Body Model (HBM) test and Transmission Line Pulse (TLP) test. The HBM ESD stress test has been carried out by means of a Keytek Zapmaster using the HBMllC Module and following the specification reported in the EOS/ESD Association standard. The TLP Characterization has been carried out using a TLP tester capable of providing rectangular pulses of lOOns - 1~ width with a sub-nanosecond rise time and variable amplitude up to 4 A. A very schematic description of the TLP system together with the tipical output characteristics are depicted in Fig.2.

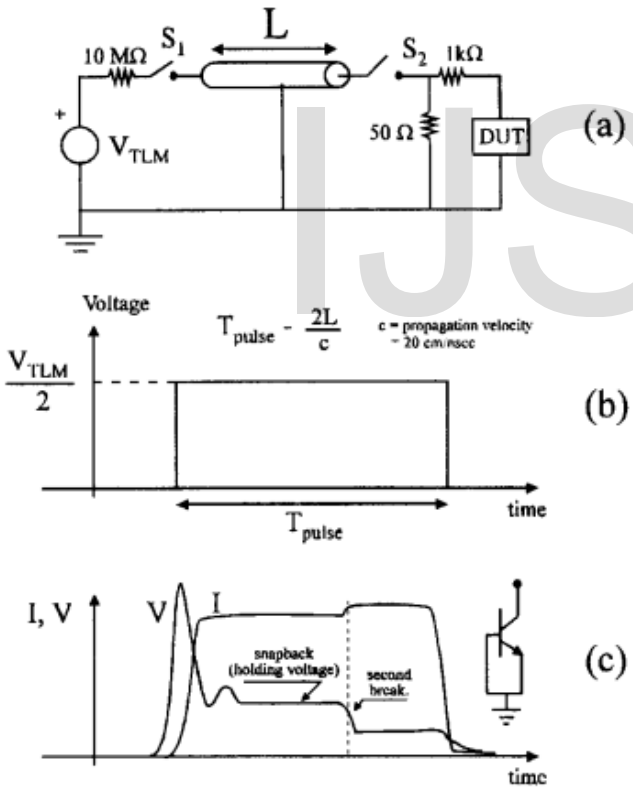

Fig. 2. Transmission line pulse set-up: (a) circuit model; (b) voltage pulse across the 1 k.Q serie resistance and the device under test; (c) current and voltage waveform in a typical protection structure (bipolar) during a pulse.

The TLP characterisation of ESD-protection structures is readily used as an alternative to less informative HBM tests [2]. The TLP chamcterisation of an ESDprotection element (device under test, DUT) provides not only the failure currenL but identifies also the holding voltage and the quasi-static differenlial resistance in the high-current regime. Both are key parameters for the DUT and determine the protection behaviour of the device. Furthermore, due to its comparable simple two-pin set-up, TLP can be applied at wafer level.

That particularly makes this method so valuable in the early stage of technology development, where a great number of wafers with splitted technology parameters should be characteFised. However, since the ESD qualification standard is the HBM testing as deemed in MIL-STD-883C method 3015.7 one has to assure the correlation of the ESD-failure thresholds obtained with HBM and TLP before trying to obtain any information on the ESD sensitivity simply from TLP characterisations.

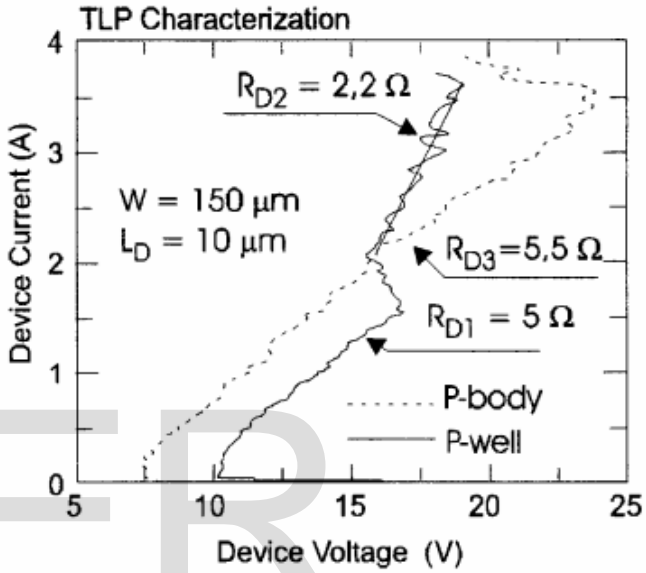

Fig. 3. Mesured I-V characteristics plot

3 RESULTS

Figure 3 shows the quasi static I-V curves obtained by using the TLP system in both p-well and p-body devices (W=150 um, LD = 10 um). The presence of an anomalous snap-back in the I-V curves of the p-well device can be observed; the dynamic resistance, Rm, changes from about 5 ohm to R_{D2} ,~ 2 ohm when the current is beyond 2 A, possibly due to the turn-on of a vertical npn bipolar transistor. The values of the Rm and R_{D2} resistance for all the different p-well device layout is reported.

In Table I. The p-body device instead shows a more conventional behavior with a dynamic resistance R_{D3} = 4.7 ohm. The values of the R_{D3} resistance forall the different p-body device layout is reported in Table II. The resistance values of all the tested devices decreases both on increasing the device width and on decreasing the distance between the collector contact to the end of the n-EEPROM collector diffusion, LD.

The behavior of the leakage current during the TLP ESD stress test of a typical device is reported in Fig.4. During this procedure, the TLP stress current level is increased from 0.1 A to the hard failure (3.5 A in this case). At each step the device leakage current (at 5.5 V) is measured after having applied the

Table I: Dynamic Resistances R_{D1}, R_{D2} (Ω)

	Lateral npn P-Well		
	W=50 µm	W=100 µm	W=150 µm
L_D=7 µm	R_{D1} = 12.9 R_{D2} = 5.18	6.12 2.7	4.1 1.5
L_D=10 µm	13.63 6.37	6.79 2.6	5 2.2
L_D=15 µm	15.24 7	8.03 4.12	5.6 3.4

Table II: Dynamic Resistances R_{D3} (Ω)

	Lateral npn P-Body		
	W=50 µm	W=100 µm	W=150 µm
L_D=7 µm	12.2	6.1	4.6
L_D=10 µm	13.2	6.7	4.7
L_D=15 µm	14.9	7.7	5.5

TLP having applied the TLP ESD stress current pulse to the device under test. The pwell devices tipically show a slight increase of the leakage current after ~ 2 A TLP current pulse. This is normally indicated as "soft-failure" since the device is slightly damaged but considered still good. After the 3.5 A TLP current pulse the device presents an increase of the leakage current beyond the failure threshold, hence a "hard failure" is present. This value define the ESD TLP robustness of the device. The p-body devices during the ESD TLP test show only "hard" failures (at about 3.5 A), see Fig.4.

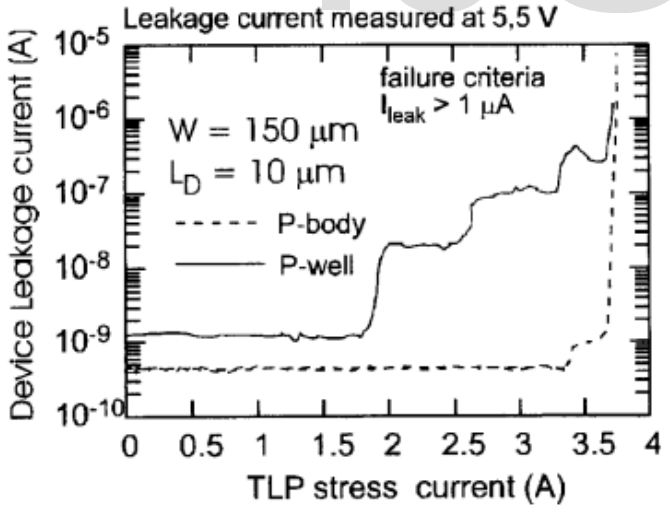

Fig. 4. Device leakage current during TLP stress test

The ESD robustness of p-body devices is shown in Fig.5, for both I-IBM (open symbols) and TLP (closed symbols) tests for devices with different W and Lb. Since the TLP system gives a current level of ESD robustness while the HBM tester provide a voltage level of ESD robustness, in order to compare the two tester the HBM voltage has been converted in I-IBM current. To do that the voltage obtained with the HBM tester has been divided by the 1.5 kohm. This considering that the dynamic resistance of the device, that is in the order of few ohms, is negligible if compared with the 1.5 kohm resistor of the HBM tester [7].

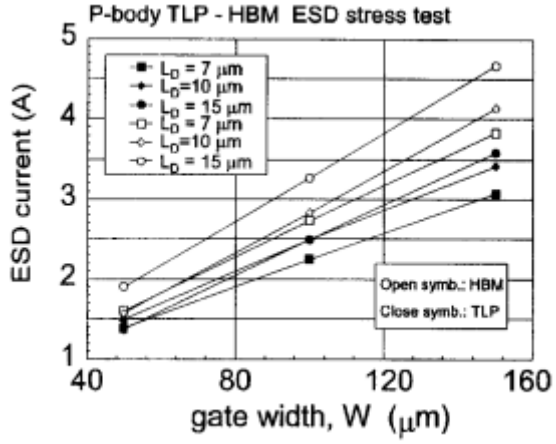

Fig. 5. ESD failure level measured with TLP and HBM tester for different p-body device geometry.

4 Conclusion

The ESD robustness of p-body and p-well lateral NPN bipolar Iransistor have been studied in this work. It has been found the the roboustness of these device scale with their width. However, in p-well structures soft failures are observed and the ESD robustness does not scale perfectly with device width, possibly due to current crowding caused by the soft failures. Better ESD performances and absence of soft failures have been observed in the p-body devices.

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