Novel Low Power and High Speed 8T Full Adder

Shrikant M Pattar, H V Ravish Aradhya

Abstract - Full adder (FA) is an essential component for the design and development of all types of processors viz. digital signal processors (DSP), microprocessors etc. Adders are the core element of complex arithmetic operations like addition, multiplication, division, exponentiation etc. In most of these systems adder lies in the critical path that affects the overall speed of the system. So enhancing the performance of the 1-bit full adder cell is a significant goal. Thus in this work 8 transistors full adder (8T FA) is proposed which addresses the discharging problem at the carry output for the particular combinations of the inputs in the existing 8T FA. The proposed 8T full adder is implemented using the 90nm technology library and is simulated & verified using the Cadence spectre simulator. Further the proposed full adder is compared with some other existing full adder designs such as conventional CMOS FA, 10T FA, 16T FA and static energy recovery full adder. And it observed from the simulation results that the proposed 8T full adder outperforms the other existing full adders in terms of power consumption, delay PDP (power delay product) and transistor count.

Index Terms - *Full adder, 8T FA, DSP, microprocessor, arithmetic operations, low power and PDP.*

I INTRODUCTION

The continuing decrease in transistor feature size (transistor channel length) and corresponding increase in chip density and operating frequency have inspired VLSI (Very large scale integrated circuits) designer to give a primary importance for the power consumption in VLSI circuit design. In the past, VLSI designer used to consider area, performance, cost and reliability as primary parameters. There was a secondary importance for power consumption. But nowadays, the demand for power-sensitive designs has been increasing tremendously. This increasing demand has mainly been due to the fast growth of portable electronic devices such as smart phones, notebook and laptop computers, PDA and other portable communication devices which require high speed and complex functionality computations with lower power consumption. Excessive power dissipation in integrated circuits discourages their use in these portable device applications. High power systems often run hot, and this increment in temperature tends to failure in several silicon components. To control the temperature levels, the chip need specialized and costly packaging and cooling arrangements, which would result in further increase in the system cost. These impacts of high power influenced the VLSI designers towards the optimization of power consumption in a chip. So, the low power design is critical these days in the semiconductor industry. Simultaneously, we also need to reduce the delay of the critical paths of the circuits, while reducing its power consumption.

The total power dissipation in a circuit consists of two components, namely, the static and dynamic power dissipation. Dynamic power constitutes the major part of the power dissipated in complementary metal oxide semiconductor (CMOS) VLSI circuits. It is the power dissipated during switching activity i.e charging or discharging of the load capacitance of a given circuit. And static power is due to the leakage current through the short circuit transistors and also due to the sub threshold leakage current. And this static power can be eliminated by proper sizing of the pmos and nmos tranistors. The average power dissipated in a generic digital CMOS gate is given by:

$$P_{avg} = P_{dynamic} + P_{static} \quad (1)$$

Where, Pdynamic is dynamic and Pstatic is the static power.

Power can be minimized at different levels at either system level or architecture level or algorithm level or micro architecture level or gate level or circuit level. Here an attempt is made to reduce the power at circuit level.

In digital adders, the speed of addition is limited by time required to propagate a carry through the adder. The sum of each bit position in an elementary adder is generated sequentially (starting at the lowest order bit position) only after the previous bit position has been summed and a carry (if generated) propagated into next position [1].Despite the simplicity of adding two binary numbers, there exist several adders based on very different design ideas. Thus if one need to implement an addition circuit one must decide which circuit is most appropriate for its planned application. There are many binary adder architecture ideas to be implemented in such applications. In order to design these adders, single bit full adder is basic element. So, selection of 1-bit full adder based on power, delay and area is necessary to build other type of adder circuits.

In recent years, several variants of different logic styles have been proposed to implement full adder cells. There are two types of full adders, static and dynamic. Static full adders are generally more reliable, simpler and are lower power consuming than dynamic ones. A lot of work has been carried out for the optimization of low-power full adders, thus as a background for this work, different existing full adders is surveyed briefly as follows. K.M. Chu and D. Puffrey in [2] proposed the full adder which is based on Differential Cascode Voltage Switch Logic (DCVSL) style which consisting of 28 transistors and it uses separate modules to generate sum and carry results in faster but trades with area. N. Zhuang and H. Wu [3] proposed the TG full adder which comprises of 20 transistors designed using transmission gates and inverter. The TFA only consists of 16 transistors by employing pass transistors. The main

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disadvantage of these logic styles is that they lack driving capability. The strategy employed by E. Abu-Sharma [4] consists of a 14 transistor full adder based on the transmission gates logic, due to the non-zero standby power consumption at the intermediate node due to is due to threshold voltage loss that makes this circuit unsuitable for low power and low voltage applications. In [5] R. Zimmermann and W. Fichtner presented fully complementary static CMOS design which is made up of 28 transistors with sufficient driving ability but with area overhead. With an objective of further minimizing the transistor count, R. Shalem et.al in [6] proposed the pass transistor logic based static energy recovery full adder with as few as ten transistors. The Static Energy Recovery Full adder (SERF) cell uses only 10 transistors and it consumes less due to the absence of supply to ground path but it is not suitable for the high speed architectures due to the long delay as the sum is generated from two cascaded XNOR gates. Further in [7], A. M. Shams et.al derived the 16T full adder minimize the short circuit power dissipation of the 14T full adder proposed in [4]. The power consumption of this adder is better than the conventional CMOS design and other high gate count adders. But this design is still occupies significant amount of chip area. New 10T full adders proposed in [8] & [9] which consumes low power but do not provide full swing. Also in [10], 1-bit full adder cell featuring hybrid CMOS logic style is proposed. The new GDI (gate diffusion input) technique for low power design is proposed by Arkadiy et.al in [11] and is employed for designing fast, low-power circuits using lesser number of transistors. Liu, Hwang et.al minimized the threshold loss problem in a 10 transistor adder reported in [12] as a Complementary and Level Restoring Carry Logic (CLRCL) adder. In [13], Shubhajit Roy et.al proposed new 8 transistors full adder using novel 3 transistors XOR gate. This full adder consumes less power compared to existing full adder designs (such as C-CMOS, 10T, TFA full adder etc.) and also it occupies small chip area as it is built from less number of transistors. The new low power and high speed full adder is designed which targets at tree structured applications is proposed by Jian-Fei et.al in [14] which uses 20 transistors to achieve high driving ability and low power consumption. In [15] presented a two novel 1-bit full adder cells in dynamic logic style which leads to higher speeds than the other standard static full adder cells but consumes more power. Further the new high speed 8T floating full adder cell is presented by Nabiallah Shiri et.al in [16] it is so named as the internal nodes are not directly connected to the ground. So from this survey we understood that the different full adders are designed which have a tradeoff between power, area, speed and driving capability and these full adders are used in different application as per the requirement.

II. PROPOSED DESIGN

In this work, existing 8T full adder [13] is modified to address their discharging problem at the carry output for the particular combinations of the inputs. Before having a detailed understanding of working principle of proposed 8T full adder we need to be aware of the design and its working principle of the existing 8T full adder which is as shown in the Figure.1 and it is explained as follows. This full adder is designed using 3T XOR gates and is implemented using Boolean expressions for sum and carry as follows.

$$\text{Sum} = A \text{ xor } B \text{ xor } C \quad (2)$$

$$\text{Carry} = AB + BC + CA = AB + C(A \text{ xor } B) \quad (3)$$

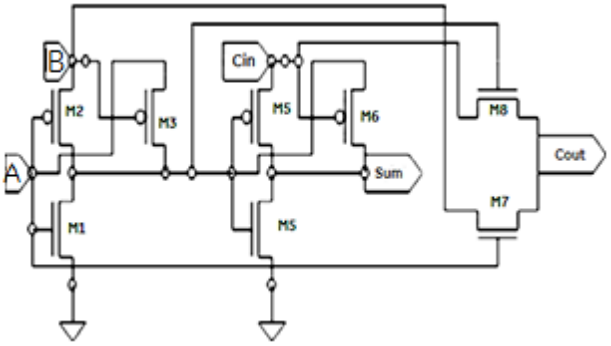

Figure.1 Existing 8T full adder

The discharging issue of the existing 8T full adder is discussed by referring the Figure.1 as follows. When A=1, B=0 and Cin=1 applied to the full adder, then carry output should be logic '1' and sum should be logic '0'. So in this case 'Cin' should be propagated through transistor M8 (refer Figure.1) and it should appear at the carry output Cout as the 'A XOR B' is logic '1'. But the existing 8T full adder produces carry output logic '0' because the transistor M7 is also switched on simultaneously with M8 because A=1 and B=0 combination switches on the nmos transistor M7 as input A is driving the gate and B input is connected to the source terminal of the M7, so it creates a ground path (discharging) for the carry output. Another problem in the existing 8T full adder is when A=0, B=0 combination is applied the carry output will be undefined.

So this issue is addressed in this proposed work by replacing the M7 nmos transistor with pmos transistor as shown in Figure.2 and driving the 'A xor B' intermediate signal to the gate terminal and feeding either one of the inputs A or B to the source terminal of new pmos transistor. So in this design, only one transistor among M7 & M8 will be switched on at once, thus the discharging path will never be created at the carry output, thus it proved that it provides proper sum and carry outputs for all the combinations of the inputs by the alleviating the discharging issue.

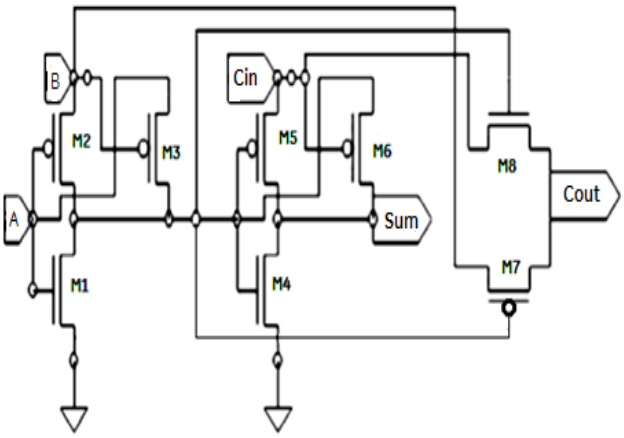

Figure.2 Proposed 8T full adder

III.RESULTS

Schematics for the designs are drawn in virtuoso ADE of Cadence, and all simulations are carried out using Cadence Spectre analyzer with 90nm Technology library at 1.8V Vdd. First the schematics for the existing and the proposed 8T full adder are drawn and the designs are simulated applying the stimulus as follows. Same input stimulus with the maximum frequency of 250MHz is applied to both existing and proposed full adder designs. Schematic & output waveform window for the existing 8T FA are as shown in Figure.3 and Figure.4 respectively.

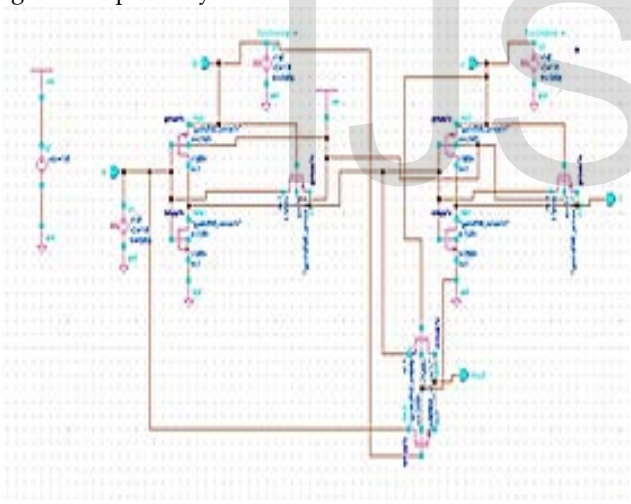

Figure.3 Schematic of existing 8T full adder

Figure 4 shows the output for the existing full adder which is obtained by the application of the stimulus and it is evident from the Figure 4 that there is a discharging issue at the carry output which is the first waveform the top in the waveform window when A=0, B=1 and C=1, it can be observed in the region highlighted between the vertical traces.

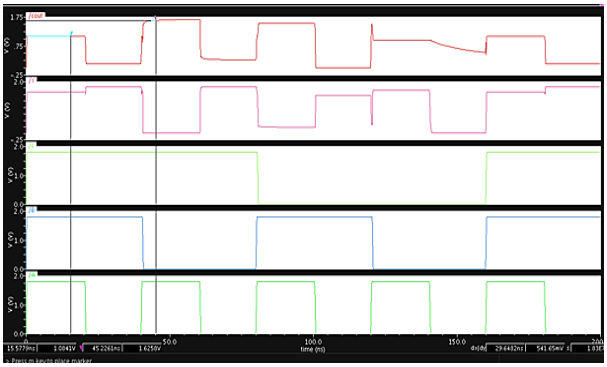

Figure.4 Output waveforms of existing 8T full adder

This problem is addressed in the proposed work and its schematic & output waveform window are as shown in Figure.5 and Figure.6 respectively.

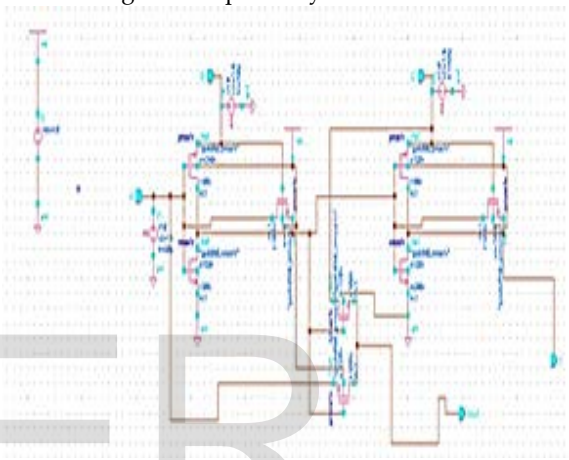

Figure.5 Schematic of proposed 8T full adder

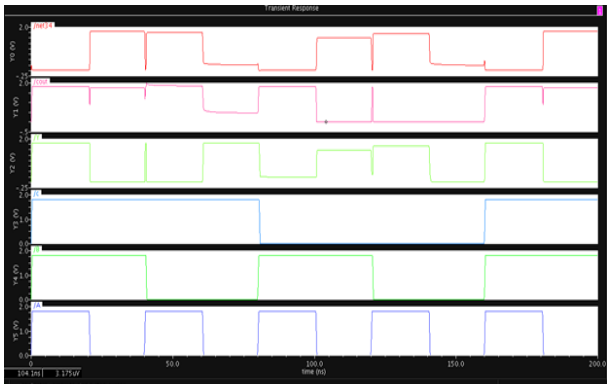

Figure.6 Output waveforms of proposed 8T full adder

The Figure 6 shows output for the modified 8T FA (full adder) which is obtained by the application of same stimulus as the existing 8T FA. And from Figure.6 it is verified that discharging problem is eliminated at the carry output by observing at the same region as for the existing, thus the modified 8T full adder produces proper outputs for all the combinations of the inputs.

Further, the proposed 8T full adder is compared with some of the existing full adders in terms of power, delay and power-delay product (PDP). In this work conventional

CMOS, 16T, 10T and SERF (static energy recovery) full adders are compared with proposed 8T full adder is given in Table.1 and Table.2.

These FA designs are simulated using spectre simulator of cadence tool. All the FA cells are implemented using 90nm gpdk technology with power supply set to 1.8V and maximum frequency is 250 MHz for the inputs. Propagation delay is measured from 50% of voltage level of input to 50% of voltage level of output.

Full adder designs	Average power (uW)	Delay (pS)	
		Sum	Carry
Conventional CMOS FA	6.718	75	42.4
10T FA	1.855	38.5	65.7
SERF	1.217	43.9	66.19
16T FA	0.614	41.7	28.15
Proposed 8T FA	0.117	34	28.13

Table.1 Power and delay comparison

FA / PDP(fJ)	Conventional CMOS FA	10T FA	SERF	16T FA	Proposed 8T FA
Sum	0.503	0.071	0.053	0.025	0.0039
Carry	0.284	0.121	0.080	0.017	0.0032

Table.2 PDP comparison for sum and Carry outputs

It is observed from the simulation results tabulated in the Table.1 that the proposed 8T FA consumes least power compared to all other full adders. And the proposed 8T FA comprises of least number of transistors compared to others so leads to smaller chip area. It is observed that the delay for sum and carry outputs also improved which in turns improves the PDP compared to other full adders which is given Table.2.

IV.CONCLUSION:

A novel 8T full adder to address the discharging issue in the existing 8T full adder is proposed. This proposed full adder which is implemented using the 90nm technology library is simulated and verified successfully using the Cadence spectre simulator. Further this full adder is compared with conventional CMOS, 10T FA, 16T FA and SERF full adders. From the simulated results it is observed that the proposed 8T full adder consumes least power, also the delay for the sum and carry outputs is less compared to other full adders. Thus it in turn improves the PDP compared to other full adder designs. Hence the proposed 8T full adder can be used for low power and high speed applications.

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