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Near State PWM Algorithm with Reduced Switching Frequency and Reduced Common Mode Voltage Variations for Vector Controlled Induction Motor Drive

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Abstract— In this paper a Near State Pulse Width Modulation (NSPWM) algorithm with reduced switching frequency is presented for vector controlled induction motor drives for reduced common mode voltage/currents. The proposed algorithm utilizes a group of three neighbor voltage vectors to construct the reference voltage space vector. In the proposed algorithm in each sector any one of the phases is clamped to either positive dc bus or negative dc bus. Hence, the proposed algorithm reduces the switching frequency and switching losses of the inverter. The simulation results illustrate that the proposed NSPWM algorithm results in reduced common mode voltage, has low switching frequency and has low switching losses of the inverter.

Index Terms—common mode voltage, induction motor drives, near state PWM, SVPWM, vector control.

1 INTRODUCTION

THE vector control methods are widely used for the control of induction motor drives in high-performance applications due to its advantages [1]. The vector control algorithm gives a decoupling control between torque and flux so that the induction motor can be controlled as a separately excited dc motor. However, the classical vector control algorithm uses hysteresis controllers for the generation of gating signals to the voltage source inverter (VSI), which results in variable switching frequency operation. To achieve constant switching frequency operation of the inverter, the space vector pulse width modulation (SVPWM) algorithm [2] has been used for vector controlled induction motor drive. Among the various possible PWM algorithms SVPWM gives superior performance and gives reduced harmonic distortion [3]. The SVPWM algorithm divides the zero voltage vector time equally among the two zero voltage vectors.

To reduce the harmonic distortion, the zero voltage space vectors are used in SVPWM algorithm, which results in large common-mode voltage (CMV) variations. The poor CMV characteristics lead to prohibitive amount of common-mode current (CMC) in induction motors. In induction motor drive applications, this may lead to motor bearing failures, electromagnetic interference (EMI) noise, or interference with other electronic equipment in the vicinity [4]-[5]. Such problems have increased recently due to increasing PWM frequencies and faster switching times. The filters can be utilized to suppress the effect of the CMV from the source. However, these methods involve additional hardware, and thus, they significantly increase the drive cost and complexity. An alternative approach is to modify the pulse pattern of the standard PWM algorithm such that the CMV is substantially reduced from its source and its effects are mitigated at no cost [9]-[11]. A novel remote state PWM algorithm is presented in [9] and a near state PWM (NSPWM) algorithm is presented in [10]. The detailed survey and analysis of various PWM algorithms has been carried out and proved that NSPWM algorithm gives superior performance when compared with the other PWM algorithms [11].

This paper presents space vector based NSPWM algorithm with reduced switching frequency for reduced CMV in vector controlled induction motor drives.

2 SVPWM ALGORITHM

Voltage source inverters (VSI) are utilized in many applications. The three-phase, two-level VSI has a simple structure and generates a low-frequency output voltage with controllable amplitude and frequency by programming high-frequency gating pulses. For a 3-phase, two-level VSI, there are eight possible voltage vectors, which can be represented as shown in Fig. 1. Among these voltage vectors, V_1 to V_6 vectors are known as active voltage vectors or active states and the remaining two vectors are known as zero states or zero voltage vectors. The reference voltage space vector or sample, which is as shown in Fig. 1 represents the corresponding to the desired value of the fundamental components for the output phase voltages. In the space vector approach this can be constructed in an average sense. The reference voltage vector (V_{ref}) is sampled at equal intervals of time, T_s referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different time durations with in a sampling time period such that the average vector produced over the sampling time period is

equal to the sampled value of the V_{ref}, both in terms of magnitude and angle. It has been established that the vectors to be used to generate any sample are the zero voltage vectors and the two active voltage vectors forming the boundary of the sector in which the sample lies. As all six sectors are symmetrical, the discussion is limited to the first sector only.

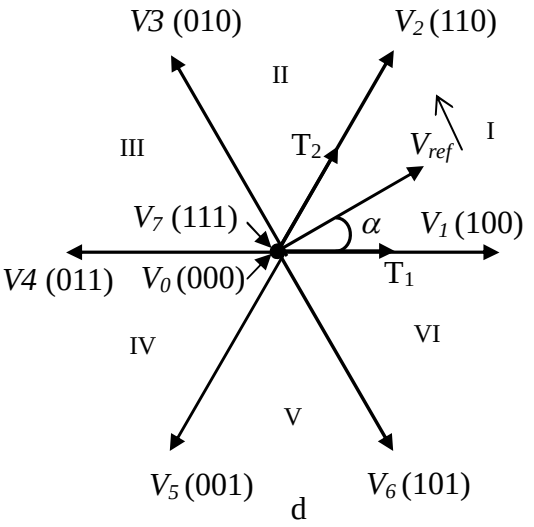

Fig. 1 Possible voltage space vectors and sector definition in SVPWM algorithm

For the required reference voltage vector, the active and zero voltage vectors times can be calculated as in (1), (2) and (3).

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \sin(60^o - \alpha) T_s \quad (1)$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \quad (2)$$

$$T_z = T_s - T_1 - T_2 \quad (3)$$

where M_i is the modulation index and defined as in [1]. In the SVPWM algorithm, the total zero voltage vector time is equally divided between V_0 and V_7 and distributed symmetrically at the start and end of the each sampling time period. Thus, SVPWM uses 0127-7210 in sector-I, 0327-7230 in sector-II and so on.

3 NSPWM Algorithm

The near state PWM (NSPWM) algorithm uses a group of three neighbor voltage vectors to construct the reference voltage vector. In order to reduce the common mode voltage variations, the proposed NSPWM algorithm did not use the zero voltage vectors. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors are utilized in each sector. Hence, the utilized voltage vectors are changed in every sector. As shown in Fig. 2, to apply the method, the voltage vector space is divided into six sectors. Here also, as all six sectors are symmetrical, the discussion is limited to the first sector only. For the required reference voltage vector, the active voltage vectors (V_1, V_2 and V_6) times can be calculated as in (4), (5) and (6).

$$T_1 = \left\{ -1 + \frac{3}{\pi} M_i \cos(\alpha + \frac{\pi}{3}) + \frac{3\sqrt{3}}{\pi} M_i \sin(\alpha + \frac{\pi}{3}) \right\} T_s \quad (4)$$

$$T_2 = \left\{ 1 - \frac{3}{\pi} M_i \cos(\alpha + \frac{\pi}{3}) - \frac{\sqrt{3}}{\pi} M_i \sin(\alpha + \frac{\pi}{3}) \right\} T_s \quad (5)$$

$$T_6 = T_s - T_1 - T_2 \quad (6)$$

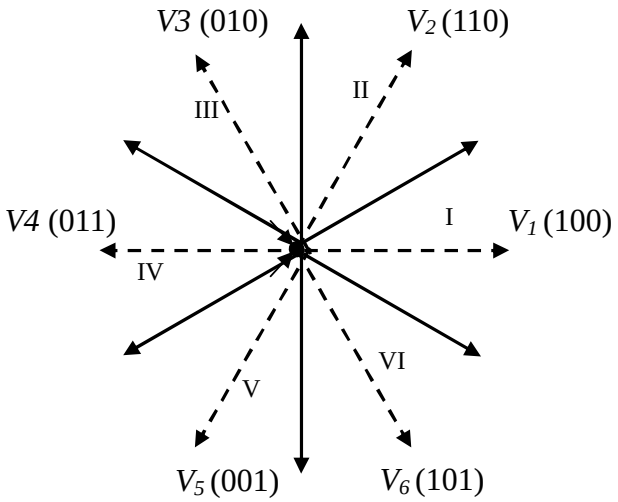

Fig. 2 Possible voltage space vectors and sector definition in NSPWM algorithm

But, in the NSPWM algorithm, the (4), (5) and (6) have a valid solution when the modulation index is varying between 0.61 and 0.906 [10]. In order to get minimum switching frequency and reduced common mode voltage the NSPWM algorithm uses 216-612 in sector-I, 321-123 in sector-II and so on.

The total number of commutations in SVPWM algorithm is three in a sampling time interval, where as the number of commutations in NSPWM algorithm is two. Moreover, the modulating waveform of NSPWM algorithm is similar to the DPWM1 waveform and hence any one of the phases is clamped to the positive or negative DC bus for utmost a total of 120^0 over a fundamental cycle. Hence, the switching losses of the associated inverter leg are eliminated. Hence, the switching frequency of the NSPWM algorithms is reduced by 33% compared with SVPWM algorithm.

4 NSPWM Algorithm Based Vector Controlled Induction Motor Drive

In the vector controlled induction motor drive, a VSI is

supposed to drive the induction motor so that the slip frequency can be changed according to the particular requirement. Assuming the rotor speed is measured, and then the slip speed is derived in the feed-forward manner. The block diagram of proposed vector controlled induction motor drive is as shown in Fig. 3. This shows how the rotor flux linkage position can be obtained by integrating the sum of rotor speed and actual speed. In the vector control scheme, to regulate λ_r and rotor speed to desired values are the two objectives.

ate the desired rotor flux linkage and rotor speed are not directly related to these variables. So the alternative way is to regulate the rotor flux linkage and rotor speed through PI controllers and the outputs of these two controllers give out the reference values for the q- and d-axis stator currents in synchronous reference frame. Then the actual q- and d-axis stator currents are regulated to these two reference currents to get the stator voltages. Then these two-phase voltages are converted into three-phase voltages and given to the RPWM block, which generates the gating pulses to the VSI.

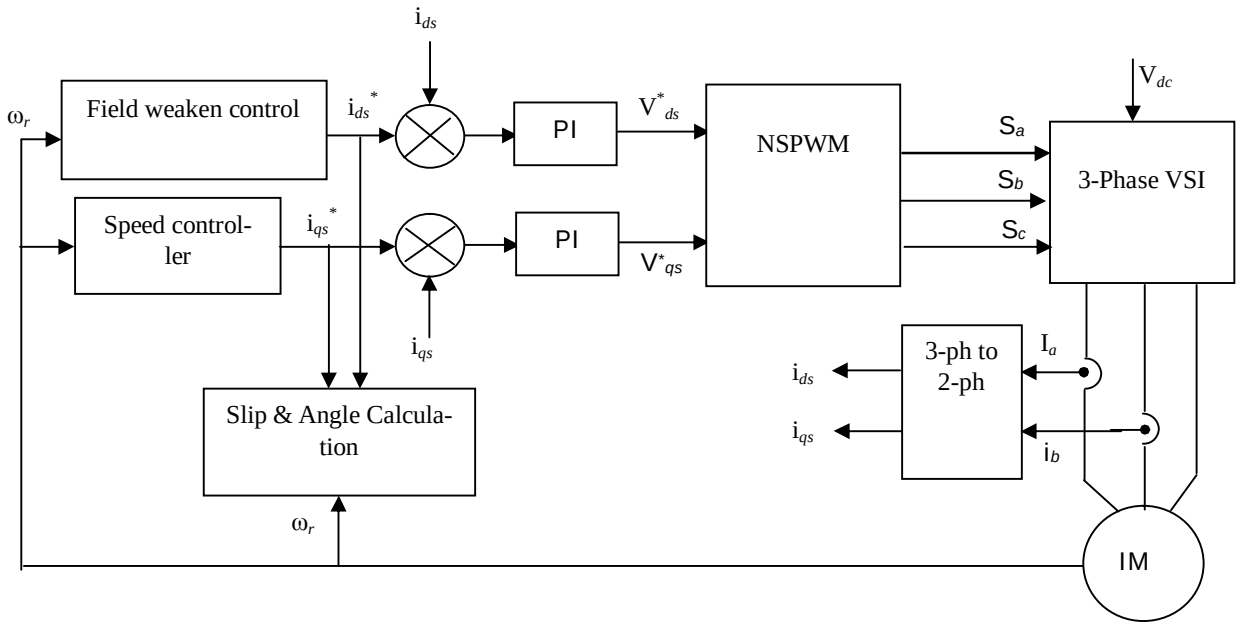

Fig. 3 block diagram of NSPWM based vector controlled I.M.drive

Apparently the stator voltages that are required to gener-

5 Simulation Results and Discussions

To validate the proposed NSPWM algorithm, the numerical simulation studies have been carried out using MATLAB. For the simulation studies, the average switching frequency of the inverter is taken as 5 kHz. In order to maintain the constant average switching frequency, the switching frequency of SVPWM algorithm is taken as 5 kHz and that of NSPWM algorithm is 7.5 kHz. The induction motor used in this case study is a 4 kW, 400V, 1470 rpm, 4-pole, 50 Hz, 3-phase induction motor having the following parameters: R_s= 1.57Ω, R_r = 1.21Ω, L_s = 0.17H, L_r = 0.17H, L_m = 0.165 H and J = 0.089 Kg.m^2.

The simulation results of SVPWM algorithm based vector controlled induction motor drive are shown in Fig.4-Fig. 7.

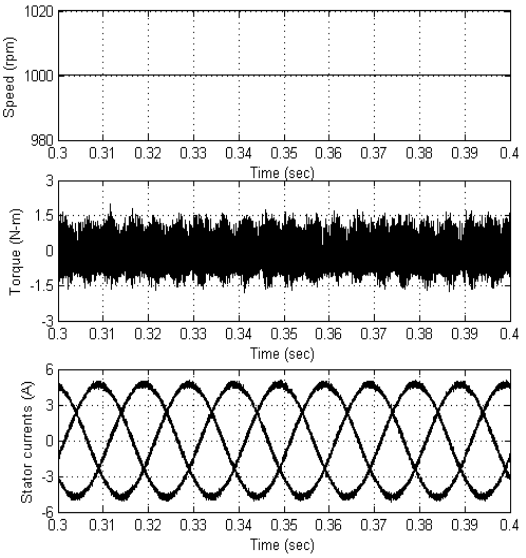

Fig. 4 Steady state plots of SVPWM algorithm based vector controlled induction motor drive

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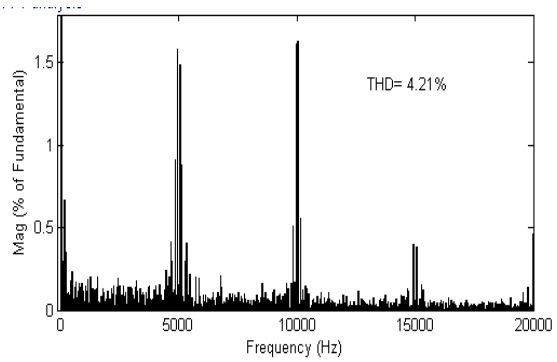

Fig. 5 Harmonic spectra of line current in SVPWM based vector controlled induction motor drive

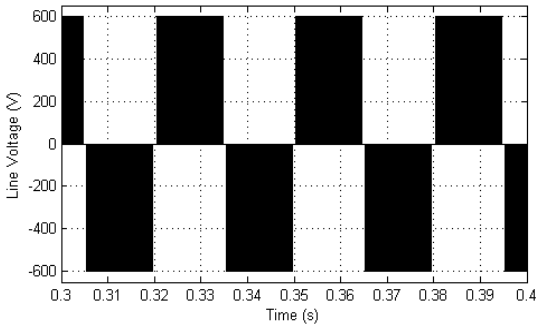

Fig. 6 Line voltage waveform of SVPWM algorithm based vector controlled induction motor drive

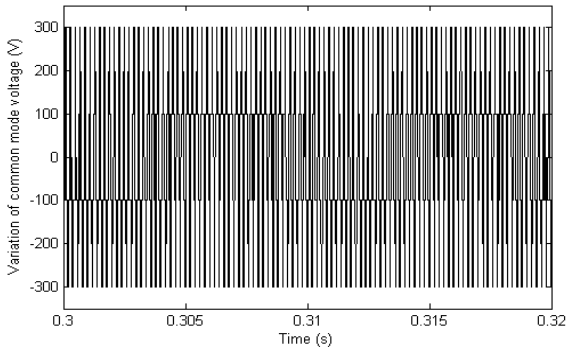

Fig. 7 Common mode voltage variations in SVPWM algorithm based vector controlled induction motor drive

Fig.4 shows the steady state plots of vector controlled induction motor drive. Fig. 5 shows the harmonic spectra of line current along wth the THD value.Fig. 6 shows the line voltage waveform of SVPWM algorithm based vector controlled induction motor drive in steady state and Fig. 7 shows the common mode voltage variations with the SVPWM algorithm, from which it can be observed that the common mode voltage is varying between $+0.5V_{dc}$ and $-0.5V_{dc}$. the simulation results of NSPWM algorithm based drive are shown from Fig. 8 to Fig. 11.

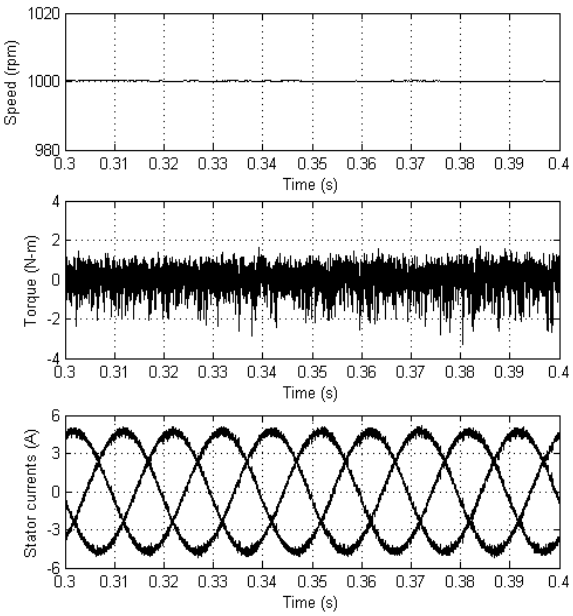

Fig. 8 Steady state plots of NSPWM algorithm based vector controlled induction motor drive

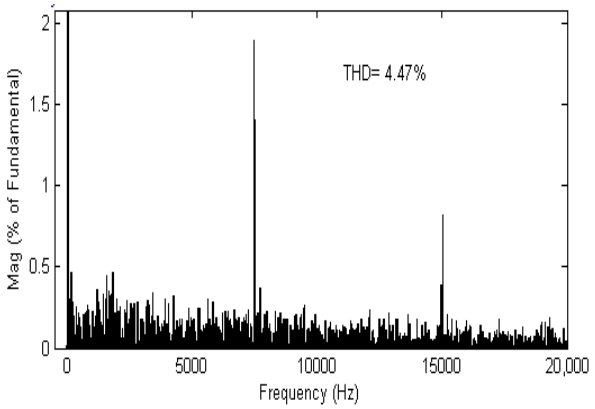

Fig. 9 Harmonic spectra of line current in NSPWM algorithm based vector controlled induction motor drive

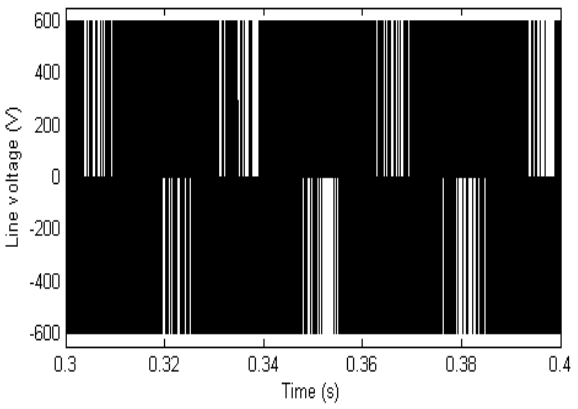

Fig. 10 Line voltagewaveform of NSPWM algorithm based vector controlled induction motor drive

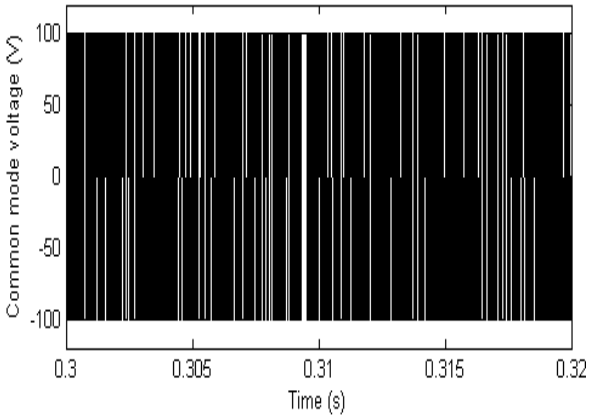

Fig. 11 Common mode voltage variations in NSPWM algorithm based vector controlled induction motor

From Fig. 5 and Fig. 9, it can be observed that the NSPWM algorithm gives more THD when compared with the SVPWm algorithm. Moreover, from Fig. 7 and Fig. 11, it can be observed that the NSPWM algorithm gives less common mode voltage variations when compared with the SVPWM algorithm.

Thus, from the simulation results, it can be observed that the proposed NSPWM algorithm reduces common mode voltage when compared with the SVPWM algorithm with slight increase in harmonic distortion. Moreover, from the line voltage waveforms, it can be observed that there are opposite pulses in line voltage of NSPWM algorithm. Also, as the proposed algorithm clams any one of the phases for a total period of 120 degrees over a fundamental cycle, it reduces the switching losses of the inverter and also the switching frequency of the inverter is 2/3 times to that of the SVPWM algorithm.

6 CONCLUSIONS

In this paper, a NSPWM algorithm is presented for vector controlled induction motor drives. to validate the proposed algorithm, simulation studies have been carried out and results are presented. From the results, it can be observed that the proposed NSPWM algorithm gives less common mode voltage variations when compared with the SVPWM algorithm with slight increase in harmonic distortion. Also, as the proposed NSPWM algorithm is a bus-clamping sequence, it reduces the switching losses by 33.33%. Hence, the switching frequency of the proposed NSPWM algorihm is also less when compared with the SVPWM algorithm.

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