Low Power Consumption of Pulse Triggered Flip Flop Using MTCMOS

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Abstract—The objective is to design and simulate the low power pulse triggered flip-flop and to reduce the Leakage power consumption of the flip flop by applying pulse triggering method used for the clocks. The proposed method uses signal feed through technique to solve the problem in the discharging path of the similar pulse triggered flip flop implementations. The discharge time is reduced by the proposed method and the speed of the pulse triggered flip flop with signal feed through technique is greatly increased. The proposed design out performs all the other similar pulse triggered flip flop implementation both in speed and power consumption.To reduce the leakage power MTCMOS is used. The design is implemented in 90nm GPDK using Cadence Virtuoso Schematic Composer and the Spectre as the simulator.

Index Terms— High Speed, Low Power, Pulse Triggered, Signal Feed Through, MTCMOS, Clocking, Layout

1 INTRODUCTION

Flip flops are the most important components in the memory, processor design and they are power hungry. They consume lot of power dissipation is more when the clock speed is more. Pulse-triggered flipflop consist of its single-latch structure, is more democratic than the conventional transmission gate and master–slave based flipflops in high-speed applications.

Analysis of conventional flip flops in terms of power , area and Speed. Conventional explicit type P-FF designs are compared.

Ep-DCO with contribution pulse generator is among all semi dynamic flip-flops believed for use in smallest of speed-critical paths. The design is stand in drawback i.e the internal node is discharged on every rising edge of the clock. It give rise to large switching power dissipation. To defeat the trouble, Conditional Discharge have been proposed[1].

CDFF not only reduces the internal switching activities, but also generates without glitches at the output, while maintaining the negative setup time and small D-to- Q delay characteristics.

While ep-DCO is suitable for speed critical paths, CDFF is suitable for both speed critical paths and speed-insensitive paths for energy-efficiency. For low-voltage environment, these techniques could also be used. However, with threshold voltage scaling, the leakage power control is essential. CDFF could be implemented with MTCMOS under 1.0V, dual Vt techniques to control leakage power consumption[2].

SCDFF requires no precharging at each clock cycle and the switching activity of SCDFF is dependent on the data switching activity, which tends to be much less than the clock switching active the use of SCDFF is a good choice when low power, minimum area and high-speed operation are required[3].

Single Edge triggered Flipflop known as MHLFF cuts down the power dissipation. The power consumption in the clock tree is reduced by halving the clock frequency of the MHLFF for the same throughput. MHLFF reduced the power consumption of HLFF by avoiding unnecessary node transitions [4].

2 MODIFIED P-FF DESIGN USING SIGNAL FEED THROUGH TECHNIQUE

2.1 Existing P-FF Design

The principles of FF operations of the existing design are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor NM3, which keeps the input stage of the FF from any driving effort. At the same time, the input data and the output feedback Q_fdbk accept complementary signal levels and the pull-down path of node X is off.

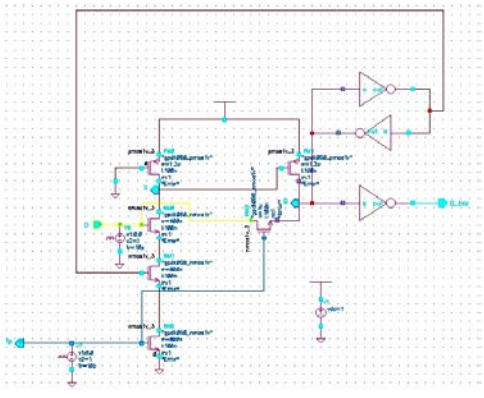

Fig. 1. Existing P-FF Design [5]

Hence, no signal switching occurs in any internal nodes. On the other hand, if a “0” to “1” data transition occurs, node X is

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discharged to turn on transistor PM1, which then pulls node Q high.

Since NM3 is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the is charging duty of the input source is lifted once the state of the keeper logic is inverted.

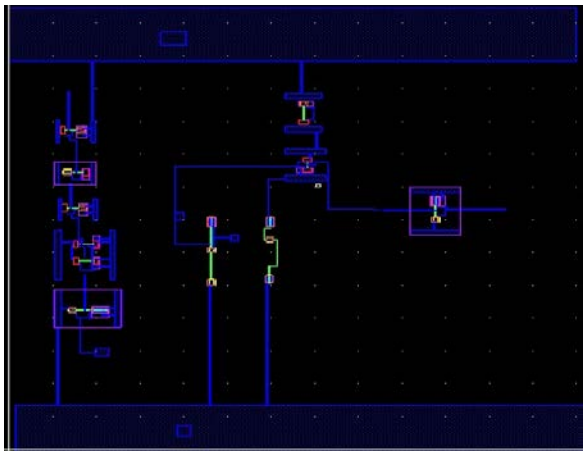

Fig. 2 Existing P-FF Layout Design

Here, Fig.2 shows the layout design of existing P-FF design. Area of existing system is 4401.2 Inches. The top and bottom yellow colour rectangular box shows that the VDD and GND respectively. On the left side pulse generator is designed. Yellow line indicates metal 1and wire is connected to the transistor. No DRC (design rulecheck) error found and LVS i.e (layout versus schematic) also verified.

2.2 Modified 1 P-FF Design

In proposed design as shown in 3, number of transistor is reduced compared to existing P-FF design. Q_feedback is removed so that the area and power are consumed. The width of the transistor is reduced. PM0 and PM1 are connected parallel, NM0 and NM1 are in series, through the pass transistor NM2 signal is feed through it.

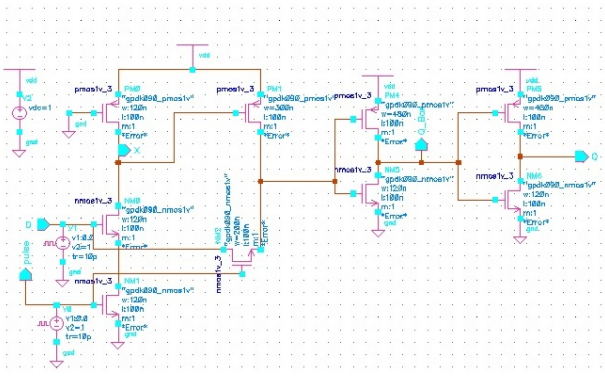

Fig. 3 Modified 1 P-FF Design

Continuously two 4 transistors in the form of invertors are designed. PM4 and NM5 output leads to Q_Bar, PM5 and NM6 output leads to Q.

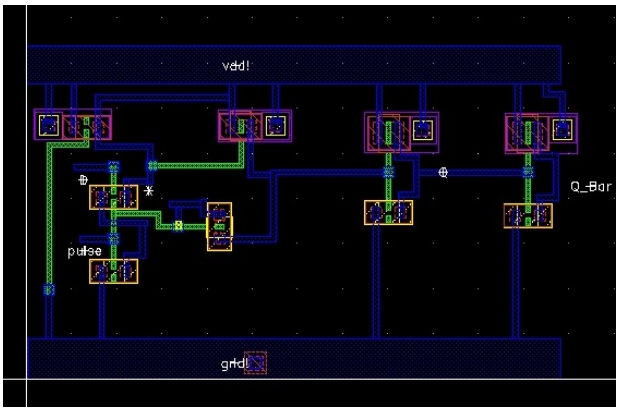

Fig. 4 Modified 1 P-FF Layout Design

Here, Fig.4 shows the layout design of proposed P-FF design. Area of existing system is 86.14 Inches. The top and bottom yellow colour rectangular box shows that the VDD and GND respectively. On the left side pulse generator is designed. Yellow line indicates metal 1and wire is connected to the transistor and the blue wire indicates the poly i.e gate connected terminal. No DRC (design rulecheck) error found and LVS i.e (layout versus schematic) also verified.

2.3 Modified 2 P-FF Design

In proposed design using MTCMOS as shown in 5, number of transistor is reduced compared to existing P-FF design and proposed1 P-FF Design. Q_feedback is removed so that the area and power are consumed. The width of the transistor is reduced. PM0 and PM1 are connected parallel, NM0 and NM1 are in series, through the pass transistor NM2 signal is feed through it. Continuously two 4 transistors in the form of invertors are designed. PM4 and NM5 output leads to Q_Bar, PM5 and NM6 output leads to Q. Here NMOS transistors are designed with MTCMOS.

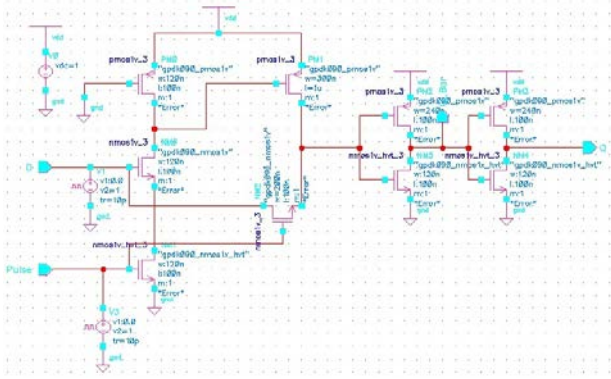

Fig. 5 Modified 2 P-FF Design

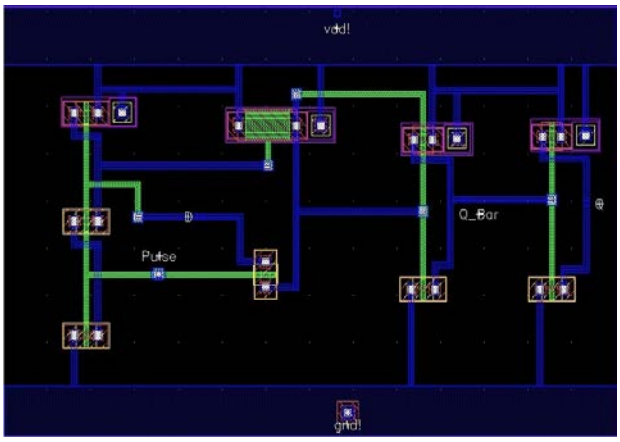

Fig. 6 Modified 2 P-FF Design

Here, Fig.6 shows the layout design of Proposed P-FF design using MTCMOS. Area of existing system is 70.2 Inches. The top and bottom yellow colour rectangular box shows that the VDD and GND respectively. On the left side pulse generator is designed. Yellow line indicates metal 1and wire is connected to the transistor. No DRC (design rulecheck) error found and LVS i.e (layout versus schematic) also verified.

2.4Signal feed through technique

Low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data "1" and "0," the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving [5].

2.5 Pass Transistor

It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels, between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Pass transistor logic often uses fewer transistors, runs faster, and requires less power than the same function implemented with the same transistors in fully complementary CMOS logic.

3.SIMULATION RESULTS

Simulations were carried out using CMOS GPDK 90nm in Cadence Analog Design Environment with Spectre as the simulator. The pulse width for clock is 120ps and the period is 240ps while for input clock pulse width is 400ps and the period is 800ps.

3.1 Output Waveform

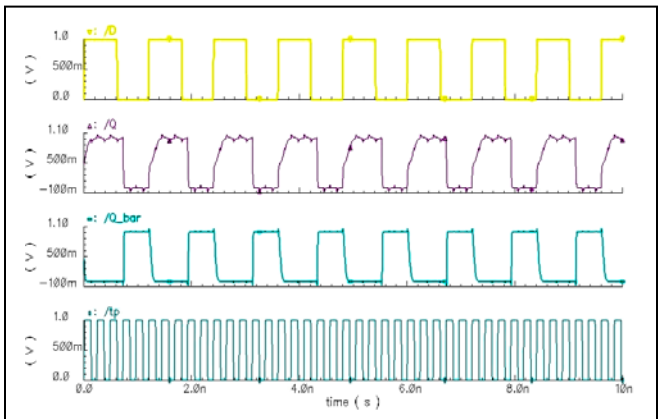

Fig.7 Existing P-FF Design output waveform

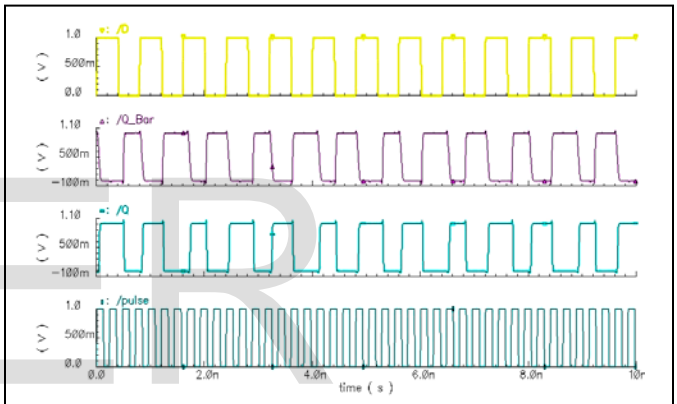

Fig.8 Modified1 P-FF Design output waveform

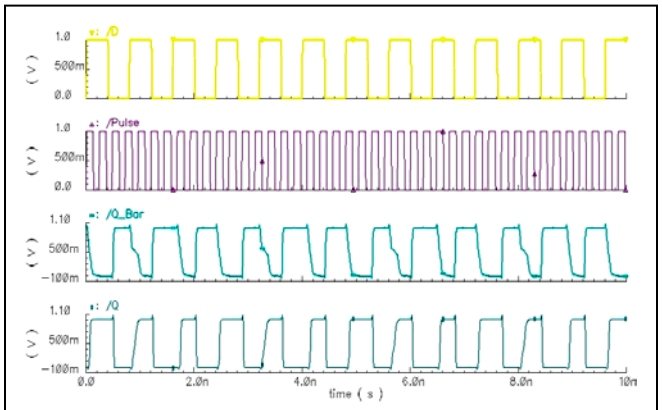

Fig.9 Modified 2 P-FF Design using MTCMOS output waveform

The output waveforms are shown below: Fig.7 shows exist-

ing P-FF design Output waveform; Fig. 8 shows modified 1 output waveform and Fig.9 shows modified 2 output waveform.

4. Measuring Parameters

4.1 Leakage Power Calculation

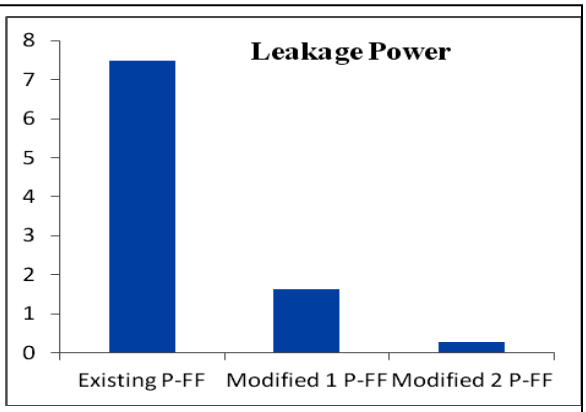

Fig.10 Comparison of modified 1&2 P-FF design Leakage

Fig.10 shows the leakage power comparison of modified 1&2 P-FF Design with the existing P-FF design. The average leakage power of modified 2 P-FF design using signal feed through technique shows better leakage power than existing P-FF Design. It is expressed in microwatts.

4.2 Static Power Calculation

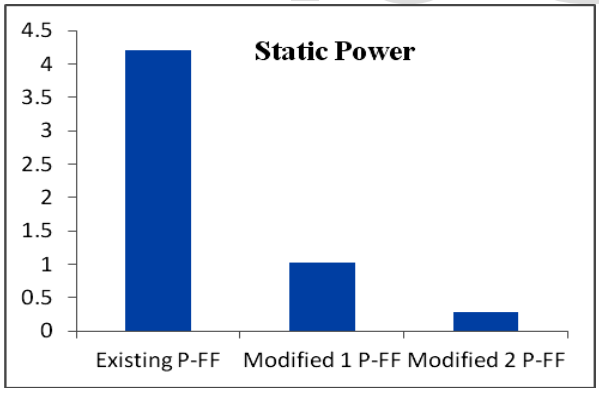

Fig.11 Comparison of modified 1&2 P-FF design Static Power with existing P-FF Design

Fig. 11 shows the static power comparison of modified 1&2 P-FF Design with the existing P-FF design. The average static power of modified 2 P-FF design using signal feed through technique shows better static power than existing P-FF Design. It is expressed in microwatts.

4.3 Dynamic Power Calculation

The average dynamic power of modified 2 P-FF design using signal feed through technique shows better dynamic power than existing P-FF Design. It is expressed in microwatts.

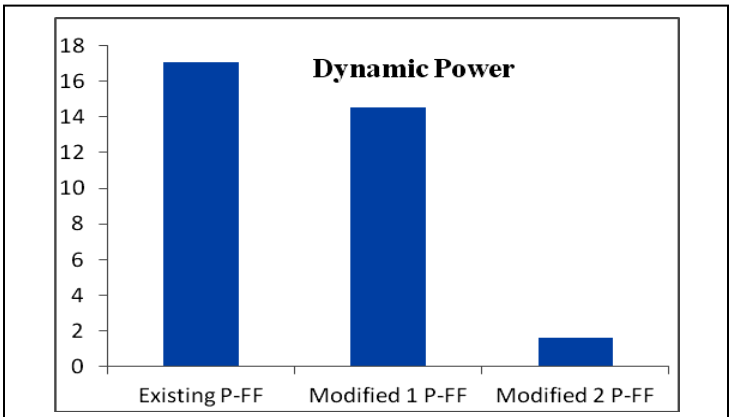

Fig.10 Comparison of modified 1&2 P-FF design Dynamic Power with existing P-FF Design

Fig.12 shows the Dynamic power comparison of modified 1&2 P-FF Design with the existing P-FF design.

4.4 D-to-Q Delay

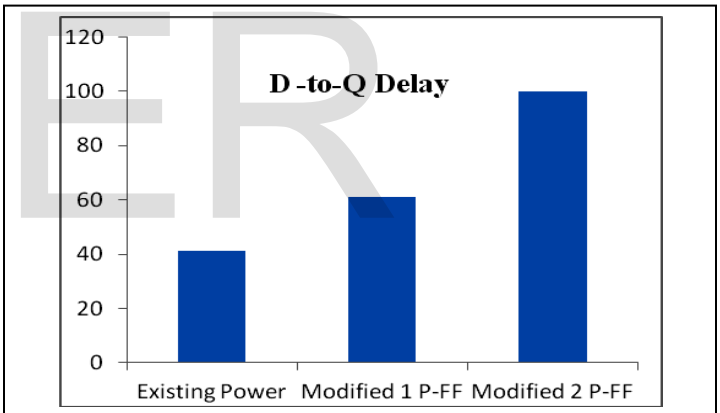

Fig.13 Comparison of modified 1&2 P-FF design D-to-Q delay with existing P-FF Design

Fig.13 shows the Delay comparison of modified 1&2 P-FF Design with the existing P-FF design. The Delay of modified 1&2 P-FF design using signal feed through technique shows lower delay than existing P-FF Design. Because of lowering the power delay increases. It is expressed in Picoseconds.

4.5 Voltage Scaling

Scaling the power supply voltage enables a quadratic reduction in dynamic power dissipation with a reduction in Performance which can be partially compensated by scaling the threshold voltage.

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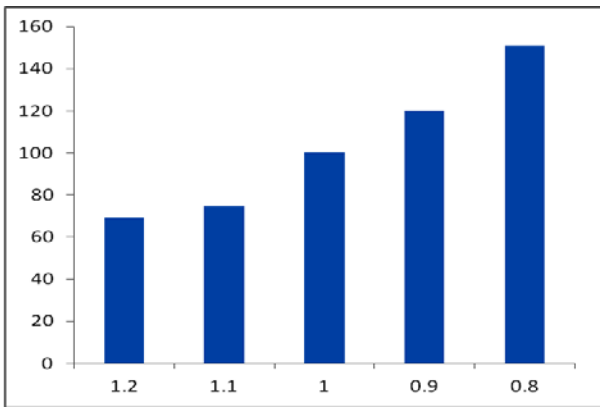

Fig.14 Supply Voltage (V) Vs Delay (Ps)

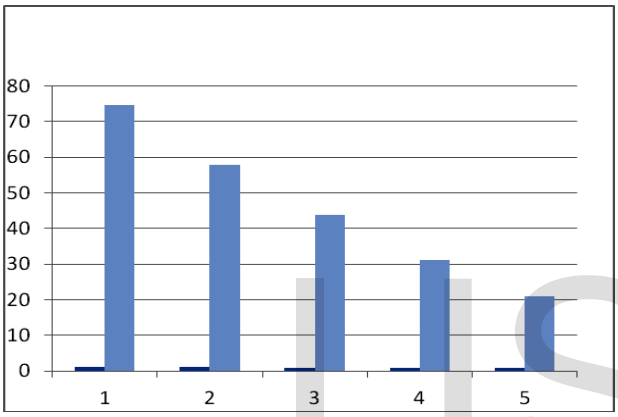

Fig.15 Supply Voltage (V) Vs Power (mW)

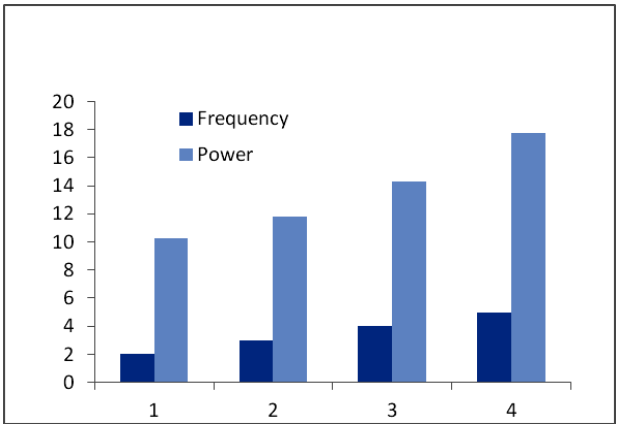

Fig.16 Frequency (GHZ) Vs Power (mW)

Voltage scaling is the measure of delay and power with supply voltage. Fig.14 shows supply voltage vs delay while voltage decreases delay increases. Fig.15 shows voltage vs pwer as voltage increases power also increases.

4.6 Frequency Scaling

The power savings and the stability of the resonant clocking are directly proportional to its frequency. Thus, lower frequency implementations of rotary clocking are often inefficient and less stable.

Fig.16 shows the frequency Vs Power when frequency increases power decreases. Power is inversely proportional to frequency.

4.7 Effect Of Temperature On Delay

The performance of the analog circuit depends upon the delay in the circuit and the path delay depends upon the delay . Analog circuit designing typically assumes that with increasing voltage and increasing temperature delay increases.

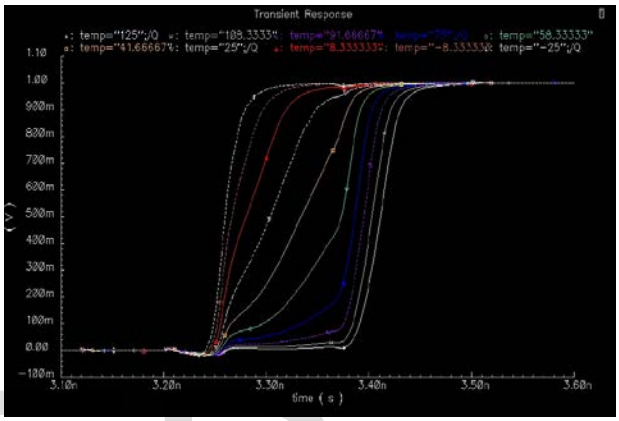

Fig.17 FrequencyRise time Delay in Effect Of Temperature (GHZ) Vs Power (mW)

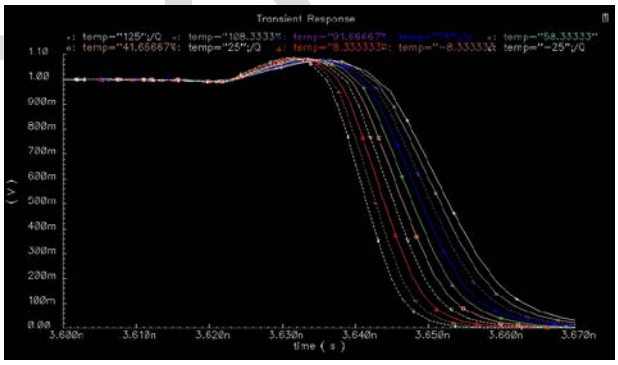

Fig.18 Frequency Fall time Delay in Effect Of Temperature (GHZ) Vs Power (mW)

Fig. 17 shows the rise time of delay in the effect of temperature while the temperature is rising. Fig.18 shows the fall time of delay in the effect of temperature while the temperature decreases.

While the temperature increases delay also increases. The variation between the temperature and delay shown in fig. 4.19

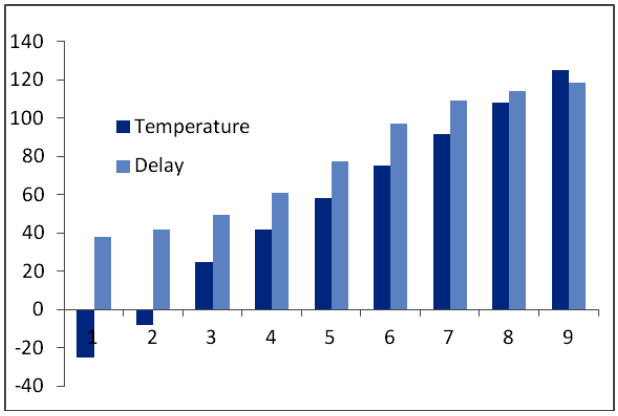

Fig.19 Temperature (^{0}C) Vs Delay(Ps)

5 Conclusion

Modified 1 & Modified 2 Circuit shown minimum dynamic and static power. In modified 2, MTCMOS is attached so the leakage power is decreased but delay is increased. n-MOS would have extra driving to shorten the transition time and perform low power and high speed. The design was employed by simple signal feed through technique. Leakage, static and dynamic power is reduced in the proposed design compared to conventional flip-flops and the delay is also reduced and hence the proposed design outperforms the existing flip flops.

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