# Design and VLSI Implementation of Second Order Sigma-Delta Modulation ADC for I-UWB Receiver

K.Lokesh Krishna, T.Ramashri, D.Srihari

**Abstract**— Analog to Digital converters plays an essential role in modern mixed signal circuit design. Mixed-signal System-on-chip devices such as Analog-to-Digital Converters (ADC) have become increasingly prevalent in the semiconductor industry. Nyquist Samplers require a complicated analog low pass filter to limit the maximum frequency input to the A/D and Sample and Hold circuit. Sigma-Delta (ΣΔ) modulation based Analog to Digital (A/D) conversion technology is a cost effective alternative for low power, high resolution (greater than 12 bits) converters, which can be ultimately integrated on Digital Signal Processor ICs. In this paper Over Sampling concept is used to address the problem of power dissipation, noise in ADCs and investigating the possibilities of utilizing alternative methods to reduce the noise and power dissipation in ADC architectures. This is achieved by design techniques namely Over Sampling, Second order Sigma-Delta architectures and Switched Capacitor based Sample & Hold circuits. A Second order Sigma-Delta Modulator is implemented using CMOS 0.13 µm technology using a ±1.8 V power supply. Over sampling ratio are 128 with clock frequency of 45 GHz which gives bandwidth of 20 GHz. The total power dissipation of the modulator is 60 µW. The area occupied by the modulator is 30 µm x 35 µm.

**Index Terms**— Analog to Digital Converter (ADC), Sigma-Delta Modulator, Over Sampling, Sample and Hold circuit, Switched capacitor, Ultra Wide Band (UWB), Poweer dissipation and Two stage Op Amp.

## 1 INTRODUCTION

High Speed Analog-to-Digital Converter (ADC) blocks are essential for a very wide range of applications in wireless telecommunications, medical imaging, instrumentation, audio and video processing systems. Sampling rates in excess of 500 MHz and bit resolution of more than 10 bits are increasingly required to accommodate the very high bandwidth requirements in wireless applications [1, 2, 3]. Sigma-Delta (ΣΔ) Analog to digital converters (ADCs) are being increasingly used in wireless applications.

On February 14, 2002, the Federal Communications Commission allocated spectrum for a new radio communication technique called Ultra-Wide-Band (UWB) [4]. With the frequency band between 3.1 GHz to 10.6 GHz being made available for UWB based applications, many researchers are involved in developing new electronic devices and applications that can work in this band. Ultra-Wide-Band (UWB) communication is an emerging and a promising new generation wireless technology with huge expectations in short range wireless market segment, which is very active today. The great potential of UWB lies in the fact that it can co-exist with the users of already licensed spectrum and that it opens a wide range of applications.

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Such applications include high-speed wireless personal area networks (WPANs) and wireless USB [5]. UWB signals have bandwidths over 500 MHz and can be transmitted without carrier such as impulse radio or non-sinusoidal pulses or can be modulated as wide-bandwidth signals with carriers such as multi-band orthogonal frequency division multiplexing (MB-OFDM). A UWB signal is typically composed of a train of sub-nanosecond pulses, resulting in a bandwidth over 1 GHz. Since the total power is spread over such a wide range of frequencies, its power spectral density is extremely low. This minimizes the interference caused to existing services that already use the same spectrum. On account of the large bandwidth used, UWB links are capable of transmitting data over hundreds of megabits per second. Other benefits include a low probability of interference and detection, precise locationing capability and the possibility of transceiver implementation using simple, "all digital" architectures. Due to the very large bandwidths, UWB systems rely on very high sampling rates to operate. UWB systems must be able to transmit and receive an extremely short duration burst of radio frequency (RF) energy – typically from a few tens of picoseconds to a few nanoseconds in duration. These bursts may be formed by one or a few cycles of an RF carrier wave. Therefore the waveform is extremely broadband, and it is often difficult to determine the real RF center frequency, and thus, the term "carrier-free". There are basically two types of UWB communication: (i) Impulse-based UWB (I-UWB) that is based on very short pulses and (ii) Multicarrier UWB (MC-UWB) that is based on multiple simultaneous carrier signals [6].In this work, the design and analysis performances of Second order Sigma Delta Modulation (ΣΔ) ADC architecture that can be used in I-UWB receiver is presented.

This paper is organized as follows. Section II discusses the

theoretical background of I-UWB receiver. Section III discusses the design specifications of Sigma Delta Modulator ADC for I-UWB receiver and design of high speed ADCs. The performance results and discussions are presented in Section IV. Finally, conclusions are drawn in Section V.

## 2.0 IMPULSE-BASED UWB

Unlike classic communication systems, impulse-based UWB (I-UWB) does not use a carrier to convey information. The information is transmitted in a series of baseband pulses. Since the pulse durations are in the nanosecond range, the signal bandwidth is in the range of gigahertz. For radar applications, short pulses can provide very fine time resolution and precision for the measurement of distance and/or positioning. Short pulses are relatively immune to multipath cancellation effects due to mobile and in-building environments. Multipath cancellation occurs when the direct path signal and an out of phase reflected wave simultaneously arrive at the receiver, thus causing a reduced amplitude response in the receiver. With very short pulses at short range, the reflected signal will arrive at the receiver after the direct signal is gone, and there is no cancellation. Therefore, I-UWB systems are well suited for high-speed, mobile wireless applications. Since the bandwidth is large, the UWB energy density (power per hertz) can be quite low. Low energy density translates into a low probability of detection which is of particular interest for military applications such as stealth communications and radar. At the same time, a low probability of detection also represents minimal interference to other systems and minimal RF health hazards. Figure 1, shows the spectrum of impulse UWB signal [7].

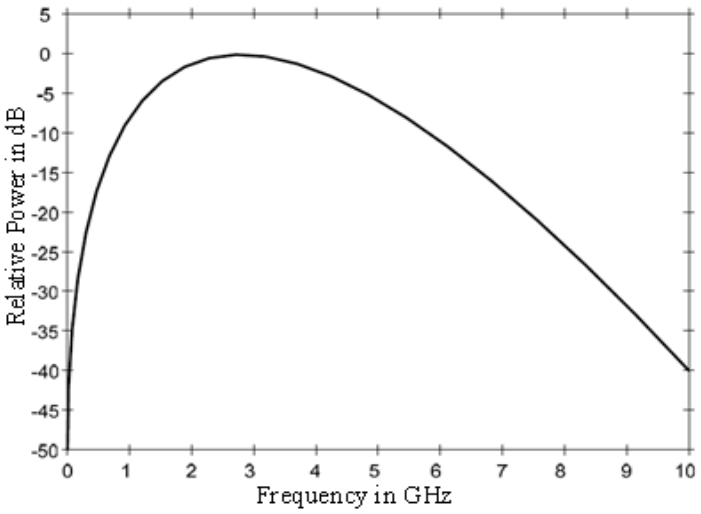



**Figure 1 Spectrum of Impulse UWB signal**

Figure 2, shows the top level block diagram of I-UWB receiver [19]. I-UWB receiver consists of an ultra wideband Low Noise Amplifier (LNA), a frequency domain sampler, an energy harvester block, and a decision block. LNA must exhibit a low return loss, a low noise figure and a high gain across the entire frequency band of interest. These characteristics are mainly supported by the input matching skills of the circuit.

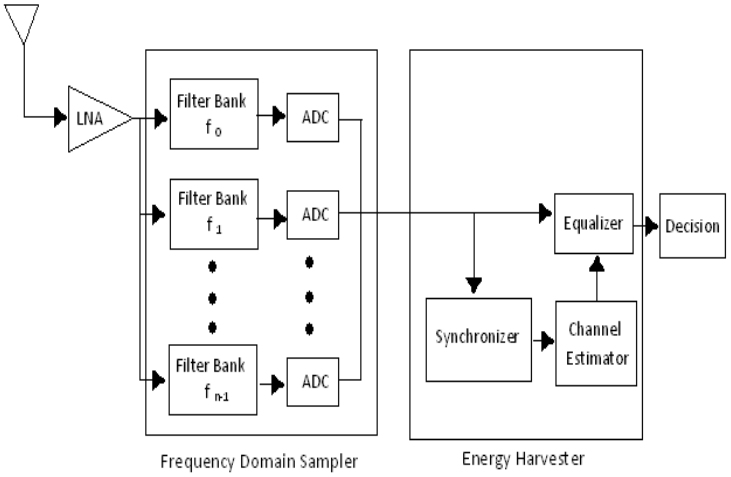



**Figure 2 Top level block diagram of I-UWB receiver [8]**

The incoming signal is amplified using LNA and is filtered using multiple filter banks with centre frequency $f_0$, $f_1$,…… $f_{n-1}$. The filtered data is sampled using ADC and is fed to the energy harvester. The ADC samples the filtered signal and is digitized for further processing. In order to reduce complexity time-interleaved ADC is employed. A time-interleaved ADC consists of parallel ADCs driven by multiple clocks with small difference in time. This reduces the required speed of the ADC by the number of parallel ADCs. For example, two ADCs in parallel reduce the required ADC speed by half. The energy harvester block collects the energy dispersed on multipath and its function is identical to the RAKE function used for narrowband communications systems [9]. The communication channel is estimated after achieving synchronization, and the equalizer performs inter-symbol interference cancellation to recover an ideally interference-free representation of the desired symbol. A major challenge in digital I-UWB receiver design is due to the I-UWB channel, the narrow pulse shape, and narrowband interference. First, the I-UWB channel inherently suffers a relatively large delay spread as compared to the pulse width. The delay spread is normally at least tens of nanoseconds [10] compared to typical pulse widths of hundreds of picoseconds. During the large delay spread it is possible that hundreds of multipath reflections may be seen by the receiver. Thus, for a standard RAKE receiver, many correlates are necessary to exploit available multipath diversity. Such a large number of RAKE fingers are not practical for an analog correlate because it adds excessive complexity in hardware and control operations. Figure 3, shows the top level architecture of digital I-UWB receiver. The incoming signal is filtered and is sampled to convert analog data to digital data and is passed through DSP for further processing. $H_i(j\Omega)$ is the frequency response of the Band Pass Filter (BPF) assigned to each sub-band and $f_{ck}$ is the sampling clock frequency.

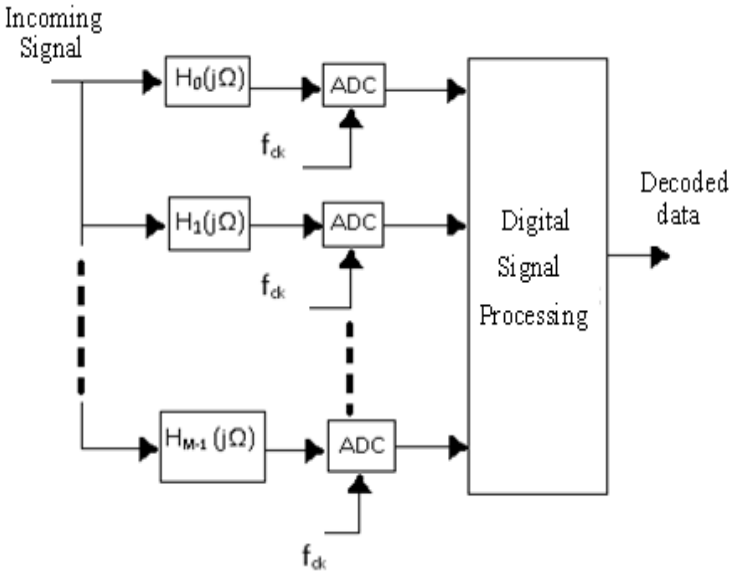



**Figure 3 Top level module of digital I-UWB receiver [11]**

The ADC architecture designed in this paper can be used for high speed I-UWB receiver.

## 3.0 Sigma-Delta Modulator (ΣΔ) ADC:

Sigma Delta (ΣΔ) modulators are the most suitable Analog-to-Digital Converter (ADC) topologies for digitizing with high-resolution analog signals characterized by a bandwidth much smaller than the sampling frequency *fs*. With these architectures, a resolution up to 19–21 bits can be reached using standard Integrated Circuit (IC) technologies. Sigma delta modulators employ coarse quantization enclosed in one or more feedback loops. By sampling at a frequency that is much greater than the signal bandwidth, it is possible for the feedback loops to shape the quantization noise so that most of the noise power is shifted out of the signal band. The out of band noise can then be attenuated with a digital filter. The degree to which the quantization noise can be attenuated depends on the order of the noise shaping and the over sampling ratio. In addition to their tolerance for circuit nonlinearities, over sampled A/D converters simplify system integration by reducing the burden on the supporting analog circuitry. Because they sample the analog input signal at well above the Nyquist rate, precision sample-and-hold circuitry is unnecessary. Also, the burden of analog anti aliasing filter is considerably reduced. To fulfill the requirements we chose the second-order modulator. The second-order will give enough margins for circuit non-idealities and process variations. Cyril et. al [12] have discussed techniques to design sigma delta modulator. The techniques discussed in [12] have been used in this work with suitable modifications to operate at higher frequency.

### *3.1* Modulator Architecture:

The (ΣΔ) modulator architecture is implemented by combining two summing integrators with comparator and 1-bit D/A converter, as shown in Figure 4. The most important building block in this architecture is a summing integrator, for which the output is the delayed integration of a weighted sum of input. The remaining building blocks in the analog portion of the modulator are comparator and 1-bit D/A converter. The comparator circuit acts as a 1-bit A/D converter that maps its input into one of two digital output codes. The two digital output codes are then mapped back into analog levels by the D/A converter. If the two output codes of the comparator are defined as ±1/2 LSB, then the D/A converter, neglecting D/A errors, can be represented simply by gain block. X represents input signal, Y represents sampled output, y represents feedback input and $g_n$ represents gain.

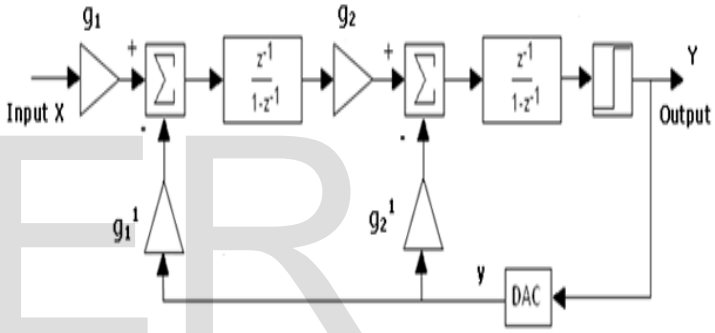



**Figure 4 Second Order Sigma-Delta (ΣΔ) Modulator Architecture [13]**

### 3.2 Stability Analysis:

The advantage of first order noise shaping is an improvement of the SNR by 9 dB for every doubling of the over sampling ratio as opposed to a 3 dB increase without noise shaping. It can be also be proved that implementing a second order delta-sigma ADC can provide for much better noise shaping and a higher order resolution. Thus, the signal to noise ratio (SNR) is higher for a second order ADC [14]. The transfer function for the second order system can be given by Eq. (1)

$$Y(Z) = (Z^{-1})^2\, X(Z) + (1 - Z^{-1})^2\, E(Z) \quad (1)$$

where X denotes input signal and Y denotes output signal

As it can be seen from the transfer function, the input signal is to be delayed by two cycles and two integrators can be used in cascade to implement the square term in the transfer function expression. Therefore, implementing a second order system does not cause any serious changes in the design procedure except for using two integrators. Hence, a first order system will be de-

signed and implemented as a second order system to yield the advantages of high resolution and better signal-to-noise ratio. Assuming again a linear model for the comparator, the modulator output in the z -domain yields expression Eq. (2).

$$Y(Z) = \frac{g_1\, g_2\, g_q\, Z^{-2}X(Z) + (1 - Z^{-1})^2\, E(Z)}{1 + \left(g_2^{l}\, g_q - 2\right) Z^{-1} + \left(1 + g_1^{l}\, g_2\, g_q - g_2^{l}\, g_q\right) Z^{-2}} \qquad (2)$$

so that the following conditions must be fulfilled for a pure 2nd order shaping which is given by Eq (3).

$$y(z) = \frac{g_1}{g_1^{l}} Z^{-2}X(Z) + (1 - Z^{-1})^2 E(Z) \qquad (3)$$

if

$$g_1^{l}\, g_2\, g_q = 1, g_2^{l} = 2g_1^{l} g_2 \qquad (4)$$

The proper selection of these free coefficients involves important design concerns that are not covered by the linear model. The most important are keeping the state variables (integrator outputs) bounded to ensure the modulator stability. The 2nd order sigma-delta modulator is stable for inputs in the range

$$\left[-\frac{0.9\Delta}{2}, +\frac{0.9\Delta}{2}\right]$$

regardless the quantizer gains are $g_2^{l} > 1.25\, g_1^{l}\, g_2$ , $g_2^{l} = 2g_1^{l}\, g_2$

So both integrator gains are selected as 0.5 to meet the stability. The SNR of the second order noise shaping modulator is given by [15]

$$SNR = 6.02N + 1.76 - 12.9 + 50\ log\ OSR$$

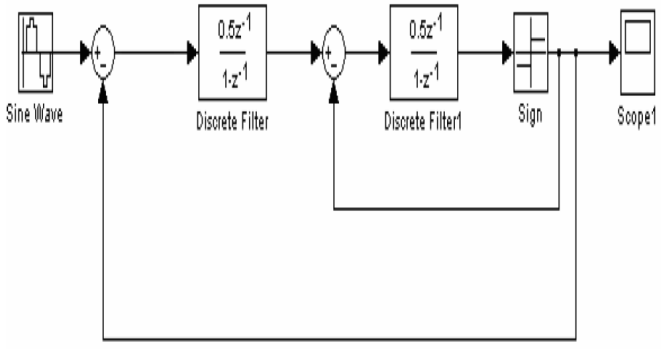
$$PQ = \frac{\Delta^2 \times \Pi^4}{60 \times OSR^5}$$

$$DR\ (dB) = 10 \log \frac{3.5 \times OSR^5}{2 \times \Pi^4}$$

so that DR increases by 2.5 bit / octave with OSR.
The poles of the integrator transfer function become the zeroes for the noise transfer function (NTF). The NTF zeroes are mapped to DC and hence noise shaping can be obtained.

### 3.3 Behavioural Simulation:

The functional diagram of the second order (ΣΔ) modulator is simulated using Simulink in MATLAB is shown in Figure 5. The single bit DAC is replaced by a simple wire. The input is a sinusoidal signal with 1 V amplitude and frequency 1GHz. This signal is fed through two integrators in cascade and is connected to the comparator at the output. Intermediate gain stages are used to provide stability to the system to ensure that all the poles of this system are well within the unit circle in the z domain. The modulated output as seen through the scope is shown in Figure 5. A discrete Fourier Transform (DFT) of the sampled output signal (4*2048 samples) is performed to calculate the SNR of the system.



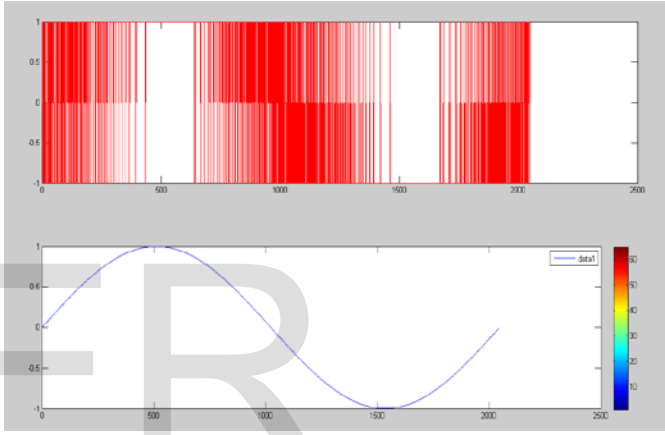



**Figure 5 MATLAB Simulink simulation of the modulator**

The logarithm of the amplitude of the signal is plotted versus the signal frequency and the SNR. It can be seen that second order noise shaping is taking place wherein most of the noise is pushed to the higher frequency bands. The original signal can be retrieved using a digital low pass filter.

## 4.0 CIRCUIT DESIGN:

After behavioural level simulations were performed we had enough parameters for transistor level implementation. All required analog blocks (operational amplifiers, switches, capacitors and quantizer) were designed, simulated and then layout is carried out.

### 4.1 Two stage Operational Amplifier Design:

The operational amplifier used in integrators is the most critical element of the modulator. Comparator also can be implemented from the operational amplifier. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required. The need for high speed, coupled with a relatively modest gain

requirement of 60 dB to suppress harmonic distortion, encouraged the use of the general two stage operational amplifier [16]. Figure 6, shows general two stage operational amplifier used in this design. Figure 7, shows two stage operational amplifier simulation results. The second major component of the modulator is the comparator. The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effects of those impairments is attenuated by the second order noise shaping. The operational amplifier has been used to implement the comparator.

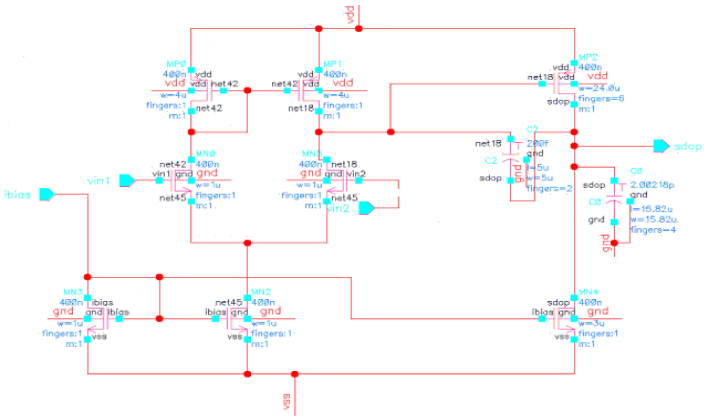


**Figure 6 Two Stage Operational Amplifier schematic**

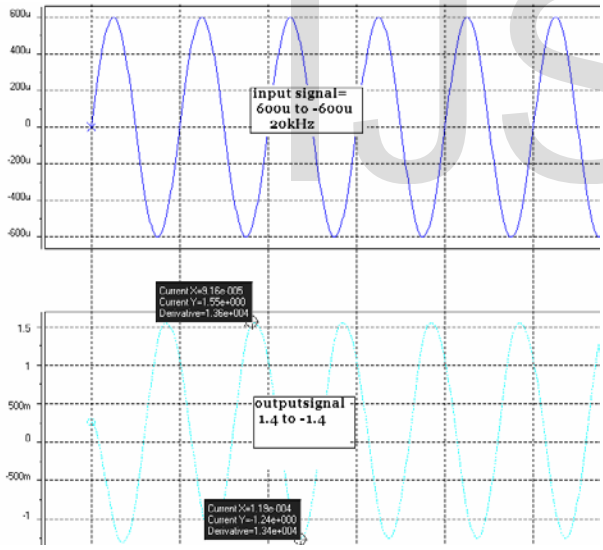



**Figure 7 Two Stage Operational Amplifier simulation results**

| Specification | Achieved Value |
|---|---|
| Gain | 60 dB |
| Voltage Swing | 1.4 V to -1.4 V |
| 3 dB Frequency | 50 GHz |
| Unity Gain Frequency | 60 GHz |
| Phase Margin | 45° |

**Table1: Operational Amplifier specifications**

The two stage operational amplifier is designed to operate with UGB of 60 GHz and phase margin of 45⁰. In order to improve the UGB to 60 GHz, the bias transistors in the first stage are designed with larger widths in the order of 300 microns, further the load capacitance in the first stage is set to 0.001 pf for better stability. The achieved values of the operational amplifier specifications are listed in Table 1.

## 4.2 Sample & Hold Circuit:

In this current work sampled hold circuits are implemented by the switched capacitors. Switched capacitors are implemented by the transmission gates [17]. Figure 8 shows the schematic diagram of sample and hold circuit. Figure 9 shows the simulation results of sample and hold circuit. The input to the sample and hold circuit is sine wave having bandwidth of 20 KHz and the sampled signal frequency is 45 GHz to meet the OSR of 128 .The delay of the sampling signal is 0.4 nsec. The output of the sample and hold circuit is sampling signal having frequency of 45GHz.

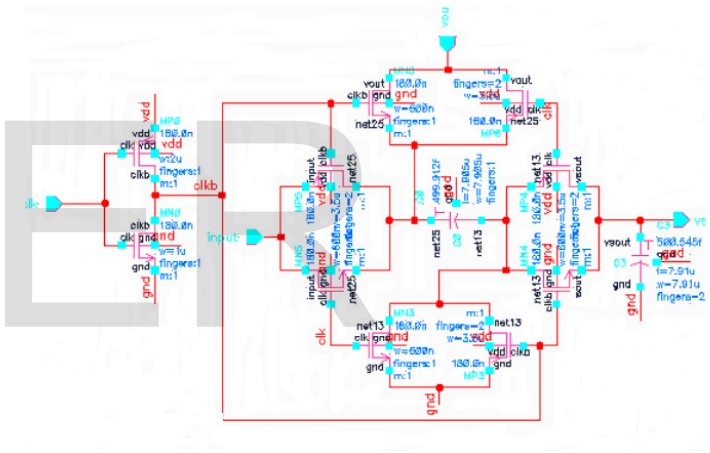


**Figure 8 Sample & Hold Circuit schematic**

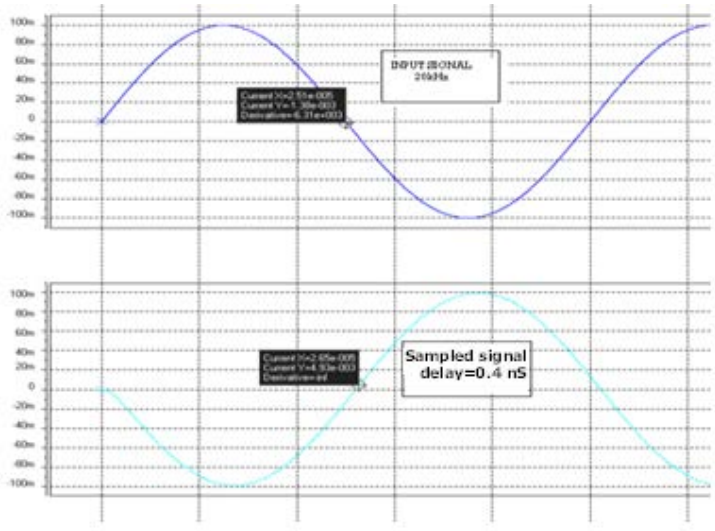



**Figure 9 Sample & Hold Circuit simulation results**

### 4.3 Second Order Sigma-Delta (ΣΔ) Modulator Design:

The sigma-delta modulator depicted in Figure 10 was designed for fabrication in 0.13 µm CMOS technology. The operational amplifier used in integrators is the most critical element of the modulator. Since the comparator can be designed to be quite fast, the settling speed of the integrator ultimately limits the achievable sampling rate of the modulator, even if complete settling is not required. The need for high speed, coupled with a relatively modest gain requirement of 60 dB to suppress harmonic distortion, encouraged the use of the general two stage operational amplifier.

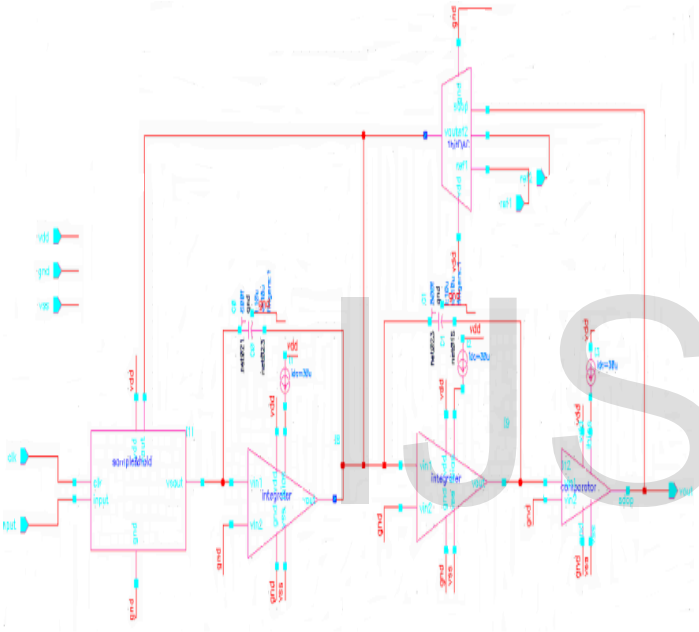


**Figure 10 Top level schematic of the ADC**

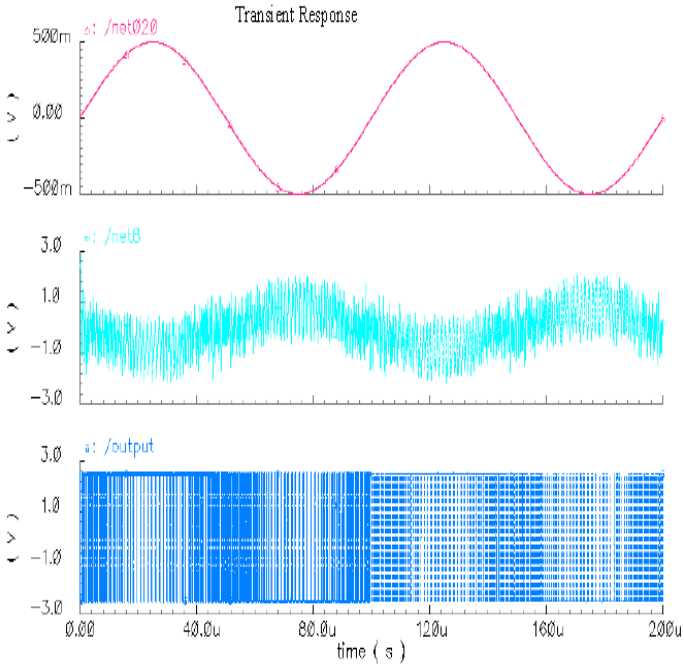



**Figure 11 Output waveforms of the ADC**

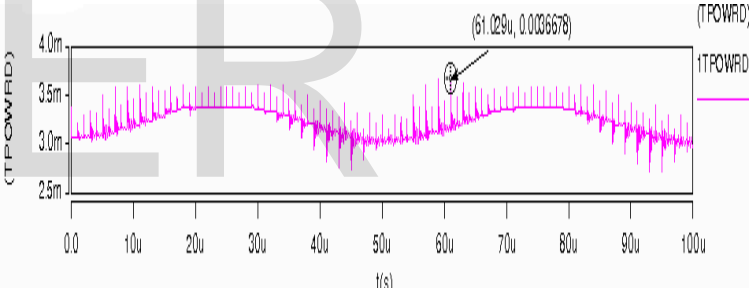



**Figure 12: Power Dissipation of the ADC**

## 5.0 RESULTS & DISCUSSION:

Output spectrum obtained from transistor level simulations data for 1GHz sinusoidal input signal is shown in Figure 11 . Input signal frequency is 1 GHz, which is enough to have a reasonable simulation time, while giving enough samples (16 k samples) to perform a FFT. During layout implementation a special attention was paid to matching and noise considerations. Figure 11 shows the 1bit output waveform of the modulator and power dissipation of the modulator was found to be 60 µW from figure 12. Modulator occupies an area of 30 µm X 35 µm. All the results are summarized in Table 2.

**Table 2 Summary of the Results**

| Parameter | Value |
|---|---|
| Technology | CMOS 0.13 µm |
| Power Supply | ±1.8 V |
| Bandwidth | 20 GHz |
| OSR | 128 |
| Power Dissipation | 60 µW |
| Area | 30 µm x 35 µm |

## 6.0 CONCLUSION:

Sigma-Delta (ΣΔ) modulation based analog to digital (A/D) conversion technology is a cost effective alternative for low power, high resolution (greater than 12 bits) converters, which can be ultimately integrated on digital signal processor ICs. In this paper over sampling concept is used to address the problem of power dissipation, noise in ADCs and investigating the possibilities of utilizing alternative methods to reduce the noise and power dissipation in ADC architectures. This is achieved by design techniques namely over sampling, second order sigma-delta architectures and switched capacitor based sample & hold circuits. A second order sigma-delta modulator is implemented using CMOS 0.13 µm technology using a ±1.8 V power supply. Over sampling ratio are 128 with clock frequency of 45 GHz which gives bandwidth of 20 GHz. The power dissipation is limited to less than 127µW, power density is found to be 0.120W/ µm². The operating frequency can be increased by redesigning the Op amp to operate at higher bandwidth by changing the bias current and driving capability. The layout can be optimized by adopting layout optimization technique.

## 7.0 ACKNOWLEDGEMENT:

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