Closed Loop Control of Zero Voltage Switching DC-DC Converter to Generate Three Outputs

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Abstract: Hard switching specifies the stressful switching behaviour of the controlled switches. During the turn-off and turn-on processes, the power electronic device has to withstand high current and voltage simultaneously, resulting in high stress and switching losses. The switching loss is directly proportional to the switch frequency, thus reducing the maximum switch frequency of the power electronic converter. The concept was to incorporate resonant tanks in the converters to create oscillatory (usually sinusoidal) voltage and/or current waveforms, so the zero current switching (ZCS) or zero voltage switching (ZVS) conditions can be achieved for the power control switches. The Soft-switched power converters are generally utilizing the resonance condition. Resonance condition is generally occurred just during the turn-off and turn-on processes, so as to create ZCS and ZVS across each switch. The Regulated three and five multiple-output dc-dc converter under zero-voltage switching (ZVS) condition is proposed. The converter is consists of three outputs altogether. With the help of two asymmetric half bridge converters, the first and second outputs are controlled. Based on the phase shift between two asymmetric half bridge converters, the third output is controlled. At high switching frequency, these multiple-output dc–dc converters can give higher efficiency. The various stages of operation, soft switching condition and controlling schemes are also explained. A closed loop and open loop control techniques of the three multiple output converter is explained.

Keywords: DC-DC Converter, Zero voltage Switching(ZVS), Zero Current Switching(ZCS), Switching losses, Full bridge, Inverter, duty cycle, switching period, Pulse width Modulation (PWM)

1. INTRODUCTION

The DC-DC converters are widely used for battery power supply in different electronic devices like mobile phones, MP3 players and laptops. There is a scope for developing DC-DC converters to generate multiple dc output voltage from single dc power supply. These multiple output voltages are feed to the different dc load applications. This scheme of developing multiple dc voltage levels from a single dc supply source can reduce the overall device area. The dc voltage provided by rectifier or battery contains more ripples and it is not a constant value and it ia not suitable for many electronic devices. To overcome this problem, the dc-dc voltage regulators are used to control the ripples even when change in the input voltage or load current.

The switching mode type dc-dc converters power supply is widely used because it uses a switch in the form of transistor type and less loss components such as transformers, inductors and capacitors for controlling the output voltage. The switched mode power supply contains two different parts: control part and power part. The majority of the work is carried out by the control part for getting better control of output voltage. Generally the MOSFET is used as a control switch in Switched mode power supply for stabilizing the required output voltage. The MOSFET switches are not to be conducted continuously and they operate only under specific frequency interval only, hence these switches are useful for a long future and also provide less power loss the converter circuit. The basic structure of Switched mode power supply is used for stepping up or stepping down of input DC voltage. The SMPS circuit is basically consists of a filter at the output side for removing the ripples due to switching.

The main objective of the project is to regulate three multiple output voltages with dc-dc zero-voltage switching (ZVS) converter is proposed. The converter is consists of three multiple outputs voltages. With the help of two asymmetric half bridge converters, the first and second outputs are controlled. Based on the phase shift between two asymmetric half bridge converters, the third output is controlled. ZVS is realized for all the main switches**.** At high switching frequency, these multiple-output dc–dc converters can give higher efficiency. The various stages of operation, soft switching condition and controlling schemes are also proposed. A closed loop and open loop control techniques of the three multiple output converter is explained.

2. PROPOSED THREE MULTIPLE OUTPUT ZVS DC-DC CONVERTER

The fig.2.1 shows the main diagram of three multiple outputs ZVS DC-DC converter. Fig.2.2 shows the control signal of the multiple output converters. The Multiple outputs ZVS DC-DC converter consists of the two asymmetrical half bridge converters and it is connected to the three single phase transformers.

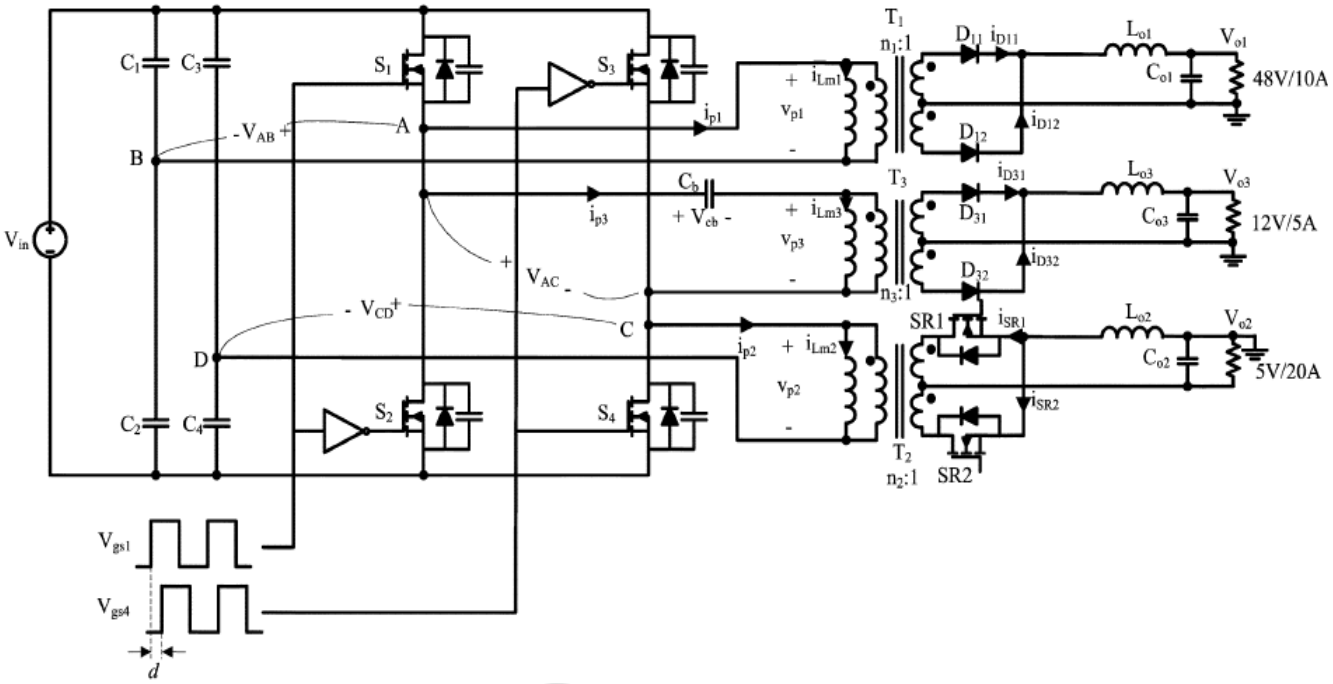


Fig.2.1 Three Multiple output ZVS dc–dc converter

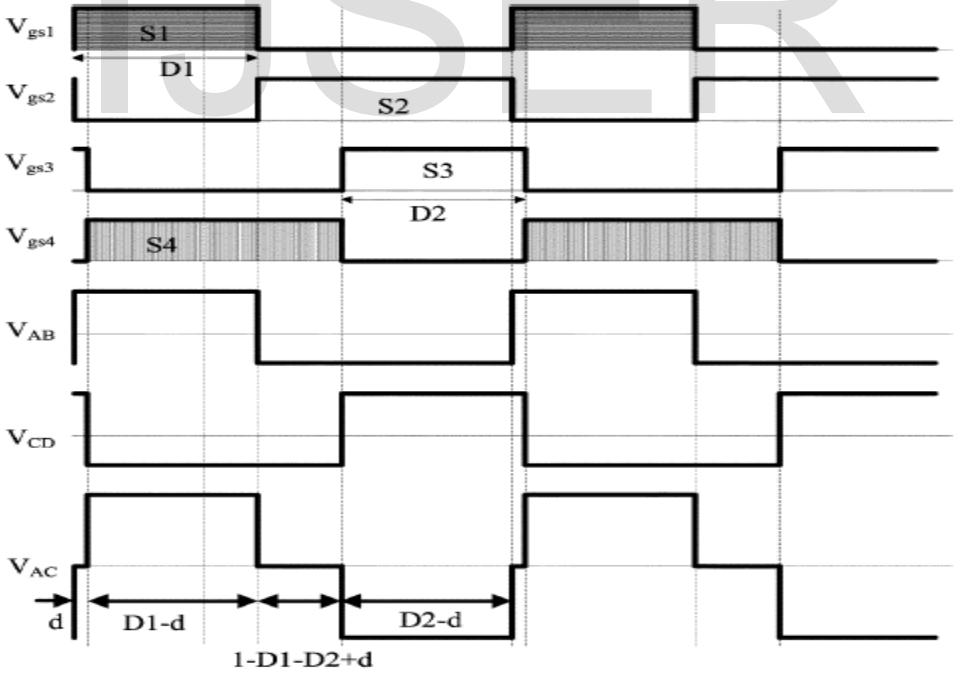


Fig.2.2 Control signals of the three multiple-output dc–dc converter

2.1 DESIGN CONSIDERATION OF THE PROPOSED MULTIPLE OUTPUT DC–DC CONVERTER

The multiple-output ZVS dc–dc converter is shown in Fig.2.1 Since the second output $V_{02}$is low voltage and high

current output, we use self-driven synchronous rectification to reduce rectification loss and improve efficiency. All three outputs are regulated through the switches in the primary side. The control signals are shown in Fig.2.2, where V_{AB} and V_{CD} are the voltage across transformer T1 and T2, respectively, while $V_{AC}$is the voltage applied to blocking capacitor C_b and transformer T3.

The first output $V_{01}$is regulated through the duty cycle of the first asymmetrical half bridge converter which is composed of switches S1–S2 and capacitors C1–C2. Based on the phase shift between two asymmetric half bridge converters, the third output is controlled which is composed of switches S3–S4 and capacitors C3–C4. Based on the phase shift between two asymmetric half bridge converters, the third output is controlled. Since ZVS can be realized for all the main switches, this converter operates at high efficiency under high switching frequency.

According to the volt-second balance of the output inductors, we can derive the output voltages of the converter.

The first output voltage V_{01} is

$$V_{01} = 2.V_{in}.D_1.(1 - D_1).\frac{1}{n_1} \qquad (2.1)$$

Where $V_{in}$is the input dc voltage, $D_1$is the duty cycle of the first asymmetrical half bridge converter,n_1 is the turn ratio of transformer T1.

The second output voltage V_{02} is

$$V_{02} = 2.V_{in}.D_2.(1 - D_2).\frac{1}{n_2} \qquad (2.2)$$

Where V_{in} is the input dc voltage,$D_2$is the duty cycle of the second asymmetrical half bridge converter,n_2 is the turn ratio of transformer T2.

The expression of the third output voltage V_{03} is different and depends on both duty cycles D_1 and D_2 . When duty cycle D_1 is larger than duty cycle D_2 , the third output voltageV_{03} is

$$V_{03} = V_{in}.(D_1 + D_2 - 2.d).\frac{1}{n_3} + V_{in}.(D_1 - D_2).(1 - 2.D_1 + 2.d)\frac{1}{n_3} \qquad (2.3)$$

when duty cycle $D_1$is smaller than duty cycleD_2 , the third output voltage V_{03} is

$$V_{03} = V_{in}.(D_1 + D_2 - 2.d).\frac{1}{n_3} + V_{in}.(D_2 - D_1).(1 - 2.D_2 + 2.d)\frac{1}{n_3} \qquad (2.4)$$

Where V_{in} is the input dc voltage,D_1 andD_2 are the duty cycles of the first and second asymmetrical half bridge converters respectively, d is the phase shift of the switch S4 to the switch S1, and n_3 is the turn ratio of transformer T3.

For simplifying the expression of the third output voltageV_{03}, we compare the two equations.

Therefore, the third output voltage V_{03} can be simplified as

$$V_{03} = V_{in}.(D_1 + D_2 - 2.d).\frac{1}{n_3} \qquad (2.5)$$

2.2 OPERATION STAGES OF THE PROPOSED THREE MULTIPLEOUTPUT DC–DC CONVERTER

Before the analysis, we first make the following assumptions.

- The duty cycles $D_1$and D_2 are both near 0.5 and almost same, so the voltage across capacitorC_b, which is (D_1 -D_2).V_{in}(When duty cycle D_1 is larger than duty cycle D_2) or (D_2 -D_1).V_{in} (When duty cycle $D_1$is smaller than duty cycle D_2), and is very small compared to the input voltage V_{in} , and therefore can be ignored.
- The ZVS of the switches S1–S2 is realized through the energy stored in the output inductor of the third output and the ZVS of the switches S3–S4 is realized through the energy stored in the leakage inductor of transformer T2 and T3.
- The capacitors C1–C4 and C_b are so large that the voltages across them are considered to be constant.
- The output inductors are so large that they are considered as current sources.

The operating modes of the proposed converter are shown in the figures from 2.3 to 2.13.

Stage1 (t0–t1): Before the starting of this stage, the controlled switches S1 and S3 are on, and the first and second outputs are transferring energy to the load while the third output is freewheeling. At time t0, the switch S3 is turned off. The sum of primary current i_{p1}andi_{p2} begins to charge the parasitic capacitance of the switch S3, and discharge the parasitic capacitance of the switch S4. The voltageV_{AC} turns positive, so the current through the diode D31 begins to increase from zero. The diodes D31 and D32 conduct simultaneously and the voltage across the transformer T3 $V_{p3}$is clamped to zero.

Stage2 (t1–t2): At the time of t1, the parasitic capacitance voltage of switch S4 is discharged toD_2V_{in}. Since the voltage across the capacitor C4 isD_2V_{in}, the voltage V_{CD} is zero. Therefore, the current through the synchronous rectifierSR2 begins to decrease and the current through the synchronous rectifier SR1 begins to increase from zero. Since the synchronous rectifiers SR1 and SR2 conduct simultaneously, the voltage across the transformer T2V_{P2} is clamped to zero.

Stage3 (t2–t3): At the time of t2, the parasitic capacitance voltage of switch S4 is discharged to zero. Then the sum of currenti_{p2}andi_{p3} begins to flow through the

body diode of the switch S4, creating ZVS condition for the switch S4.

Stage4 (t3–t4): At time t3, the gate signal of the switch S4 is applied, and the switch S4 is ZVS turned on. Then the sum of currenti_{p2} and i_{p3} begins to flow through the switch S4.

Stage5 (t4–t5): At time t4, the current through the synchronous rectifier SR2 decreases to zero and the current through the synchronous rectifier SR1 increases to the second output current.

Stage6 (t5–t6): At time t5, the current flowing through the secondary side diode D32 starts decreasing to zero and the current through the diode D31 increases to the third output current.

Stage7 (t6–t7): At time t6, the switch S1 is turned off, and the sum of primary currenti_{p1}andi_{p3} begins to charge the parasiticcapacitance of the switch S1 and discharge the parasitic capacitanceof the switch S2.

Stage8 (t7–t8): At the time of t7, the parasitic capacitance voltage of switch S2 is discharged to $D_1 V_{in}$. Since the voltage across the capacitor C2 is $D_2\, V_{in}$, the voltage V_{AB} is zero. The current through the diode D11 begins to decrease and the current through the diode D12 begins to increase from zero. As the diode D11 and D12 conduct simultaneously, the voltage across the transformer T1V_{p1} is clamped to zero.

Stage9 (t8–t9): At the time of t8, the parasitic capacitance voltage of the switch S2 is discharged to zero. Then the sum of primaryi_{p1}current i_{p3} and begins to flow through the bodydiode of the switch S2, creating ZVS condition for the switchesS2.

Stage10 (t9–t10): At time t9, the gate signal of the switchS2 is applied, and the switch S2 is ZVS turned on. The sum of primary current i_{p1} and i_{p3} begins to flow through the switchS2.

Stage11 (t10–t11): At time t10, the current through the diodeD11 decreases to zero and the current through the diode D12increases to the first output current.

2.3. ZVS ANALYSIS OF THE PROPOSED MULTIPLE OUTPUT DC–DC CONVERTER

ZVS of the switches S1 and S2 can be realized through the energy stored in the output inductor of the third output The ZVS of the switches S3 and S4 can be realized through the energy stored in the leakage inductor of transformer T2 and T3. To make sure all the main switches can realize ZVS at full load conditions, we can calculate the needed leakage inductance of transformer T2 and T3.

2.4 SIMULINK MODEL OF THE THREE MULTIPLE OUTPUTS DC-DC CONVERTER

The Simulink model of the three outputs converter as shown in the figure 2.14. In this model we have taken 400V input to the full bridge inverter. The full bridge inverter which is converted direct current into alternative current. The output of the inverter is fed to the linear transformer, and connected to diode bridge rectifier which is converted alternative current into direct current.

The first output V_{01} is regulated through the duty cycle control of the asymmetrical half bridge converter which is composed of switches S1-S2 and capacitors C1-C2. The second output voltage outputs V_{02} is regulated through the duty cycle control of the asymmetrical half bridge converter which is composed of switches S3-S4 and capacitors C3-C4. The third output voltage outputs V_{03} is regulated through the phase shift of two asymmetrical half bridge converters. The control signal of the proposed three output converter as shown in the figure 2.14

2.5 ZVS CONDITIONS OF THE THREE OUTPUTS DC-DC CONVERTER

The fig.2.16 and fig.2.17 shows the gate pulse and voltage across switch S1. Two stages of ZVS conditions of switch as shown, when pulse is ON the voltage across the switch is zero and when pulse is OFF the voltage across the switch is zero. Fig.4.4 (a) shows the ZVS condition of switch S1 from Off to On state and (b) shows the ZVS condition of switch S1 from On to Off state. The multiple output voltage and current waveforms of the proposed converter is shown in the figures 2.18 and 2.19.

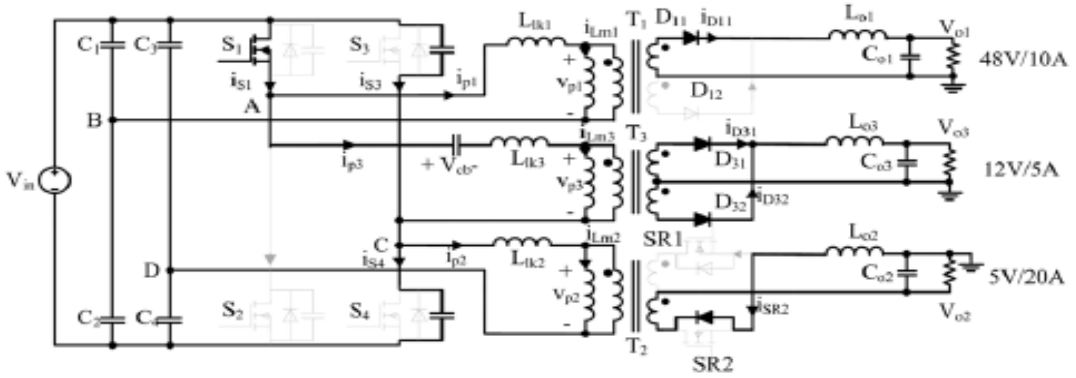


Fig.2.3Mode 1of the proposed multiple-output dc–dc converters

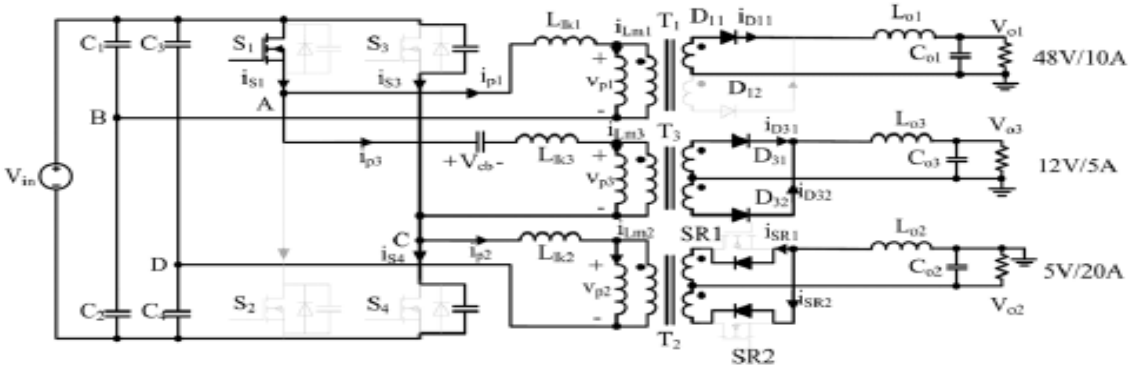


Fig.2.4Mode 2 of the proposed multiple-output dc–dc converters

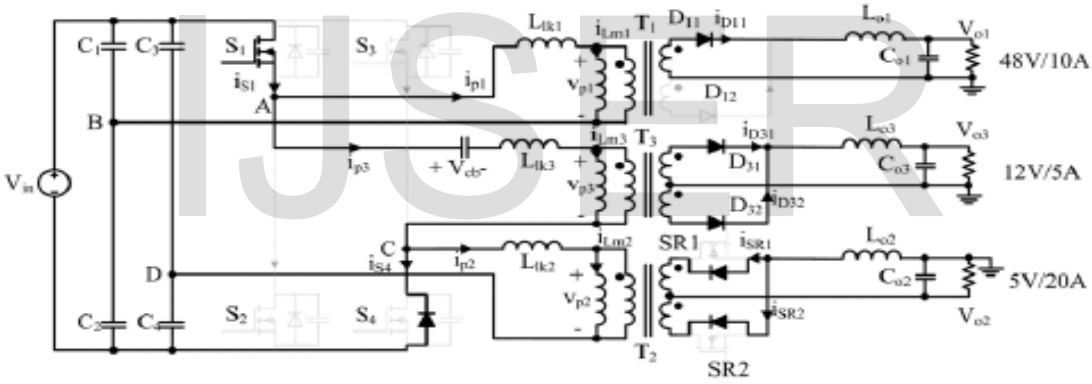


Fig.2.5 Mode 3 of the proposed multiple-output dc–dc converters

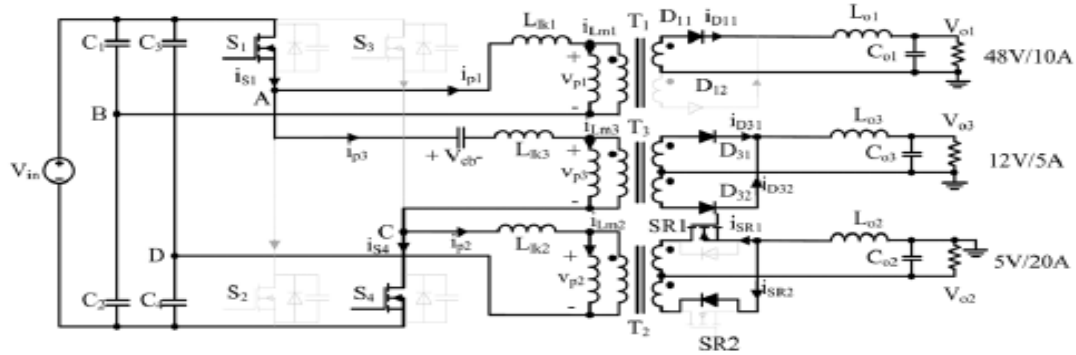


Fig.2.6 Mode 4 of the proposed multiple-output dc–dc converters

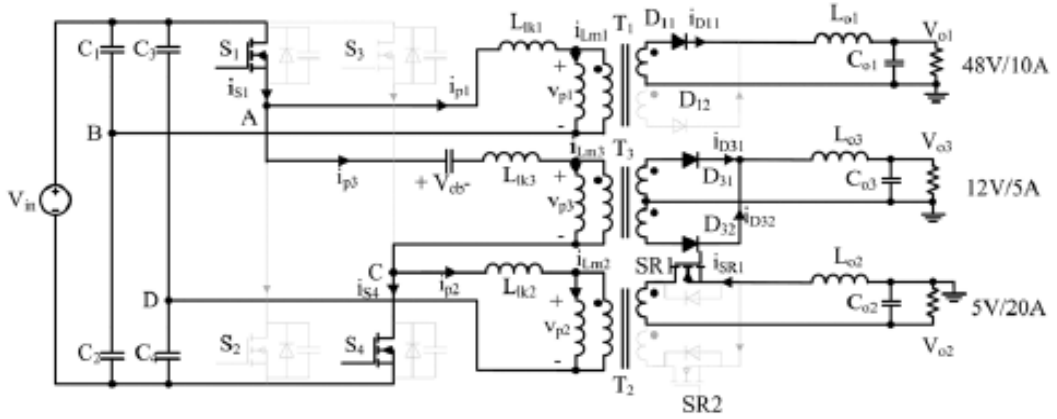


Fig.2.7 Mode 5 of the proposed multiple-output dc–dc converters

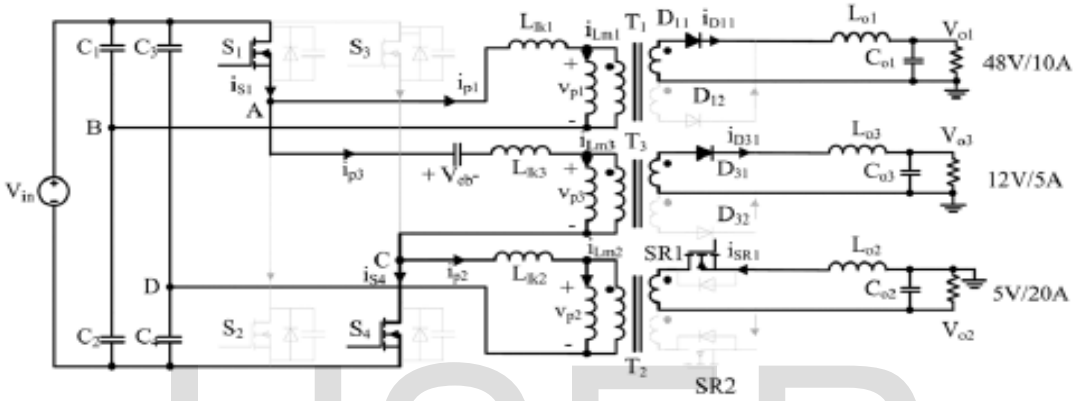


Fig.2.8 Mode 6 of the proposed multiple-output dc–dc converters

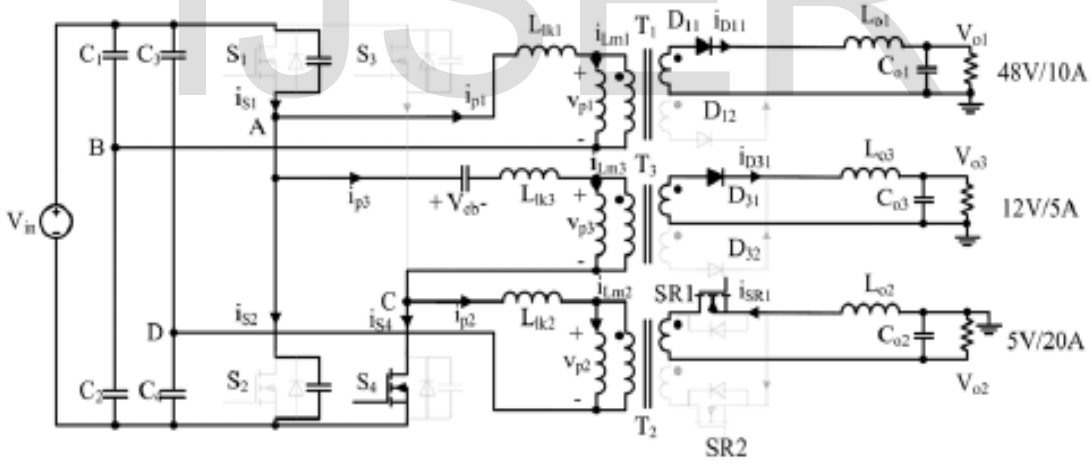


Fig.2.9.Mode 7 of the proposed multiple-output dc–dc converters

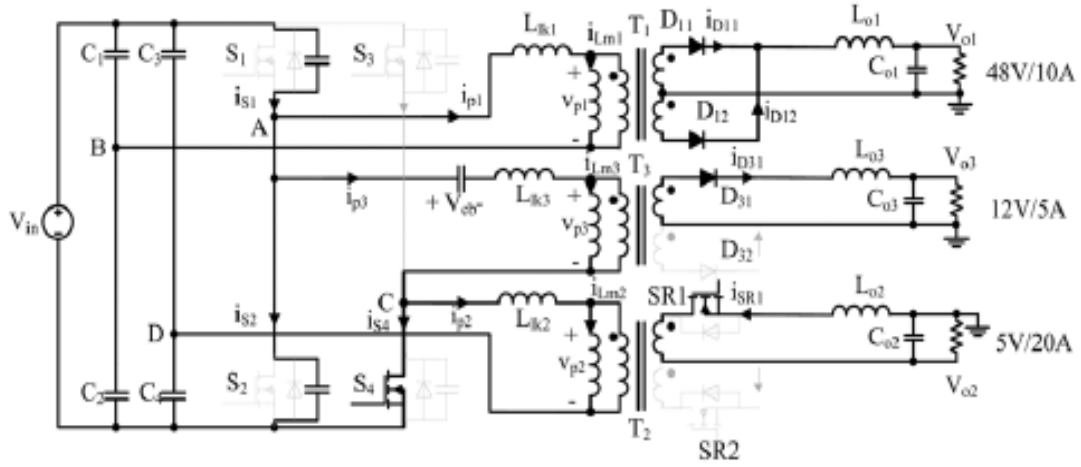


Fig.2.10 Mode 8 of the proposed multiple-output dc–dc converters

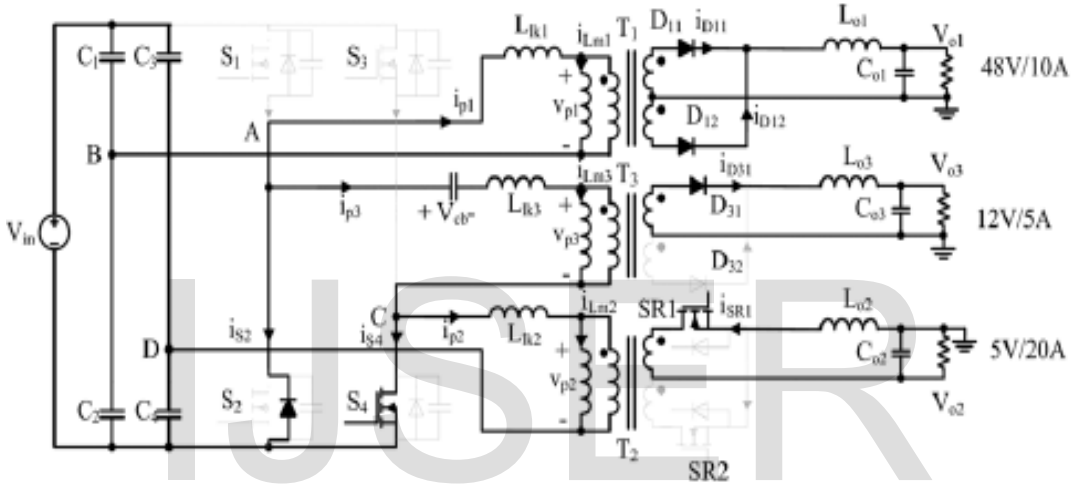


Fig.2.11 Mode 9 of the proposed multiple-output dc–dc converters

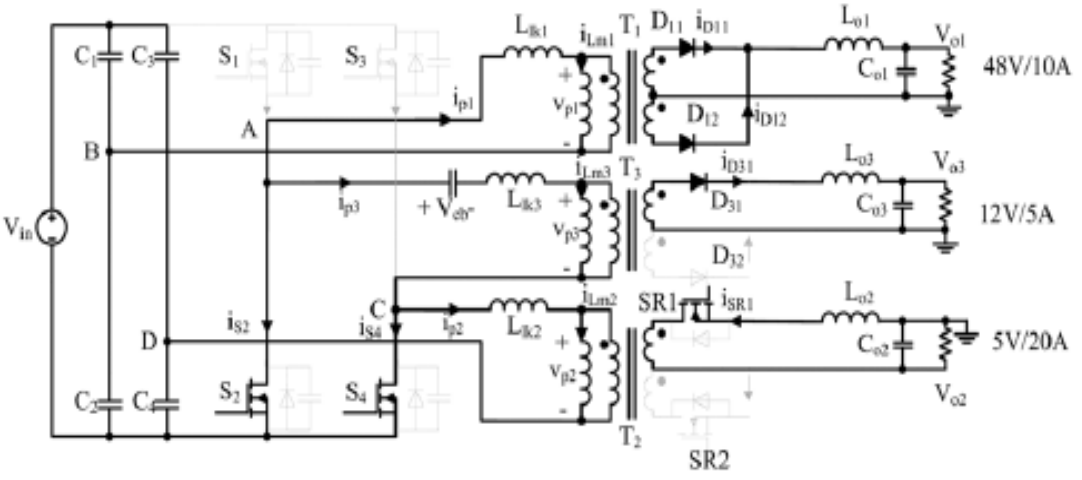


Fig.2.12 Mode 10 of the proposed multiple-output dc–dc converters

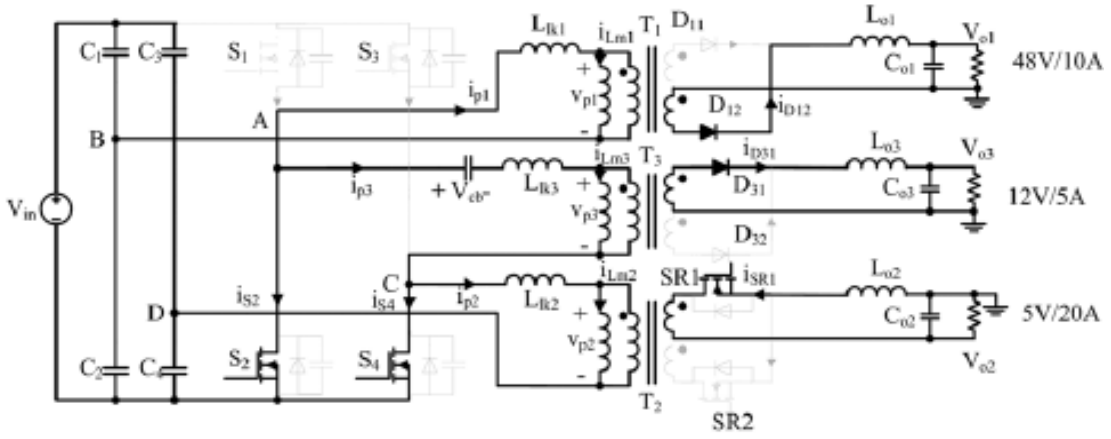


Fig.2.13 Mode 11 of the proposed multiple-output dc–dc converters

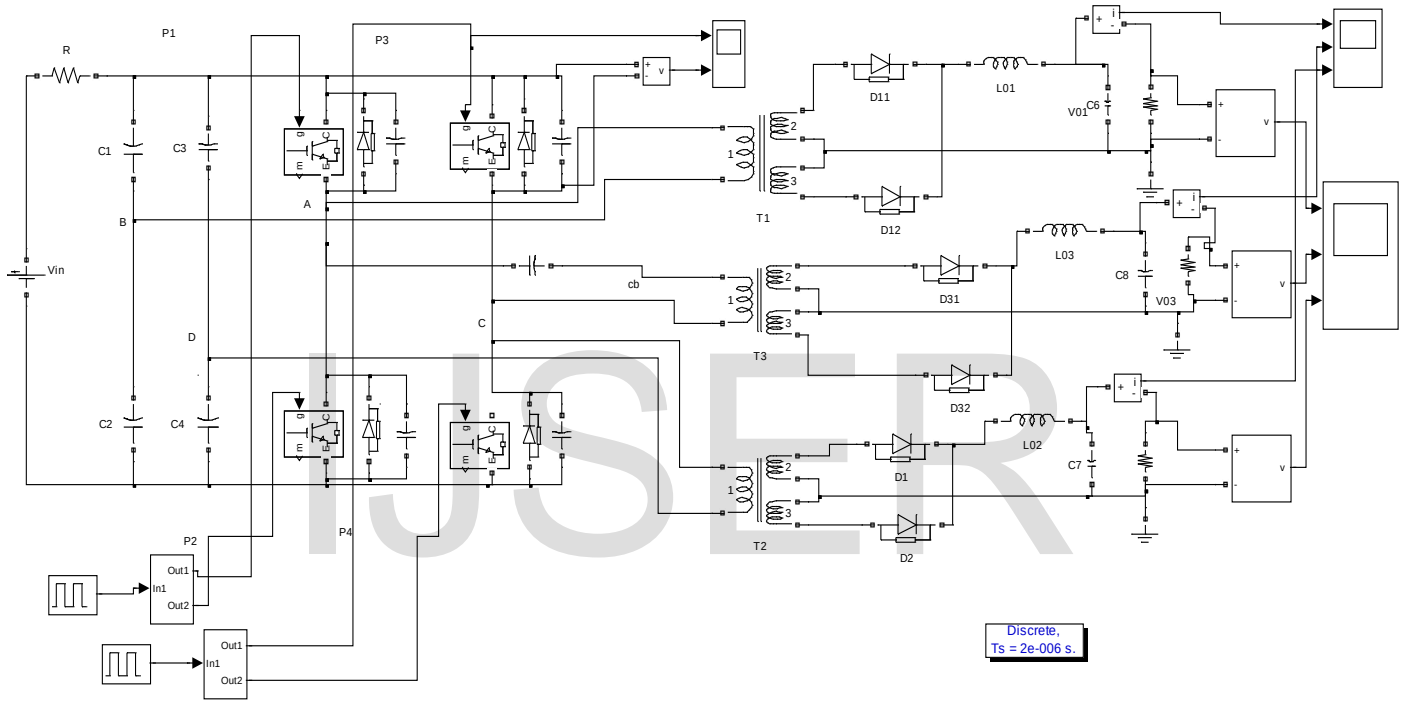
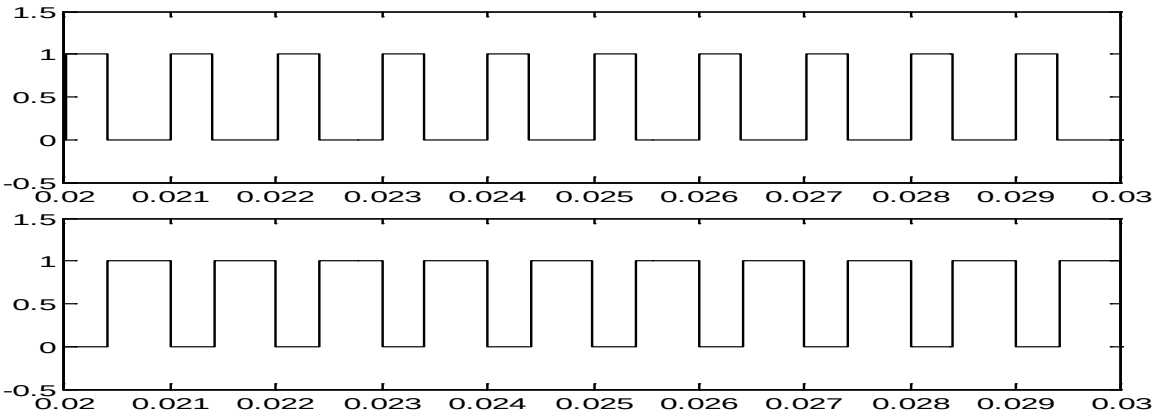


Fig.2.14. Simulink model of open loop multiple outputs DC-DC converter



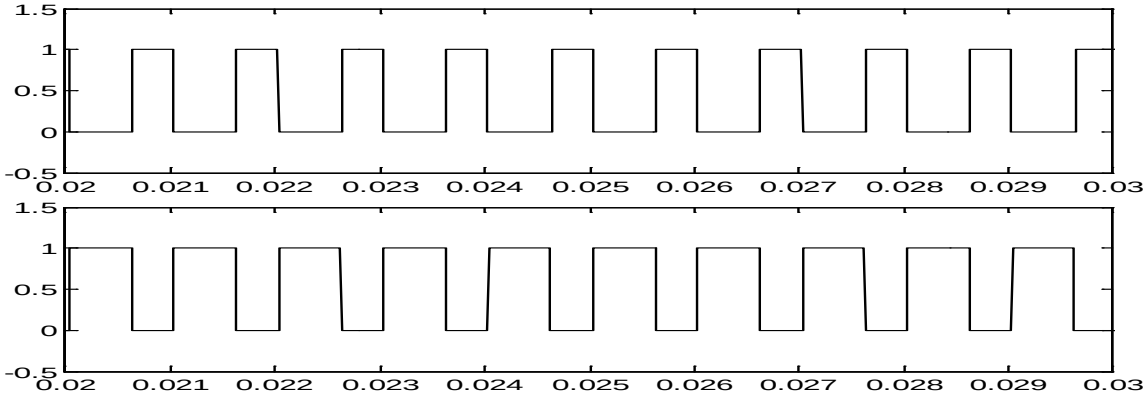


Fig.2.15. Control signal of the multiple outputs converter

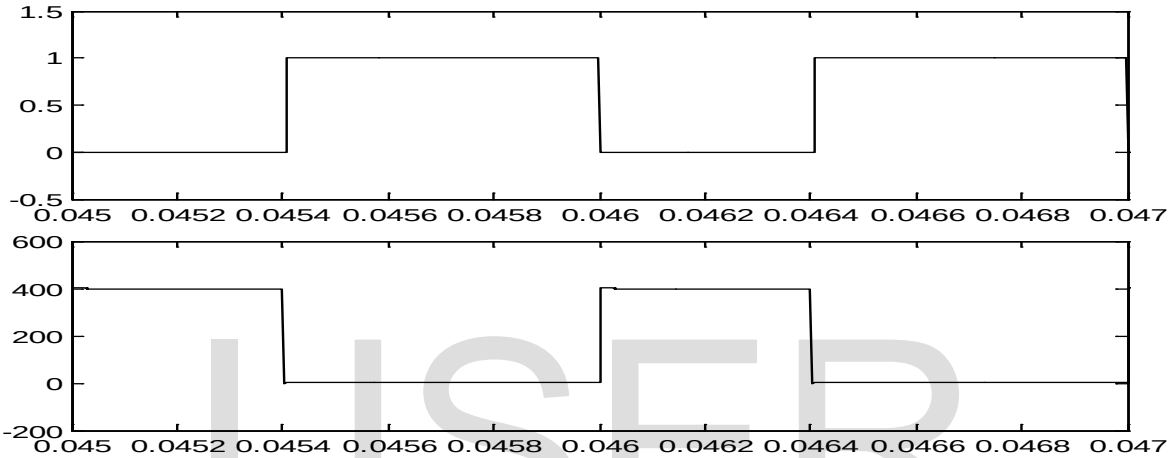


Fig.2.16. Gate pulse and voltage across switch S1

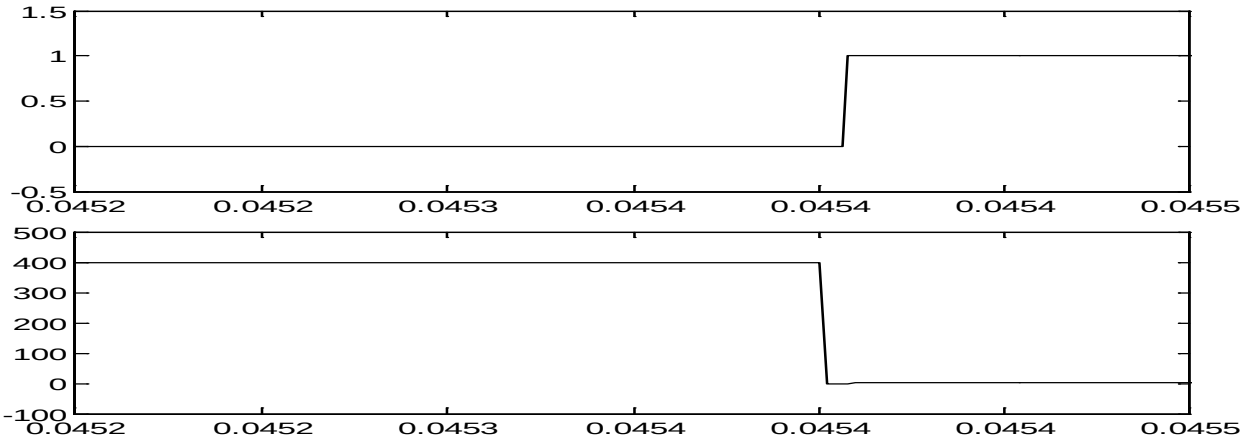


Fig.2.17 (a) ZVS condition of Switch S1 from Off-On state

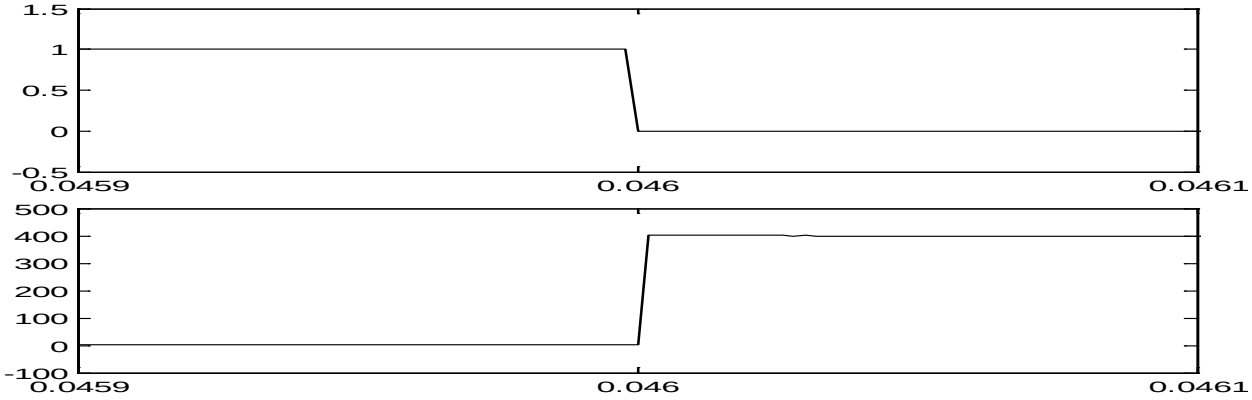


Fig.2.17 (b) ZVS condition of Switch S1 from On-Off state

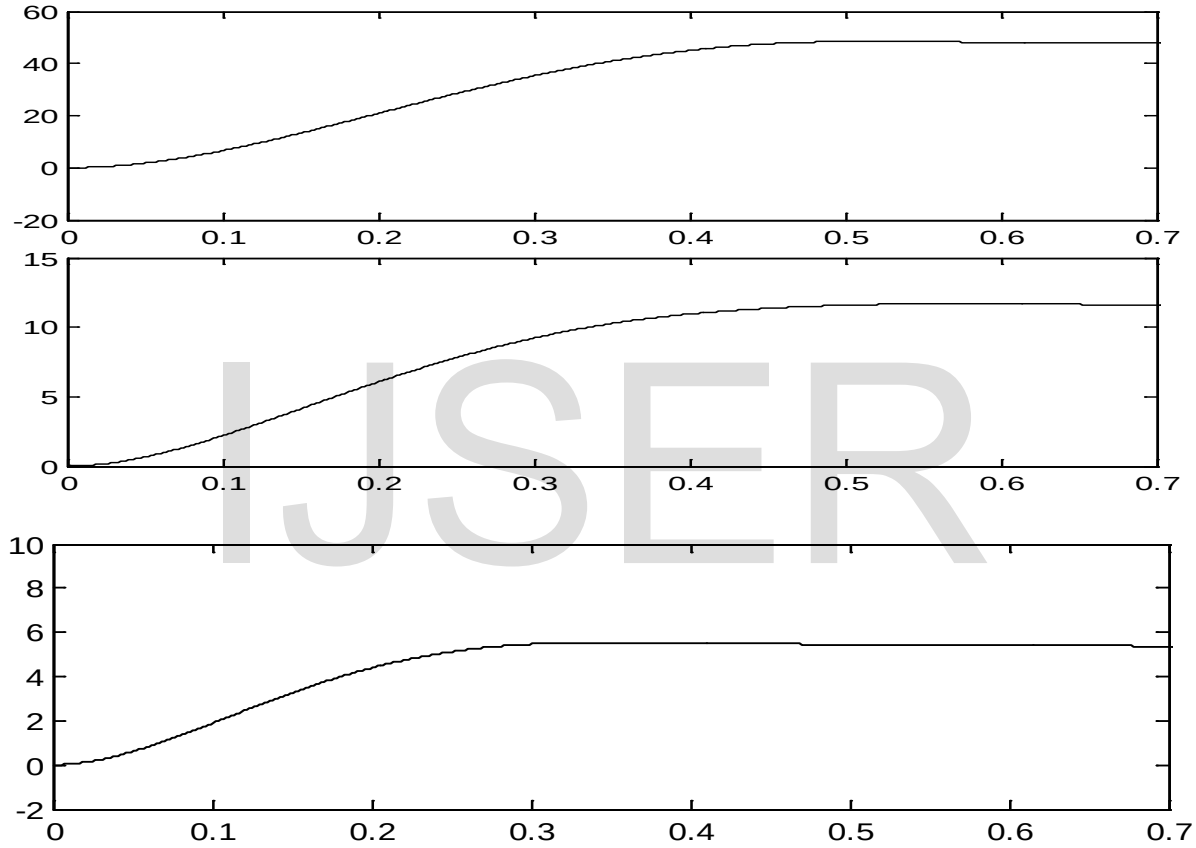


Fig.2.18. Output voltage wave forms of the proposed three output converter

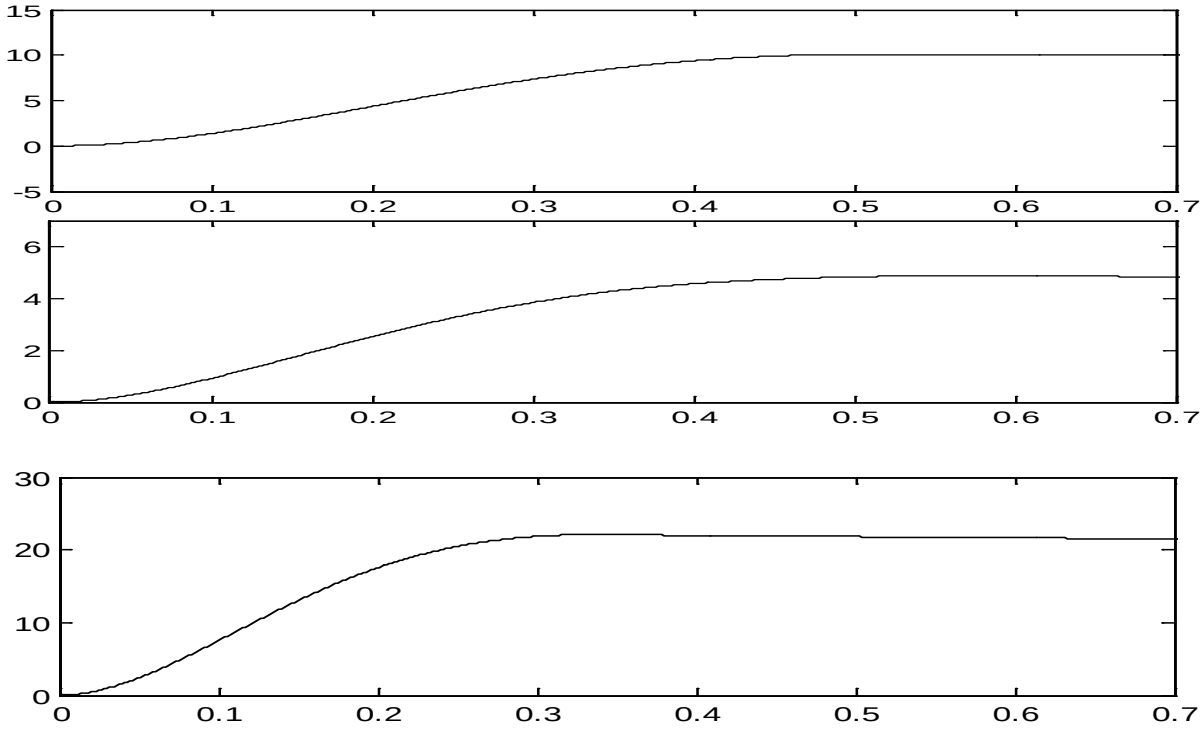


Fig.2.19.Output current wave forms of the proposed three output converter

3. CLOSED LOOP CONTROL OF THE THREE MULTILPE OUTPUTS DC-DC CONVERTER

In this closed loop mode we are also taken 400V as a input voltage. The output voltage of the inverter is connected to the three single phase transformers and to diode bridge rectifier to convert alternative voltage onto direct voltage. Three different output voltages 48V/10A, 12V/5A and 5V/20A are obtained. The block diagram of proposed closed loop control of ZVS DC-DC converter is shown in figure 3.1.The Simulink model of the closed loop proposed three output voltage converter as shown in the figure 3.2.

The detailed control block of the closed loop proposed three output converter as shown in the figure 3.2.In this model we are taken three outputs as a feedback control. Compare the reference voltage and feedback voltage by using error amplifier. The error signal is given to PWM comparator to compare the ramp signal which is having 1000Hz frequency and error signals and gives pulse to the switch S4 and inverted pulse is given to the switch S3 of the proposed three outputs converter. By using remaining two outputs we generate a pulse and it is given to the switch S1 and inverted pulse is given to the switch S2 of the proposed three outputs converter.

During the time of turn-off and turn-on conditions, the power electronic devices have to withstand large currents and voltages, thus resulting in the high switching stresses and switching losses. To reduce the switching losses and stress we are using zero voltage switching (ZVS). Zero voltage switching (ZVS) conditions of the converter are pulse and switch across capacitor voltages as shown in figures. The zero voltage switching (ZVS) conditions of the four switches at ON time and OFF time period of the pulses and switch across the capacitor voltages are as shown in the below figures.

3.1. ZVS CONDITIONS OF THE THREE MULTIPLE OUTPUTS DC-DC CONVERTER UNDER CLOSED LOOP

The fig.3.3 shows the gate pulses of the proposed closed loop control and fig.3.4 shows gate pulse and voltage across switch S1. Two stages of ZVS conditions of switch S1 as shown, when pulse is ON the voltage across the switch is zero and when pulse is OFF the voltage across the switch is zero. The multiple output voltage and current waveforms of the proposed converter is shown in the figures 3.5 and 3.6.

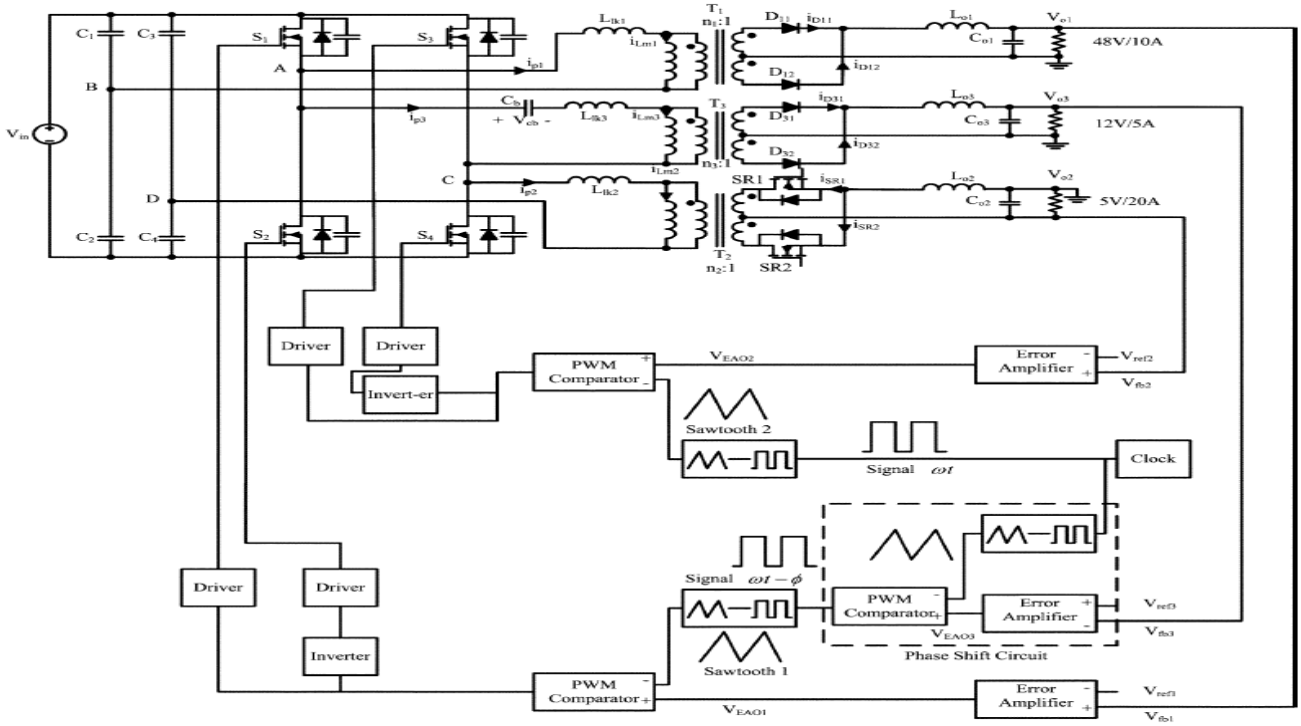


Figure 3.1.Proposed closed loop control circuit of ZVS DC-DC converter

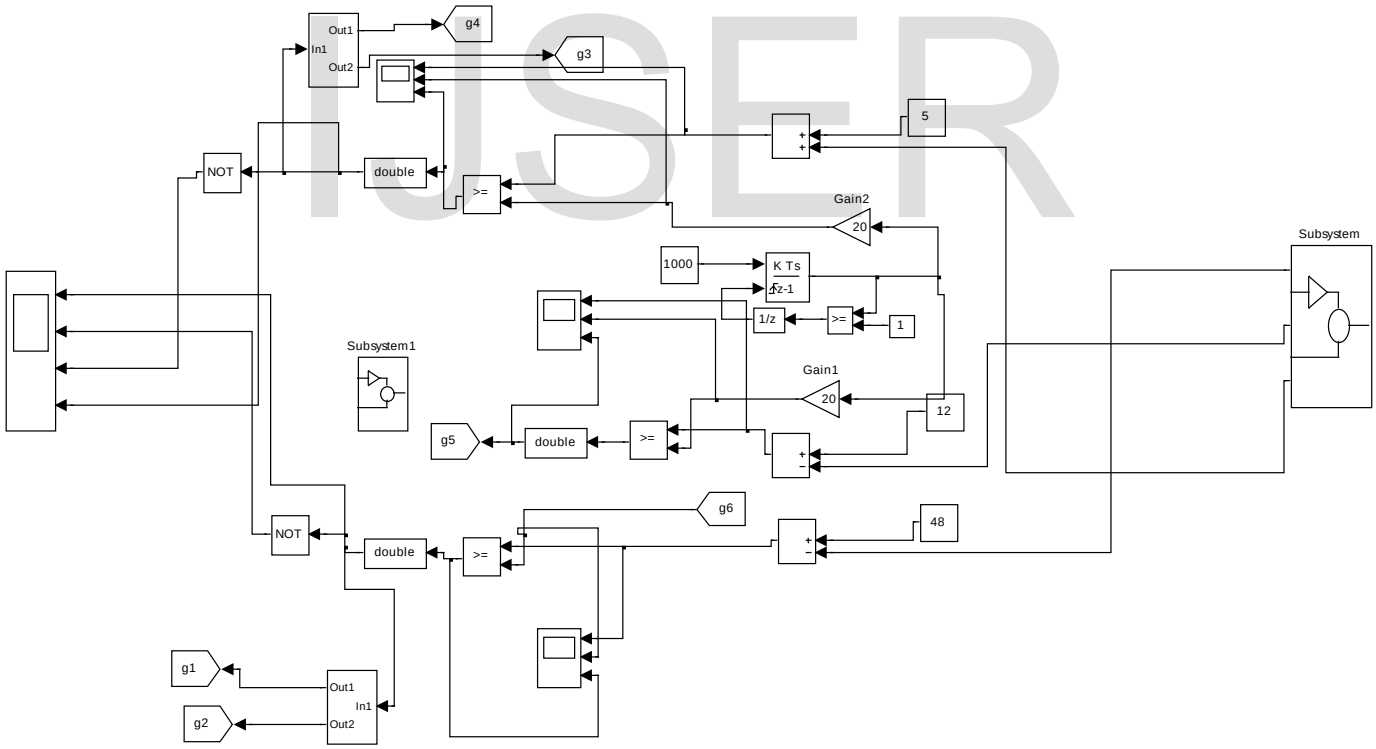


Fig.3.2.Simulink model of closed loop control of proposed three multiple outputs dc-dc converter

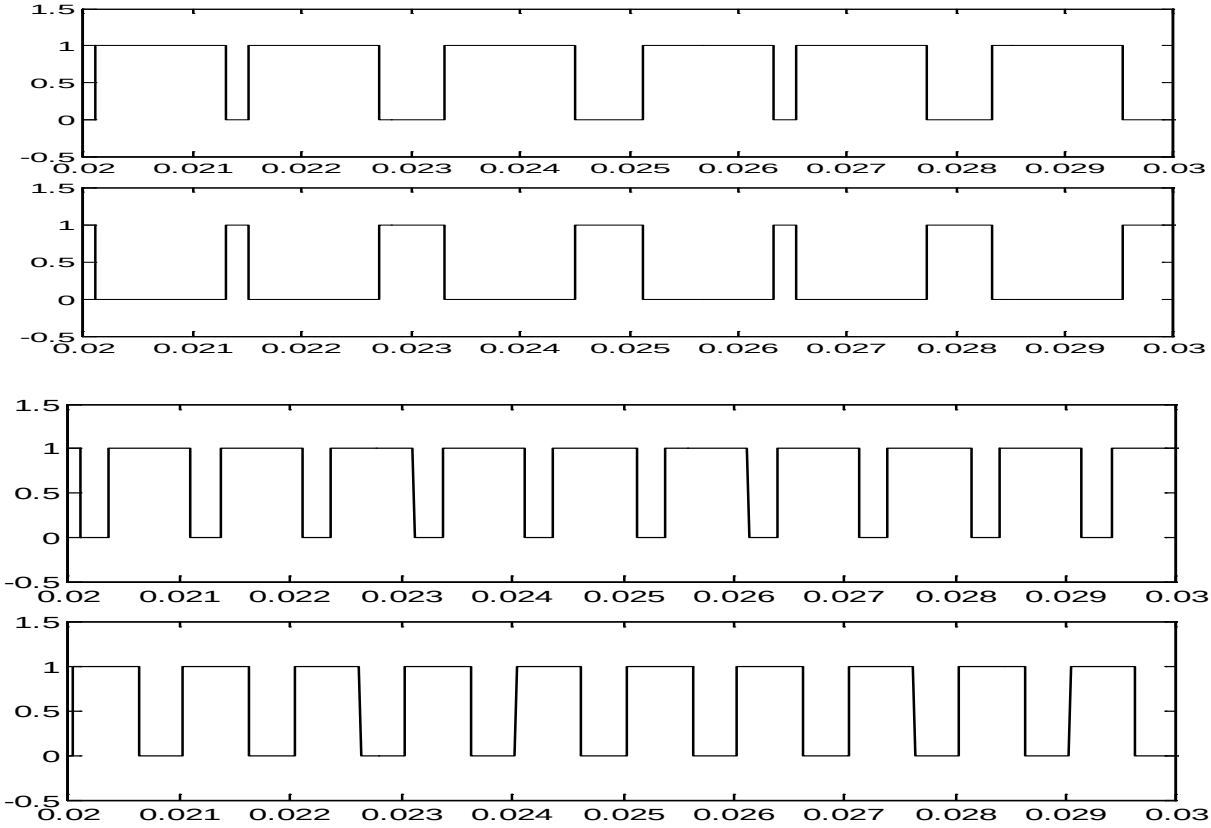


Fig.3.3 Control signal of the proposed three multiple outputs DC-DC converter

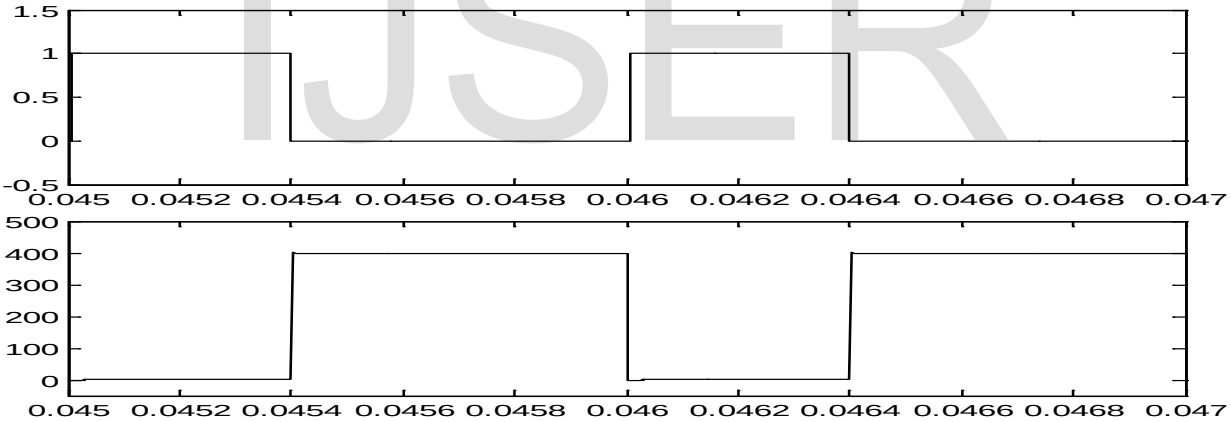


Fig.3.4. Gate pulse and Voltage across switch S1

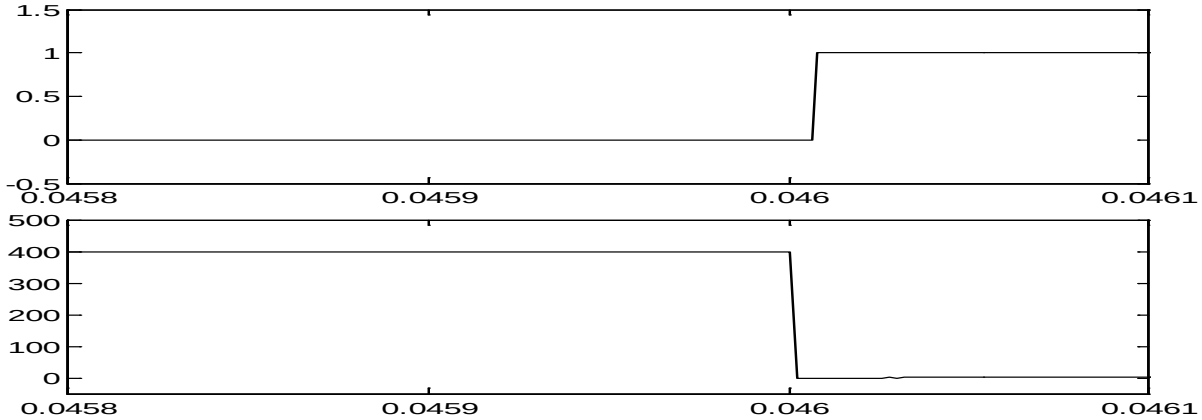


Fig.3.4.(a) ZVS condition of Switch S1 from Off-On state

Fig.3.4 (b) ZVS condition of Switch S1 from On-Off state

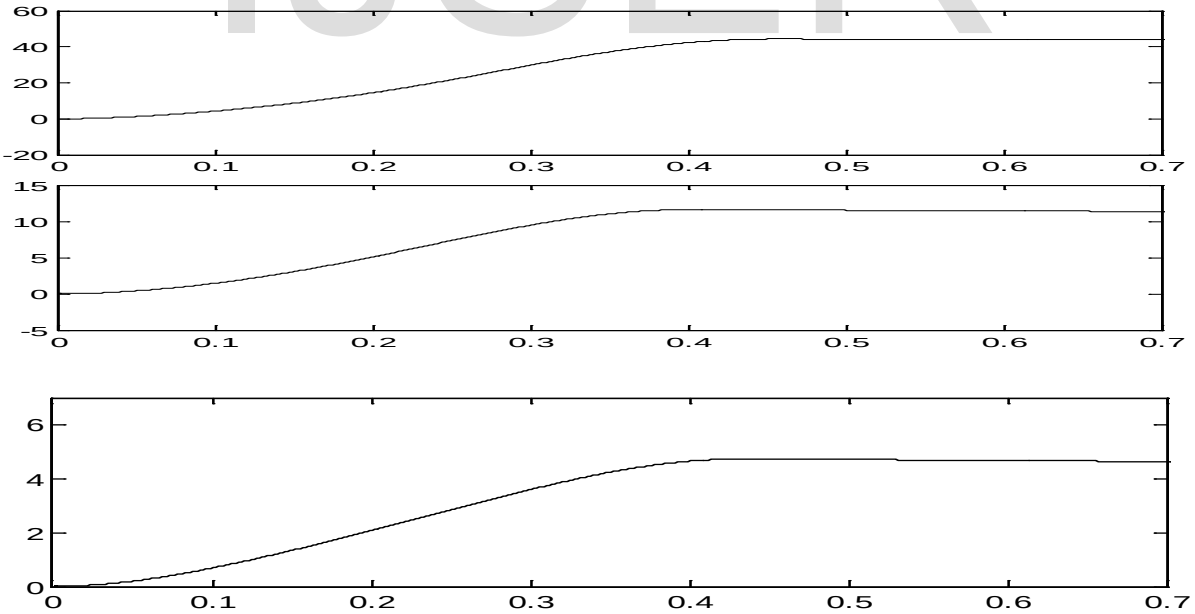


Fig.3.5. Output voltage wave forms of the proposed three outputs converter

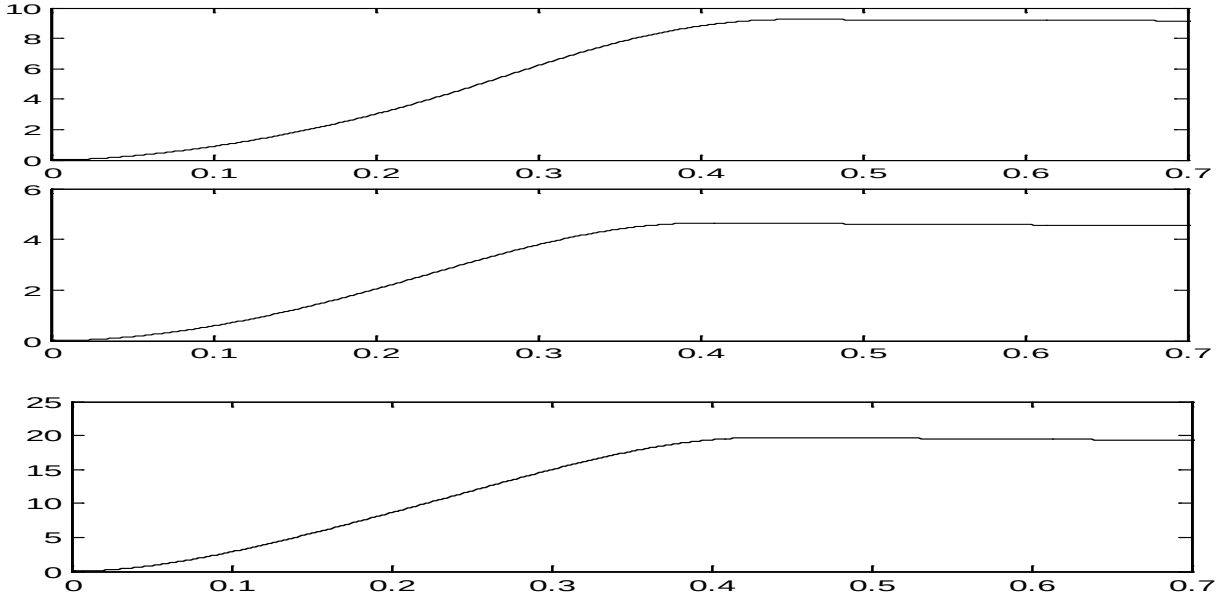


Fig.3.6.Output current wave forms of the proposed three outputs converter

4. CONCLUSIONS:

In multiple-output ZVS dc–dc converter, all the outputs are regulated through the primary side switches. All the main switches can realize ZVS, therefore the converter can work with higher switching frequency and higher efficiency. The operation stages, ZVS condition and control details are also analysed. Although in the proposed converter there are two and three bridge legs and three and five outputs, it can be extended to n number of bridge legs and $2n-1$ outputs. However, the number of the bridge legs is not limited. We can add another bridge leg, two transformers and two rectification circuits to produce additional two outputs. A generalized principle is that it can produce $2n-1$ outputs where n is the number of bridge legs.The simulation of three multiple output zero-voltage switching DC-DC converter was implemented.

5. REFERENCES

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