Analysis of Modified Energy Recovery Flip Flops with Clock Gating

Amit Kumar, Vrinda Gupta

Abstract— Power dissipation has become an important factor while designing the circuits these days. Flip flops are the basic storage element in most of the digital electronics circuits like laptop, mobile, microprocessor, washing machine, microwave etc. So, energy recovery flip flops are used nowadays to reduce power dissipation. In this paper, three modified energy recovery flip flops with clock gating namely single ended conditional capturing (SCCER) flip flop; differential conditional capturing energy recovery (DCCER) flip flop; Static differential energy recovery (SDER) flip flop are proposed. These modified energy recovery flip flops result in significant power saving up to 20-25% as compared to the conventional energy recovery flip flops. These circuits have been implemented on mentor graphics design architect 180 nanometer technology. The power dissipation of modified and conventional energy recovery flip flops have been compared at various clock frequencies.

Index Terms— Energy recovery flip flops, clock frequency, clock gating, low power, conditional capturing, charge sharing, evaluation path

1 INTRODUCTION

CLOCKING is an important aspect and a center piece of digital system design. Not only does it have the highest positive impact on performance and power, but also the highest negative impact on the reliability of an improperly designed system. This is becoming more important, as the clock frequency keeps increasing dramatically as it has been in the last decade. Thus, Clocking is one of the single most important decisions facing the designer of a digital system. Power dissipation related to the clock generation and distribution is identified as the dominating contributor of the total active power dissipation for multi-GHz systems. As the complexity and size of synchronous systems continues to increase, clock power will also increase. This makes novel power reduction techniques absolutely crucial in future VLSI design.

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. The notion of clock and clocking is essential for the concept of synchronous design of digital systems. The synchronous system assumes the presence of the storage elements and combinational logic. The flip flops find their application in frequency divider circuit [1]. The paper describes three modified energy recovery flip flops with clock gating.The topic has been introduced in section 1. Section 2 explains three modified energy recovery flip flops. These circuits have been simulated in the Design Architect and the results are shown in section 3. The topic has been concluded in section 4.

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2 ENERGY RECOVERY FLIP FLOPS

The best approach for energy recovery clocked flip-flops is to locally generate square wave clocks form a sinusoidal clock. This technique has the advantage that existing square-wave flip-flops could be used with the energy recovery clock. However, extra energy is required in order to generate and possibly buffer the local square waves. Moreover, energy is not recovered from gate capacitances associated with clock inputs of flip-flops. Recovering energy from internal nodes of flip-flops in a quasi-adiabatic fashion [2] would also be desirable. However, storage elements of flip-flops cannot be energy recovering because we assume that they drive standard (non-adiabatic) logic. Due to slow rising/falling transitions of energy recovery signals, applying energy recovery techniques to internal nodes driving the storage elements can result in considerable short-circuit power within the storage element. Taking these factors into consideration, we developed flip-flops that enable energy recovery from their clock input capacitance, while internal nodes and storage elements are powered by regular (constant) supply.

2.1 SCCER Flip Flop

Figure 1 shows a Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flop. The NMOS transistor MN3, is controlled by the output QB and provides conditional capturing. No conditional capturing is required in the right hand side evaluation path and moreover the path is static. Placing MN3 above MN4 in the stack reduces the charge sharing [3]. That is because when the charge sharing occurs, the capacitance associated with MN3 is already charged and therefore does not contribute to the charge sharing [4]. The

energy recovery flip flop can also be dual edge triggered [5]. The flip flop dissipates the same amount of power during sleep mode and the active mode. A major portion of the power is dissipated by the clock network. We can save power by disabling the clock network during the sleep mode as significant amount of power is consumed by the clock network. We can disable the clock network by implementing the clock gating due to this for some time, the circuit gets disable. This Figure 1 shows SCCER with clock gating. Clock gating was implemented by replacing the inverter with the NOR gate. The NOR gate has two inputs: the clock signal and the enable signal. In the active mode, the enable signal is low so the NOR gate behaves just like an inverter and the flip-flop operates just like the original flip-flop [6]. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. This turns off the pull down path (MN2) and prevents any evaluation of the data. Hence, not only the internal clock is stopped but also all the internal switching is prevented (power saving on data circuits). The skewed inverter was replaced by a NOR gate. It

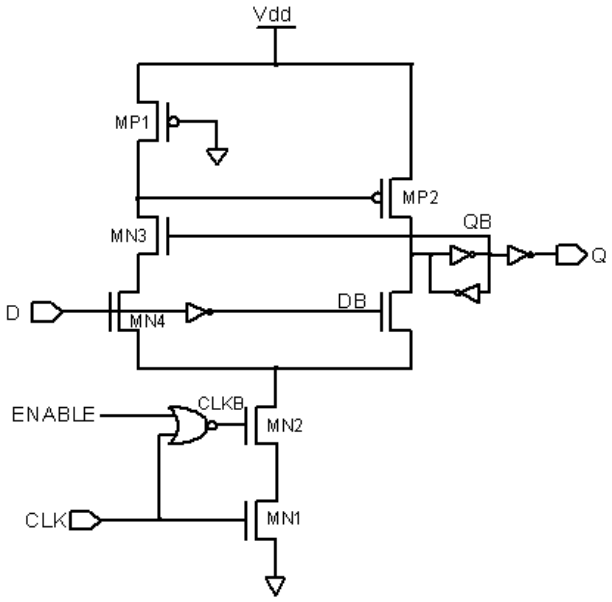

Figure 1 SCCER Flip Flop

should be mentioned that the skew direction for the NOR gate should remain as that in the original inverter gate (skewed for high to low transition; pull-down network stronger than pull-up).

2.2 DCCER Flip Flop

Figure 2 shows the Differential Conditional-Capturing Energy Recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a pre-charge and evaluates fashion. However, instead of using the clock for pre-charging, small pull-up PMOS transistors (MP1 and MP2) are used for charging the pre-charge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based Set/Reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output (Q and QB) to the control transistors MN3 and MN4 in the evaluation paths [4]. Therefore, if the state of the input data (D and DB) is same as that of the output (Q and QB), both left and right evaluation paths are turned off preventing SET and RESET from being discharged. This results in power saving at low data switching activities when input data remains idle for more than one clock cycle [4].Similar to SCCER flip flop, clock gating was implemented by replacing the inverter with the NOR gate [6].

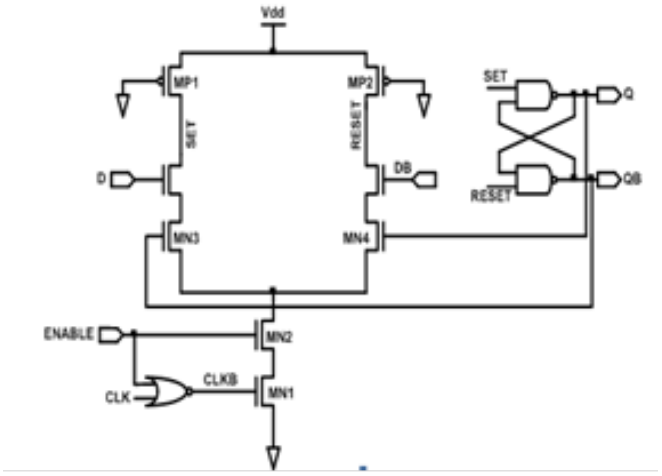

Figure 2 DCCER Flip Flop

2.3 SDER Flip Flop

Figure 3 shows the Static Differential Energy Recovery (SDER) flip-flop. This flip-flop is a static pulsed flip-flop similar to the Dual-rail Static Edge-Triggered Latch (DSETL) [7]. A cascade of three inverters instead of one can give a slightly sharper falling edge for the inverted clock (CLKB). However, due to the slow rising nature of the energy recovery clock, enough delay can be generated by a single inverter. In this flip-flop, when the state of the input data is the same as its state in the previous conduction phase, there are no internal transitions. Therefore, power consumption is minimized for

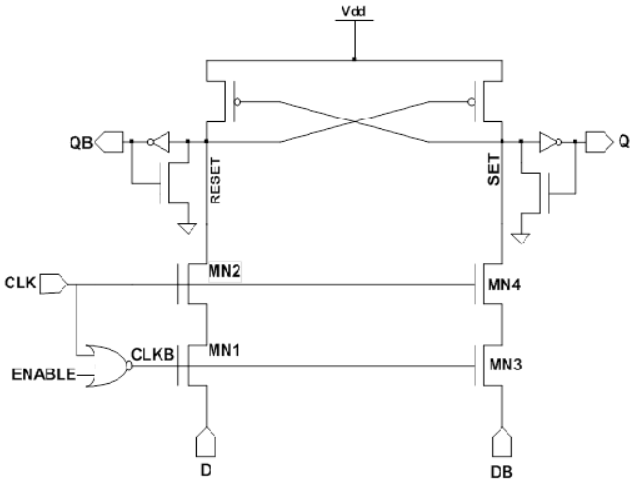

Figure 3 SDER Flip Flop

low data switching activities. The second approach for minimizing flip-flop power at low data switching activities is touse SDER Flip Flop conditional capturing [5] to eliminate redundant internal transitions [4]. Power results show significant savings when the clock gating is applied to the flip-flop during the idle state,[6] replacing inverter with the NOR gate.

3 SIMULATION RESULTS

The Modified SCCER flip flop with clock gating as shown in Figure 5, the gate terminal of MP1 transistor is connected to the drain of same transistor to convert pseudo NMOS to

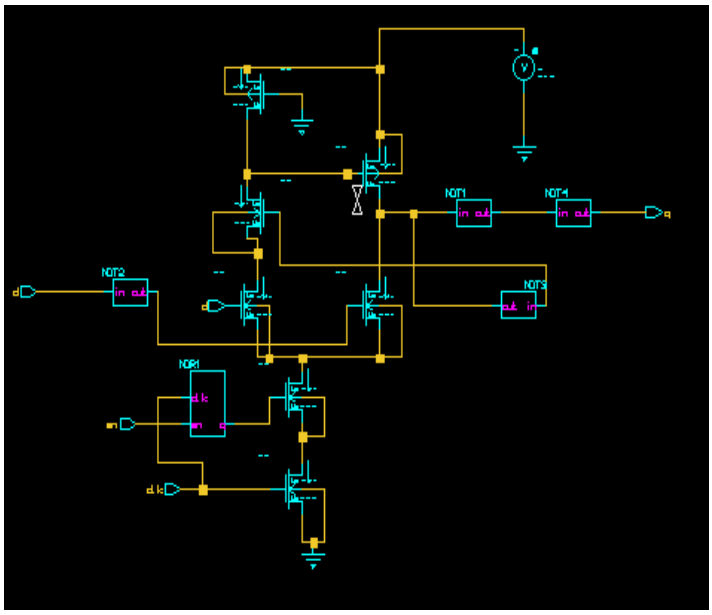

Figure 4 Conventional SCCER Flip Flop with clock gating

adiabatic logic to reduce the power reduction as shown in Figure 5. The working is same when we compare it with conventional SCCER flip flop with clock gating shown in Figure 4. Initially when the enable was equal to zero, the value of d is copied to the output q, when it becomes one, the previous value is stored. The table 1 shows the power dissipation of the conventional and modified SCCER flip flop with clock gating at different values of frequencies. The average power reduction in the modified SCCER flip flop with clock gating is 21%.

Table 1: Power consumption in SCCER flip flop

Frequency (MHz)	Conventional (uW)	Modified (uW)
100	45.67	34.98
150	49.21	45.10
200	61.70	47.37
250	65.93	48.25

The modified DCCER flip flop with clock gating as shown in Figure 7, instead of connecting the gate terminal of transistors MP1 and MP2 to the ground; their gate terminals are connected to each other's drain terminal to convert pseudo NMOS to adiabatic logic. In the conventional DCCER flip flop shown in Figure 6, the PMOS transistors always remain on due to which the power consumption increases. But the switching of transistor will depend on the potential provided at the gate terminal. Rest of the circuit will remain same. DCCER flip-flop uses a NAND-based Set/Reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output (Q and QB) to the control. The modified circuit helps to reduce charge sharing as the clock transistor (MN1), which is the largest transistor in the evaluation path, is placed at the bottom of the stack.Therefore, the diffusion capacitance of the source terminal of MN1 is grounded and does not contribute to the charge sharing. The power dissipation of modified and conventional DCCER flip flop with clock gating at various frequencies is shown in the table 2. The average power reduction in the modified DCCER flip flop with clock gating is around 27.50%.

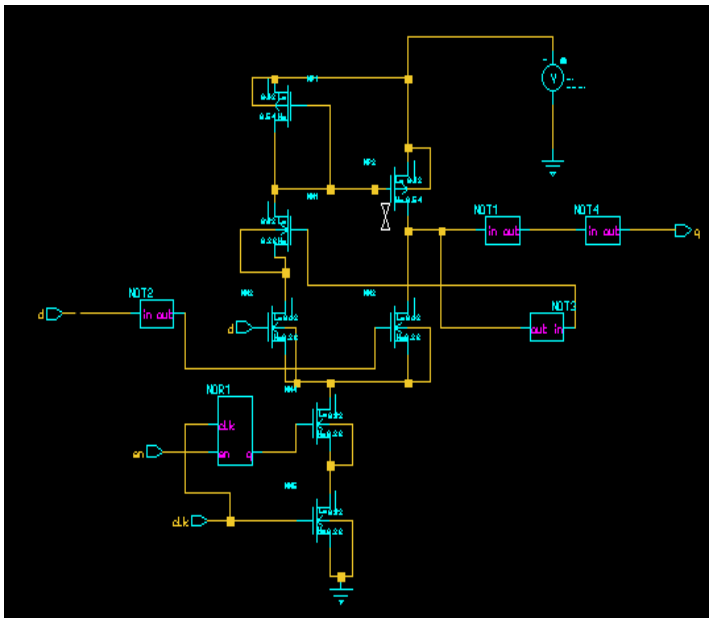

Figure 5 Modified SCCER Flip Flop with clock gating

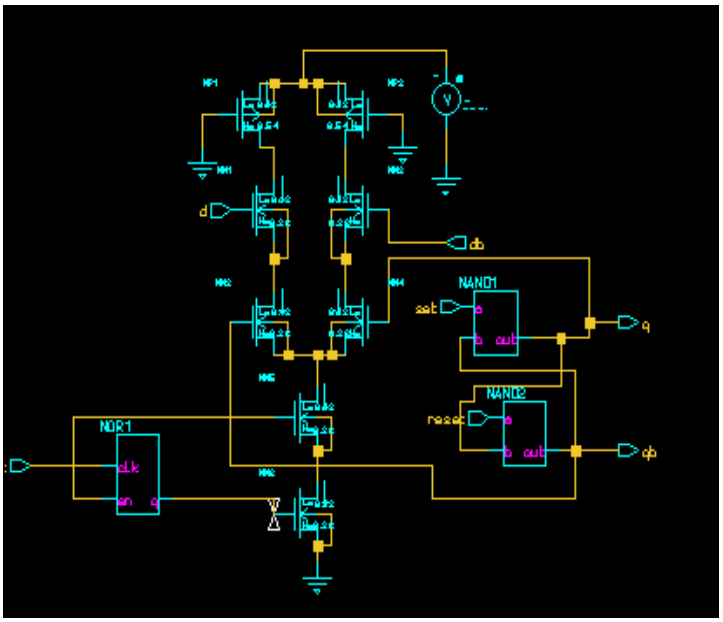

Figure 6 Conventional DCCER Flip Flop with clock gating

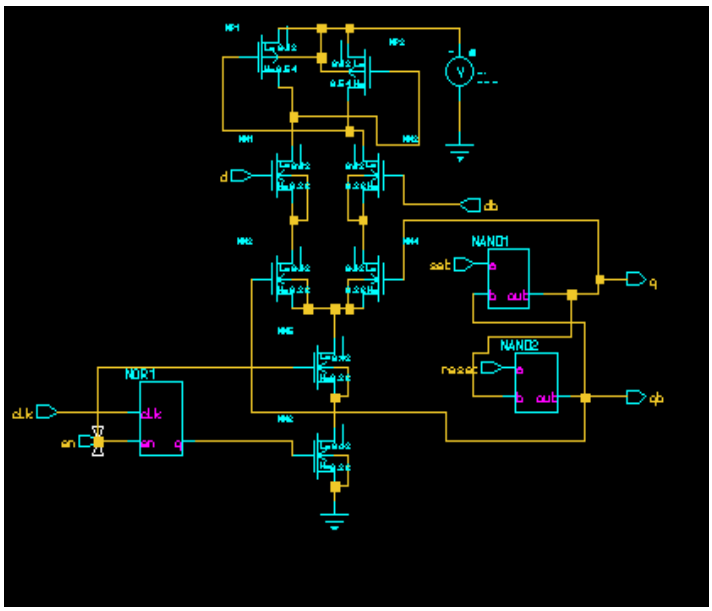

Figure 7 Modified DCCER Flip Flop with clock gating

Table 2: Power consumption in DCCER Flip Flop

Frequency (MHz)	Conventional (uW)	Modified (uW)
100	30.76	23.45
150	40.23	29.50
200	59.36	43.56
250	67.35	45.29

The modified SDER flip flop with clock gating as shown in Figure 9, is same as the conventional SDER flip flop as shown in Figure 8, in working and connection. The only difference is that the evaluating transistors which were connected to the output logic are removed. Due to this the value of output logic will not be prpper zero value.The main advantage of this modification is that it reduces the area and more importantly power dissipation.

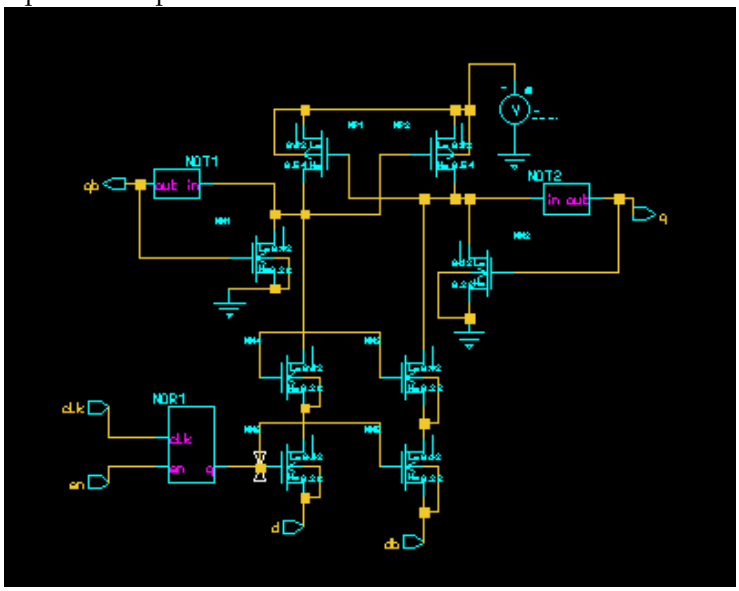

Figure 8 Conventional SDER Flip Flop with clock gating

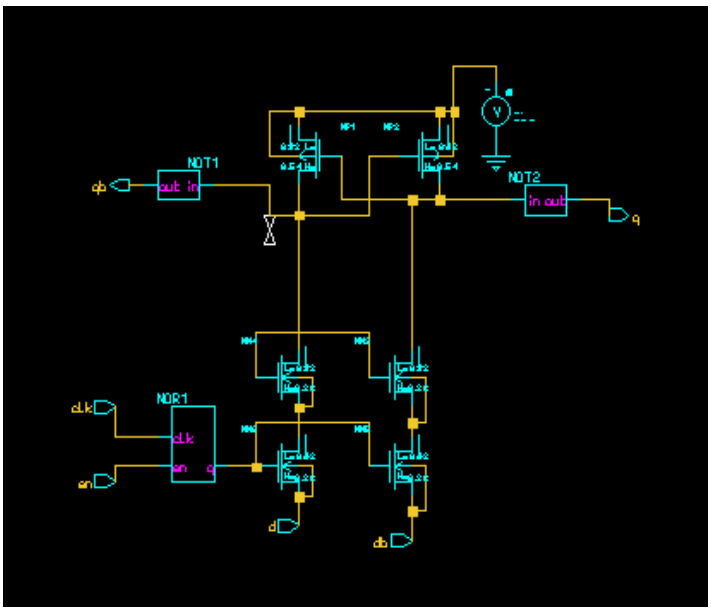

Figure 9 Modified SDER Flip Flop

The table 3 shows the power dissipation of the conventional and modified SDER flip flop with clock gating at different values of frequencies. It can be seen that power consumption increases as the frequency increases. The average power reduction in the modified SDER flip flop with clock gating is around 20.83%.

Table 3: Power consumption in SDER Flip Flop

Frequency (MHz)	Conventional (uW)	Modified (uW)
100	35.76	35.99
150	48.34	36.50
200	56.52	45.48
250	61.97	52.17

4 CONCLUTIONS AND FUTURE SCOPE

In this paper, three novel modified energy recovery flip flops with clock gating have been proposed. These circuits have been simulated in mentor graphics design architect 180 nanometer technology. The Modified energy recovery flip flops result in significant power saving up to 20-25% as compare to the conventional energy recovery flip flops. It can be seen that, the modified energy recovery flip flops with clock gating can also be used in designing the finite state machine like vendor machines, elevators, traffic lights etc. These circuits also find their use in frequency divider circuits which are used in microproceser to reduce the power considerably.

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