Advanced High Speed Low Power Topologically-Compressed Flip-Flop

Sai Nagul Namith, Mrs.Maria Jossy.

Abstract— a modified high speed Flip-Flop (FF) is edge-crafted footnote out of Topologically-Compressed Flip-Flop (TCFF). TCFF reduces power dissipation remarkably and outperforms any other techniques used in conventional FFs. This paper presents a modified TCFF, with techniques which increases the speed and hence maintaining the low power dissipation and less area of TCFF design.

Index Terms— Low power, high speed, CPL, modified TCFF, SIPO.

1 INTRODUCTION

The applications of memory devices are increasing everywhere and it has become the need of the hour to make it low power consuming. So the Large Scale Integration (LSI) comes into the focus as it is the place which have to be overhauled. The LSI's main component which consumes power is the FF's. Low Power FF's are one of the main building blocks of memory devices, power reduction in FF's can be done by removing the precharge circuit. The TCFF comes with a new approach which can replace all the presently used FF's. The paper proposes a high speed i.e., a lower delay TCFF with almost the same power reduction, performance and cell area as compared to the existing TCFF.
Part 1.1 to 1.3 explains the new TCFF, TCFF with CPL (Complementary Pass Transistor Logic) and Modified TCFF with high speed. Part 2 shows the implementation of TCFF in the TFF, SRFF and JKFF. Part 3 implements the modified TCFF using the SIPO (Serial-In/Parallel-Out) Shift Register.

1.1 TCFF

TCFF is a fine low power FF as compared to any conventional FF's. It has been built by transistor merging and topological compression method. It reduces power while maintaining the performance and area. It uses only 3 clock-fed transistors, which is a much lesser count than other FF's, thus helps it to dissipate less power in operation. TCFF comes with a reduced transistor count based on logical equivalency. The circuit consists of no dynamic or pre-charge circuits, so it avoids additional power wastage. TCFF is the latest emerging technology in the low power FF's, it can supersede all the conventional ones. Fig. 13, illustrates when CP (Clock Pulse) is low, the PMOS connected to CP turns on and the master latch becomes the data input mode. VD1 and VD2 are pulled up to power supply level and the input data (D) is stored in the master latch. When CP is high, the PMOS connected to CP turns off, the NMOS connected to CP turns on, and the slave latch becomes the data output mode. At this stage, the data in the master latch is transferred to the slave latch, and given to Q. In this operation, all nodes are fully static and full-swing. The current from the power supply does not flow into the master and the slave latch concurrently because the master latch and the slave latch becomes, active alternately. Accordingly, timing degradation is small on cell performance even though many transistors are shared with no increase in transistor size [1].

1.2 TCFF with CPL logic Style

CPL style can be employed to decrease the delay with a marginal increase in the average power. CPL is generally used in high speed operation. CPL remains one of the simplest, fastest and most frugal of the circuit families using transistor in Pass Transistor Logic. After simulation and analysis of TCFF with CPL, it gives 93% less delay than TCFF.

1.3 Modified TCFF

A new approach is performed, in order to maintain the same area and almost same power dissipation compared to TCFF with an increase in speed. The Modified TCFF promises high speed operation where the CP-Q delay has been reduced significantly related to any the above methods. It uses a cross coupled logic with several Cascaded stage's where the logic acts as a Current Mirror Circuit in order to provide the necessary voltage required. After simulation and analysis of Modified TCFF, it shows 97% less delay than TCFF.

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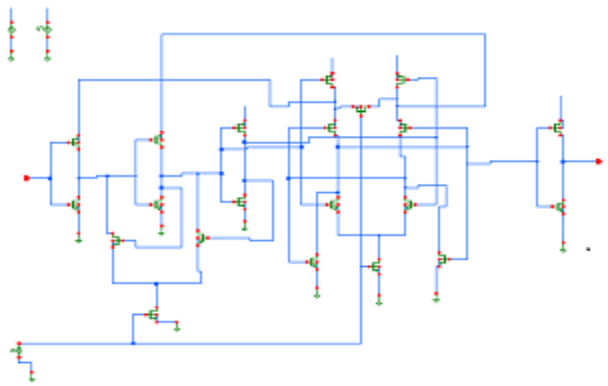

Fig.1 TCFF Schematic Diagram

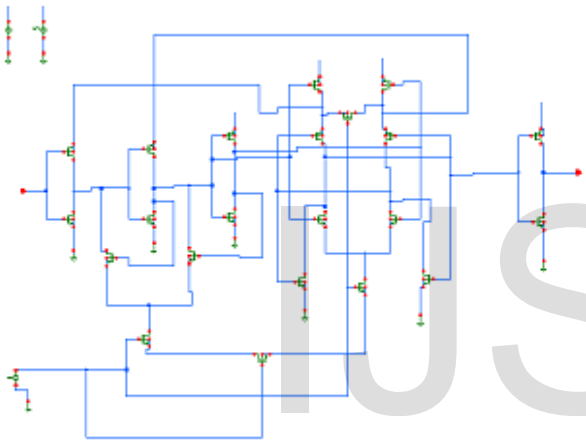

Fig.2 TCFF with CPL logic Style Schematic Diagram

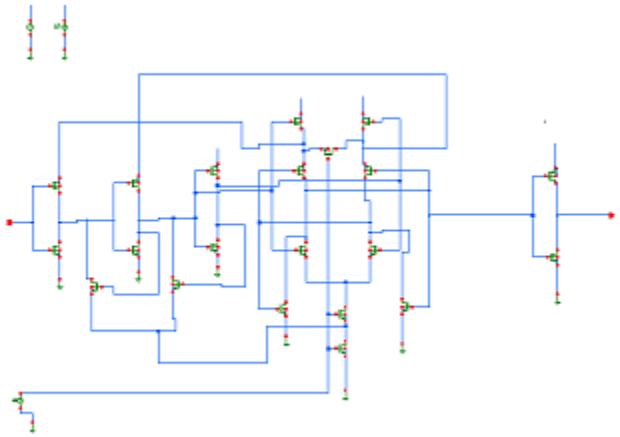

Fig.3 Modified TCFF Schematic Diagram

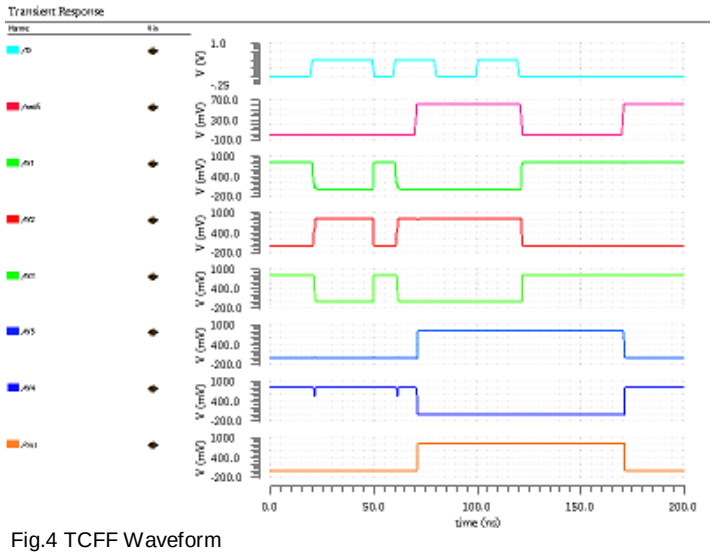

Fig.4 TCFF Waveform

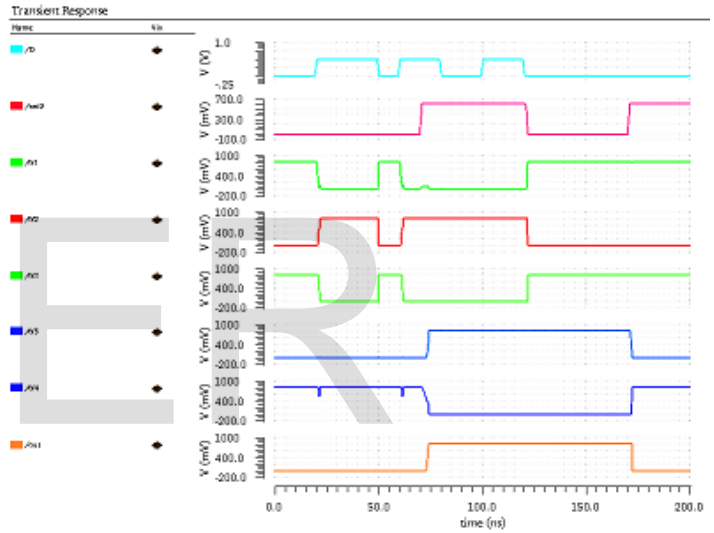

Fig.5 TCFF with CPL logic Style Waveform

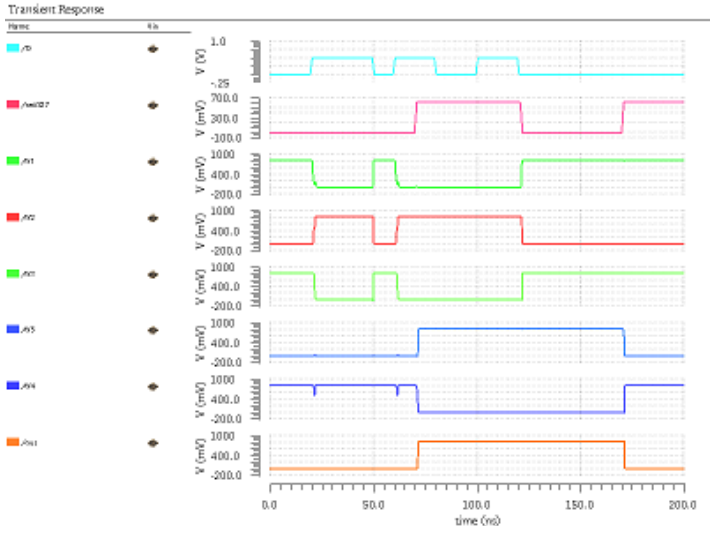

Fig.6 Modified TCFF Waveform

2 IMPLEMENTATION OF TFF, SRFF, JKFF USING MODIFIED TCFF

The Modified TCFF has taken and implemented using TFF, SRFF, JKFF by analysing the average power, CP-Q delay, PDP (Power Delay Product). The DFF is used in all the following implementations of FF's below. Instead of conventional DFF we are using modified TCFF. The T flip flop is designed using XOR (Exclusive-OR) gate and D flip flop. The characteristic equation of D flip flop is given as D=TQb+TbQ. The output of XOR gate is given as input to the N2 transistor of DFF. The XOR gate is designed with the usage of PTL (Pass Transistor Logic) technique. The SR flip flop is designed using a SR block and D flip flop. The characteristic equation of SR flip flop is given as D=S+RbQ . The SR block is designed using static CMOS techniques. The JKFF is designed using a multiplexer and a D flip flop. The characteristic equation of D flip flop is given as D=JQb+KbQ. The output of the multiplexer is fed as input to the D flip flop. The multiplexer is designed using NMOS transistor logic [7]. The block diagram and waveforms of TFF, SRFF, JKFF, are shown in fig.7, fig.8, fig.9, fig.10, fig.11, fig.12 respectively.

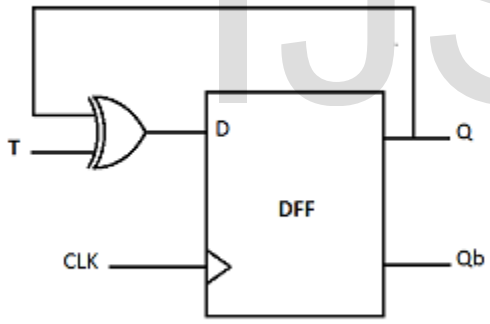

Fig.7 TFF Block Diagram

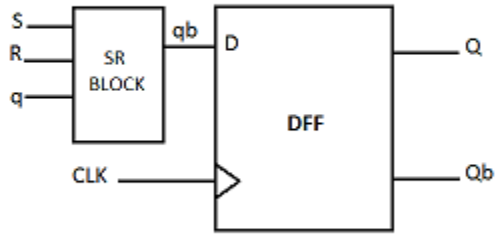

Fig.8 SRFF Block Diagram

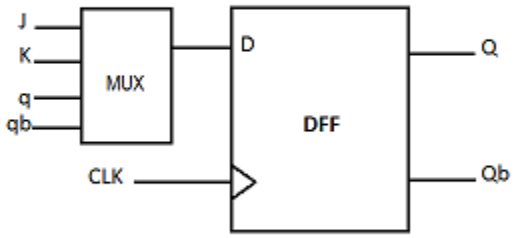

Fig.9 JKFF Block Diagram

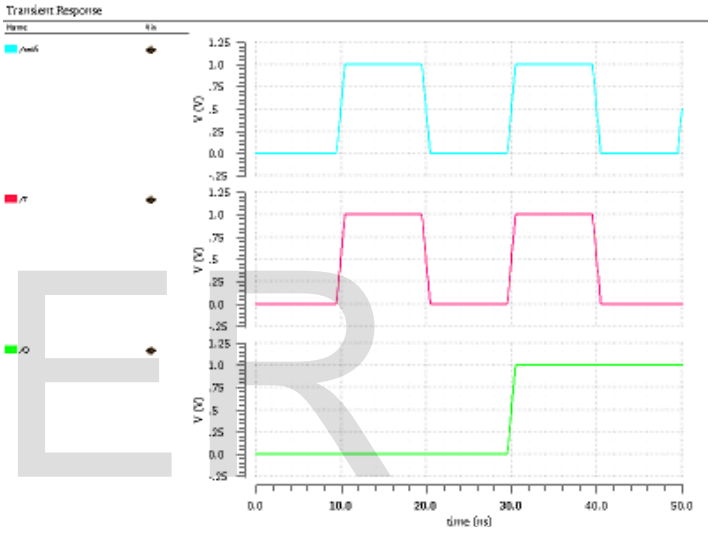

Fig.10 TFF Waveform

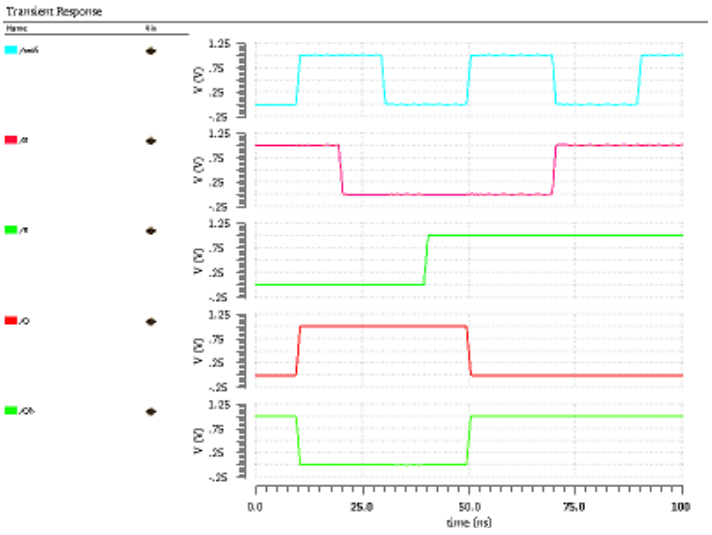

Fig.11 SRFF Waveform

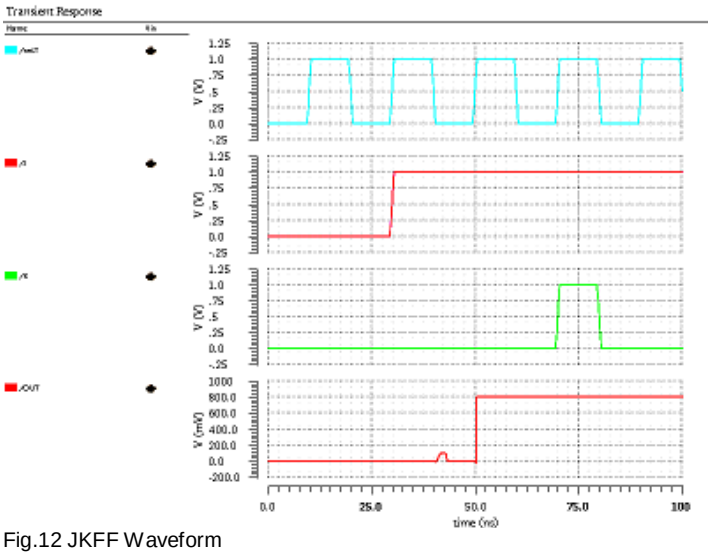

Fig.12 JKFF Waveform

3 Implementation Of SIPO Shift Register

A register is a group of flip flops. A FF stores 1-bit of data, here 4 FF's are used to make a SIPO shift register which can store 4-bits of data. SIPO shift register shifts the data into storage units and all the storage units are available as outputs. Similarly, it converts data from serial format to parallel format. If 4 data bits are shifted by 4 clock pulses via a single wire at data-in, the data becomes available concurrently on the 4 outputs, Q1 to Q4 after the 4th clock pulse. The practical application of the SIPO shift register is to convert data from serial form on a single wire to parallel form on multiple wires. The fig.13, illustrates 4-bit SIPO Shift Register Waveform.

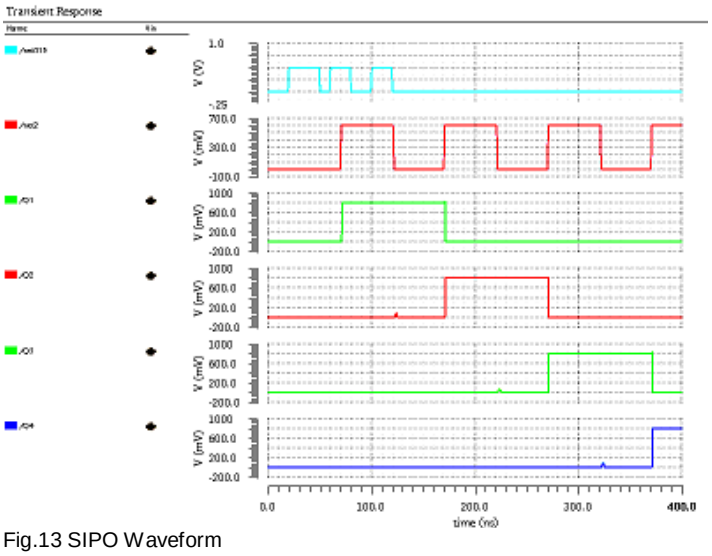

Fig.13 SIPO Waveform

4 Performance Simulation And Analysis

The simulations were carried out with 45nm (nanometer) technology in Cadence Virtuoso tool. The performance parameters of TCFF, TCFF with CPL logic style and Modified TCFF with high speed were compared and analysed. Same transistor size is given to each transistors used in the circuit design to simulate in same environment conditions. The output waveforms in fig.4, fig.5, fig.6, illustrates the Modified TCFF and TCFF with CPL style are having the same output as that of TCFF. The delay is decreased exceptionally in both modifications. The area barely remains the same and the power is marginally increased.

TABLE 1
POWER & DELAY COMPARISON

Flip Flop	TCFF	TCFF CPL	Modified TCFF
Power(nW)	28.97	29.23	29.77
Delay(ns)	49	3.094	0.990
Trans. Count	21	22	21
PDP(fJ)	1.41953	0.09043	0.02947

TABLE 2
POWER DELAY COMPARISON OF VARIOUS FF'S USING TCFF

Flip Flop	Power(nW)	Delay(ns)	PDP(fJ)
DFF	28.97	49.84	1.44386
TFF	46.89	46.31	2.1714
SRFF	35.67	49.26	1.7571
JKFF	41.15	46.70	1.9217

TABLE 3
POWER DELAY COMPARISON OF VARIOUS FF'S USING MODIFIED TCFF

Flip Flop	Power(nW)	Delay(ns)	PDP(fJ)
DFF	29.77	0.990	0.029470
TFF	56.54	0.532	0.030058
SRFF	44.25	0.821	0.036329
JKFF	48.17	0.596	0.028709

5 Conclusion

The paper introduces a new structure of TCFF, viz., Modified TCFF with a significant decrease in the delay compared to the original TCFF. TCFF outperforms any other FF's in most of all parameters. With this new method it achieves the high speed advantage as well. The area also is marginally same.
Therefore, it can be widely used for high speed applications with low power wastage.

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