Adaptive On-chip Ring Oscillator for FPGA based Systems

Adnan Ghafoor, Arbab Ali Khan

Abstract—A new topology of a high-speed adaptive oscillator for on-chip clock generation, especially suitable for FPGA based systems, has been proposed here. The oscillator generates more precise dual phase dual frequency. The simulation results show 30% improvement over conventional approaches in performance parameters for the new circuit architecture.The optimized simple circuit and more stable operation make this oscillator an excellent candidate for high-speed processing systems.The proposed design has the power to adjust itself automatically to its maximum performance in all working conditions.

Index Terms—Field Programmable Gate Arrays (FPGAs), ring oscillator, adaptive, delay skew, routing asymmetry

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1 INTRODUCTION

A chain of odd number inverters connected in a series, depicted in Fig. 1., where output of the last inverter is feedback as input of the first inverter, forms a ring that causes square-wave oscillations. These oscillations can be used as clock signal. The accumulative propagation delay of inverters along with wires (interconnects) separates input from its inversion at the output, this defines the time period of oscillations and hence the frequency of the clock. Increasing the number of inverters in series increases the overall feedback delay that results in reduced frequency. This also results in compromise on precision of the produced frequency and consumes more chip space. The unstable transitions, in addition, cause high power consumption and may result in device burn-out [1].
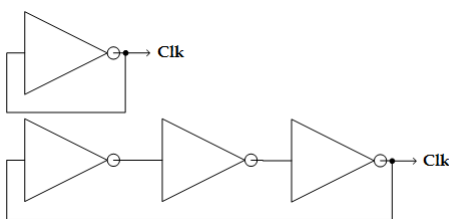

Fig. 1 Inverter based ring oscillators.

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2 SIGNIFICANCE OF ON-CHIP OSCILLATOR

On-chip ring oscillators and their properties have been widely used in a variety of applications like True Random Numbers Generators [2] and Temperature Measurements [3,4] etc., in addition to clock generation for digital systems.The output frequency of ring oscillators decreases linearly with increase in temperature. Similarly response of other semiconductor devices becomes much slower at higher temperature. The slope of the line equals 380 kHz/°C [4],depicted in Fig.2., which means with a rises of 65°C in temperature, the corresponding decrease in frequency is 24.7 MHz that results in a loss of millions of calculations per second. This means,a sequential circuit that uses fixed frequency clock has to work at a designatedclock frequency which is more than 24.7 MHz slower than the one at which hardware can perform at favorable temperature. Further, continual improvements in process technology have enabled IC designers to increase circuit density. According to International Technology Roadmap for Semiconductors (ITRS) [5], microprocessor power density has already reached 100 W/cm² for beyond 50nm technology nodes. This power density is sufficient to bake the crystal, to save the device from burning and to ensure reliable operation this heat has to be continually removed from the die. The increase in circuit density and associated exponential increase in power density results in even higher temperature changes that demand more precise frequency adjustments. To utilize the full potential of FPGA resources we, therefore, recommend that the hardware should utilize a self-adjusting clock.
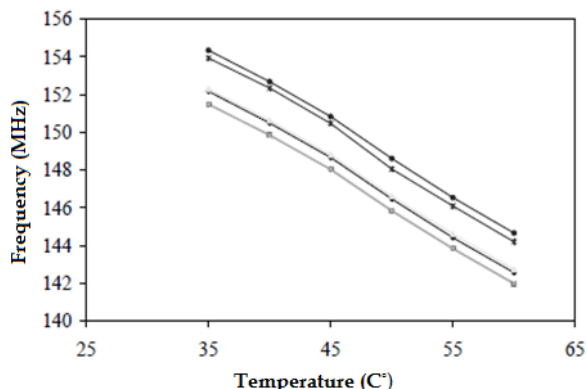
3 FPGA BASED RING OSCILLATOR

Fig.2 Variations of oscillator output frequency with temperature.

Field Programmable Gate Arrays (FPGAs) are used for implementing combinational and sequential circuits, both as test bed for new designs and as functional units for commercial usage. The functional units (building blocks) of FPGAs are logic elements (LEs) which can be connected as desired by the designers. A typical logic element, depicted in Fig. 3., contains a Lookup Table (LUT) and a D flip-flop (DFF).The output of LUT in a sequential logic goes through a DFF and in combinational logic the DFF is bypassed by a multiplexer. Selection between sequential and combinational data paths is made by a multiplexer; whose select line is adjusted by its configuration bit. The small delays associated with LUT and its' interconnects in a single inverter ring oscillator results in very high frequency oscillations. The clock generated, this way, is too fast and violates the setup and hold time conditions of sequential circuits, thus, cannot be used as clock.

In order to simplify the digital designs that saves chip space, increases speed and performance, the software used for the purpose utilize various optimizing tools.These software tools do not allow inverters in a series and remove the consecutive pairs, thus the chain of odd number
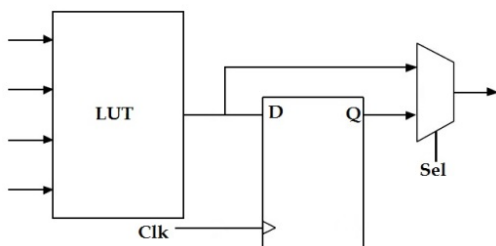
inverters is replaced by a single inverter. These optimizing tools, therefore, are disabled by (tool dependent) attributes like "keep" to preserves these chains of inverters on FPGAs, whereas the proposed oscillator design does not require all that.

4 PROPOSED OSCILLATOR AND ITS' WORKING

The uniform FPGA fabrication technology and thus physically identical DFFs have the same setup and hold times on a particular FPGA. An oscillator that generates clock by meeting setup and hold times of single DFF can, therefore, derive all the DFFs on that FPGA.

The proposed adaptive ring oscillator is depicted in Fig. 4. DFF-A is feed from its own inverted output, while DFF-B gets its input from the output of DFF-A. Outputs of both the DFFs are the inputs to XNOR and XOR gates thus their outputs are out of phase and toggle at twice the frequency than that of DFFs. The outputs of XNOR and XOR gates are feedback as clock signals to DFF-A and DFF-B respectively through AND gates. The AND gates have a non-masked Reset, when taken Low forces the clock to go Low and stops transitions of the circuit.

The input and output of DFF-B are compared by XOR gate, whose output to logic Low indicates that the DFF-B has completed its transition and the clock signal now can safely be disserted. At this point in time both the DFFs are in same logic state and a High clock signal from XNOR reaches DFF-A which will now start its transition that had already relaxed during the transition of DFF-B. Due to the same logic state of both the DFFs the output of XOR remains Low and thus DFF-B relaxes during the transition of DFF-A. As input of DFF-A is its own inverted output thus it will flip to the opposite state. When both the DFF are in opposite state
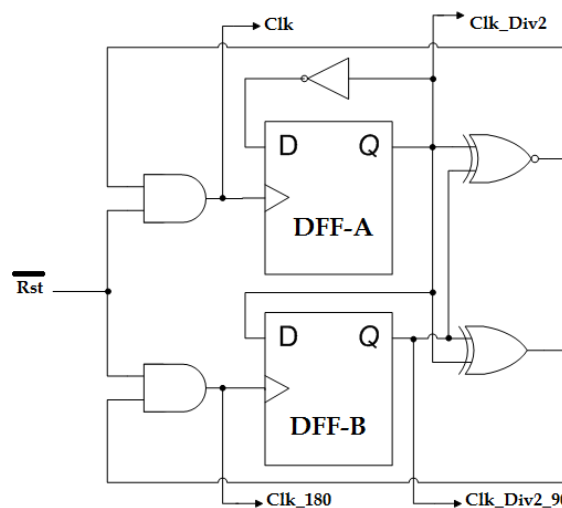

Fig. 4 Schematic of the proposed adaptive ring oscillator

Fig. 3 Schematic of a basic FPGA logic element.

the High output of XOR as clock reaches DFF-B and forces it to follow the state of DFF-A. At this point of time output of the XNOR remains Low thus DFF-A relaxes. This way as long as Reset signal remains High both DFFs keeps on toggling such that DFF-B follows as slave to its master DFF-A. This process generates clock that works at its' maximum frequency satisfying the setup and hold times requirements of the following sequential logic elements at varying conditions like temperature that badly degrades the performance. In other words the proposed design automatically adjusts to its higher performance in all favorable and unfavorable conditions.

This adaptive clock works with the same efficiency on different technologies of FPGAs, i.e., the topology is technology adaptive as well. The circuits with outside crystal oscillators have to limit their maximum clock frequency at the worst-case operating conditions which are much lower than maximum frequencies in favorable conditions. The new design, however, has the power to adjust itself automatically to its maximum performance in all conditions. The post layout simulation, describes clearly that the software nicely and neatly simulates the proposed design that works on 0.2 GHz frequency on xc2s300e-7fg456 FPGA board, shown in Fig. 5.

The output of the circuit can be drawn from any of the outputs of AND gates or outputs of either DFF, the clock frequency is half at the output of DFFs than at the output of AND gates as DFFs need two clock cycles to complete their cycle. The outputs of AND gates are 180 degrees and outputs of DFFs are 90 degrees out of phase amongst themselves as depicted in Fig. 6.

An 8-bit counter was designed and driven by the proposed oscillator and implemented in xc2s300e-7fg456. It was
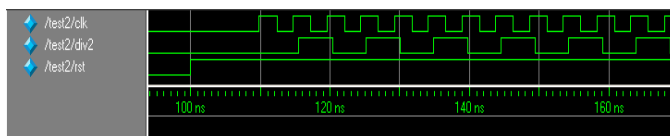

Fig. 5 Post layout simulation waveforms generated by xc2s300e-7fg456

observed that the proposed ring oscillator drives the counter without any violation of setup and hold times. The post layout simulations are depicted in Fig. 7.
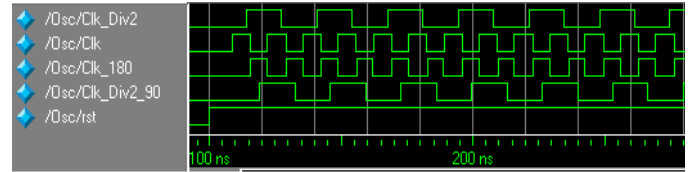

Fig. 6 Post layout simulation showing multi-phase and multi-frequency outputs of proposed ring oscillator.

When the proposed oscillator was implemented in two different FPGAs it produced different frequencies as evident form Fig. 5, 6 and 7, and shown in Table 1. The frequency varies upon technology migration, due to the change in the internal delays associated with the devices, is evidence that the proposed oscillator topology is technology adaptive.

The design proposed in this paper is found to be exactly the
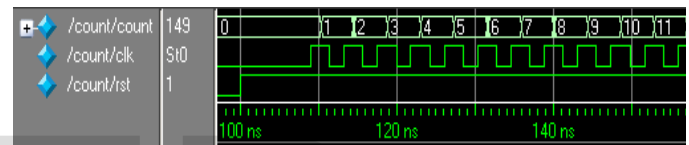

Fig. 7 Post layout simulation of 8-bit counter driven by the proposed ring oscillator

same after synthesis. This shows that our proposed design is highly optimized which cannot be influenced by optimizer. The technology schematic is depicted in Fig. 8. In the layout LUT3_60 contains the logic of XOR followed by AND gate and LUT3_90 contains the logic XNOR followed by its respective AND gate. Both FDCs (DFF with asynchronous reset) are DFF-A and DFF-B accordingly.

TABLE 1

COMPARISON OF TIME PERIODS FROM THE TWO FPGA TECHNOLOGIES

	Device	CLK (ns)	DIV2 (ns)
a	xc2s300e-7fg456	4.84	9.68
b	xc3s500e-5fg320	5.26	10.53

The comparison of proposed oscillator with conventional three inverter ring oscillator is given in Table 2. It was observed that the proposed hardware occupies less FPGA
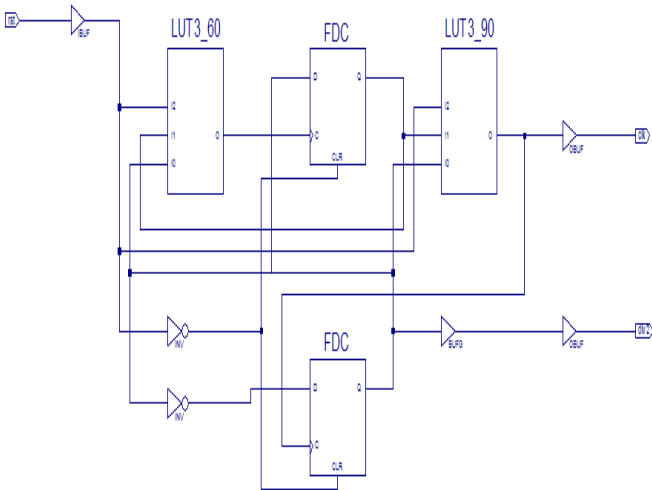

Fig. 8 Technology Schematic of proposed oscillator produced by the synthesis tool

resources than the chain of three inverters when implemented in various FPGAs. An ideal on-chip oscillator should produce maximum clock frequency while meeting setup and hold times requirements of DFFs. The inverters based oscillator works well by preserving the hierarchy but found to be slower in generation of clock frequency.

5 CONCLUSION

The proposed area and frequency optimized new topology of on-chip clock generation for FPGAs was synthesized on ISE8.1 and simulated using ModelSim XE 6.1. The oscillator proved to be adaptive with different technologies of FPGA. The proposed oscillator occupies 1 slice and is synthesized as exactly the same which shows that the design is optimized. The design is capable of producing dual phase and dual frequency clocks with precision adjusting the output frequency with variation in temperature.

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TABLE 2

COMPARISON OF PRODUCED FREQUENCIES AND CONSUMED CHIP AREA OF PROPOSED TOPOLOGY WITH THREE INVERTERS RING OSCILLATOR ON TWO FPGA TECHNOLOGIES

Devices	Generated Frequency GHz		Resource Utilization					
	Proposed Oscillator	Chain of 3 Inverters	Proposed Oscillator			Chain of 3 Inverters		
			No. of 4 input LUTs	Flip-Flops	Slices	No. of 4 input LUTs	Flip-Flops	Slices
XCV200E - 8FG456	0.211	0.175	2	2	1	3	0	2
XC2S400E- 7FG456	0.207	0.148	2	2	1	3	0	2