Router Architecture for Network on Chip Using FPGA

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Abstract: On Single chip integration of storage and computational block has becoming feasible due to continuous shrinkage of CMOS technology [1]. Field programmable gate arrays (FPGA's) are power efficient devices [3] support more complex design with good performance and low cost [6]. For effective global on-chip communication, on-chip routers provide essential routing functionality with low complexity and relatively high performance [1]. Routers implemented within FPGA can give better performance with reduced area and hence reduced power consumption [4]. This paper will provide an overview of related work for on-chip router architectures.

Keywords: First In First Out (FIFO) Buffer , Finite Sate Machine (FSM) ,NOC Router, Round-Robin Arbiter (RRA).

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1 INTRODUCTION

Extensive integration of logic resources on single chip introduces many difficult problems such as poor scaling of interconnect, increasing design complexity, increase power consumption [1]. Bus based communication architecture is standard solution for on chip communication, but it is no longer suitable for complex SOC design because of its limited scalability. It has limitation like wiring delay, noise power dissipation, signal reliability and synchronization [1]. Which make it poor choice for future system on chip. For this efficient routers are needed to communicate between these devices. Router is basic element of NoC with multiple connections to other router [1]. Router design consists of FIFO buffer to provide temporary storage of packets that are in transit [1]. Crossbar switch provide full connectivity between all available links [1]. Crossbar routes data from input channel to output channel depends on routing decision make by control logic [1]. High speed is achieved by allowing routing function to each input port, which gives high level of parallelism [1].

Typical NOC architecture consists of computational processing elements (PEs), Network interfaces (NIs) and routers [1].When packet sent from source PE to destination PE, packet forwarded on network depends on decision made by each router. Each router first received packet and store it in input buffer. Then control logic in router take routing decision and granted packet traverse through crossbar to next router and process repeats until packet arrives at its destination [4]. Crossbar is controlled by the switch arbiter module [1]. Buffers consume large power. It is better to transmit packet instead of storing them because more power consume in storing them as compared to transmission. Thus reduction in number and size of buffer increase system performance and reduces area and power consumption. Router implemented within field programmable gate array (FPGA) can give advantages of better performance and low cost [6].

2 SWITCHING TECHNIQUES

The role of a switch in a router is to connect the input port to the output port [1]. In most router designs, crossbar switch is used to provide full connectivity between all of the available links [1]. The switching technique defines how data flows through a switch in a router. There are two basic techniques of data switching: circuit switching and packet switching

2.1 Circuit Switching

In circuit switching, a fixed circuit is established between sender and receiver and direct connection is maintained as long as it is needed [9]. There is a high initial latency associated with direct circuit [9]. Moreover, links remain occupied even with the absence of data transmission. The major drawback of circuit switching is its limiting scalability [9]. Circuit switching technique uses time sharing to allocates a resource for specific connections in individual time slots. In different time slots the resource is used by different connections [3].

2.2 Packet Switching

On the other hand, transfers data by segmenting longer messages into smaller data packets, and forwarding these packets individually from the sender to the receiver possibly with different routes and delays for each packet [2]. Packet switching offers the potential for scalability [3]. Packets are composed of fields , each field carrying specific information [1].The first part is the header that contains the destination address. Second part is the payload portion in which user specify its contents and final is trailer indicate end of packet [2]. Packetization of data allow to use wide interconnects for on-chip networks ,thus increases the performance [3].

There are three basic types of packet switching schemes: store and forward (SAF), virtual-cut-through (VCT) and wormhole (WH) switching [3] .

Store and forward (SAF) switching transfer packet only when the receiving router has sufficient buffer space for entire packet, router in every hop must wait to receive the entire packet before forwarding header flit to the neighboring router [3]. Buffer size should at least equal to size of the packet [9], therefore SAF switching suffers from a larger latency compared with other switching techniques [9].

Virtual-cut-through (VCT) switching does not wait for a packet to be received completely before making routing decisions [3,9], it can forward the header flit before the next flit of the packet arrives [9]. It has advantage of low latency and less HOL blocking [9].

Wormhole(WH) switching reduces the buffer requirement [3][1] in each router by dividing packets into smaller segments called flits (flow control units) [1] and pipelining them through the network [2]. Buffer size should be at least equal to size of single flit [9]. In wormhole switching, header flit is immediately forwarded to the next hop before receiving next flit of packet [9]. It transferred the flits like a worm movement [9].

In WH switching due to packet header conflictions , flits of single packet are residing across different routers along routing path [3][9], thus block the packet and stop forward movement of packet and create head-of-line (HOL) blocking problem [9] and degrade performance. It has advantages of low latency and small buffer size [9].

3 ROUTING SCHEMES

The routing scheme for a network compute the routing decision for every router node to determine global path of the data transfer . R.Gindin, I. Cidon and I. Keidar have provided an overview of the routing schemes [5].

3.1 XY Routing

XY routing is popular deterministic routing scheme, which is simple and robust against deadlock [2]. When entire packet is arrive in FIFO Buffer, row coordinate of destination address in header flit(say R1) is compared with stored reference row coordinate (say R) to decide routing path along row. If R1 > R then the packet is forwarded to the East port of sender router. If R1 < R then the packet goes to West port of sender router. If R1 is equal to R then column coordinate of the destination Router (say C1) is compared with stored reference column coordinate (say C) to decide routing path along column. If C1 > C then the packet is forwarded to North port . If C1 < C the packet is forwarded to south port. When C1 equals C it indicates that the packet is at the destination router. In XY routing, a packet is routed along a row first, then routed along the appropriate column to the destination. This save area and reduced number of clock cycles required for requests. This helps in the implementation of light weight router with minimum area overheads and acceptable level of performance [4].

3.2 Weighted Toggle XY

Traditional routing algorithms like XY provide unbalanced capacity allocation hence not suitable for programmable chips [6]. To increase adaptively toggled-XYrouting have been proposed(TXY) that toggles between sending on XY or YX routes, TXY is not better solution for this if traffic are not symmetric [6]. For this adds weights according to design, resulting in weighted-ordered-toggle(WOT) that assigns XY or YX routes based on source-destination pairs [5]. This is efficient solutions for the FPGA routing problem[6]. Since in toggled-XY routing and weighted-ordered-toggle XY (WTXY), path of data flow is divided into two routes so they forwarded along random path therefore large re-order buffers are required [6].

4 ROUND-ROBIN ARBITER (RRA)

Round robin arbitration algorithm assign priorities dynamically. When packets from many inputs want to go out through same output channel at the same time , then to assign priorities to incoming inputs Round Robin Arbitration algorithm is used. In which priorities are assign in clockwise i.e. the request that was just served should have the lowest priority on the next round of arbitration. In this algorithm clock cycles are required only when service have to provided [4].

5 BUFFERING

Buffering is required in most on-chip routers to provide temporary storage of packets that are in transit [1]. Buffering is implemented mostly with FIFO memory [1][4]. Buffer size and the buffering scheme are the two main considerations.

There are various buffering schemes namely input, output and centralized buffering [3].

With respect to input buffering , there is possibilities of confliction of flits occurs, resulting in Head-of-Line blocking [3]. With output buffers, switching is performed before buffering so latency of packets is minimum [3]. In centralize buffering more channel shares common buffer, so it reduces buffer requirement and increases speed of performance.

6 CONCLUSION

The design scheme discuss in this paper provides router with reduced complexity and adequate clock frequency for typical operation. By using design technique discuss in the paper , it is possible to design Light weight parallel router architecture with a varying number of ports, routing algorithms, data width and buffer depths. Routers implemented within FPGA can give better performance with reduced area and hence reduced power consumption.

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