

R-2R Ladder D/A Converter Circuit Performance Optimization for Mixed-Signal VLSI Chips via Generalized Geometric Programming

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Abstract— In this paper the critical delay in R-2R Ladder digital to analog (D/A) converter circuits is minimized by uniform interconnect wire sizing via Generalized Geometric Programming approach. Elmore delay model is considered for calculating the delays associated with the circuits during low to high or high to low transitions of voltage sources. The wire sizing problem is formulated as a Generalized Geometric Programming problem in order to minimize the critical delay associated with the circuit. Assuming the critical delay corresponding to k-bit R-2R Ladder D/A converter circuit as objective function, the widths of the interconnect wire segments (optimization variables) are sized by solving the convex optimization problem. Numerical experiments show that critical delay associated with the R-2R Ladder D/A Converter Circuit can be significantly reduced while the interconnect wire segments are sized following the proposed approach. It is observed that the percentage of reduction in critical delay in sized-circuit decreases as the order of the circuit increases. Results show that 39.46 % reduction in critical delay can be achieved by wire sizing in 2-bit R-2R Ladder D/A converter circuit, while the same reduction is only 20.64 % in 16-bit R-2R Ladder D/A converter circuit.

Index Terms— Critical Delay; Digital to Analog Converter; Elmore Delay Model; Geometric Programming; Mixed-Signal VLSI; R-2R Ladder; Wire Sizing.

1 INTRODUCTION

SIZING of active and passive circuit components (e.g. transistors and interconnect wire segments) is an effective technique to achieve desirable circuit performance in analog and digital integrated circuit chips. Both the resistance and capacitance of a circuit component are functions of component size. Thus the delay of a circuit can be minimized by proper sizing of circuit components, since the delay associated with each circuit component can be modeled as a product of the resistance of the component and the capacitance of the sub circuit driven by the component [1]. Interconnect wire sizing problem refers to the problem of determining the width of wire segments at every point; objective is to reduce the delay associated with the circuit and there by improve the circuit performance. Several researches [2-7] have shown the wire sizing is an efficient technique to reduce the circuit delay.

Analog circuits are required to interface between the core digital system (most of the functionality in an integrated system is implemented in digital circuitry) and the outer world. Therefore to realize an integrated system on a single chip, the digital and analog circuits are combined together, although in an integrated system, the analog circuitry occupies a small physical area compared to the digital counterpart. Digital to analog (D/A) and analog to digital (A/D) conversion is thus an important section of the mixed-signal integrated circuits to realize the interface between digital and analog systems inside the chip. Therefore, to determine the overall performance of

the mixed-signal integrated circuits the performance of the A/D and D/A plays a very significant role. In the present paper, authors have made an attempt to size widths of the interconnect wire segments in k-bit R-2R Ladder D/A Converter to minimize the circuit delay and there by improve the performance. The wire sizing problem is modeled and solved as a convex optimization problem (Generalized Geometric Programming problem). Numerical experiments show that the solutions to the sequence of convex programs converge to the same wire sizes for widely varying initial guesses. Thus, it is strongly suggests that the approach is capable of determining the globally optimum solution to the problem.

2 GEOMETRIC PROGRAMMING PROBLEM

A geometric program (GP) is a non-linear optimization problem which has the following standard form [8],

$$\left. \begin{array}{l} \text{Minimize } f_0(x) \\ \text{Subject to } f_k(x) \leq 1, \quad k=1, 2, 3, \dots, m, \\ g_k(x) = 1, \quad k=1, 2, 3, \dots, p, \end{array} \right\} \quad (1)$$

Where the objective function $f_0(x)$ and each one of the inequality constraint function $f_k(x)$ are posynomials; Equality constraint functions $g_k(x)$ are monomials and x_k are the optimization variables ($x_k > 0$). The standard form of a posynomial function can be written as,

$$f(x) = \sum C_k \prod x_j^{\alpha_{kj}} \quad (2)$$

Where C_k 's are k positive coefficients and α_{kj} 's are positive or negative arbitrary real numbers. By taking the logarithmic transformation on the optimization variables, the posynomial function becomes,

$$f(z) = \sum_k C_k e^{\left(\prod_j \alpha_{kj} z_j \right)} \quad (3)$$

Where $z_j = \ln(x_j)$; It is very easy to show that $f(z)$ is a convex

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function of the transformed variables z_i 's. Thus the geometric programming problem becomes a convex programming problem, by taking the logarithmic transformation on the optimization variables [8]. The advantageous property of a convex programming is that any of its local minima is also a global minima.

Formulating various practical engineering analysis or design problems as GP is called GP modeling. GP modeling is successfully done on various fields of engineering, such as Electrical engineering [9], wireless communication [10], semiconductor devices [11] and circuits [12-13], heat sink design for sub-millimeter wave sources [14] etc. Wire sizing problem of k -bit R - $2R$ Ladder D/A Converter circuit can also be modeled as a geometric programming problem; the procedure is discussed in detail in the next section.

3 GP MODELING OF WIRE SIZING PROBLEM IN R-2R LADDER D/A CONVERTER CIRCUIT

In this section authors have modeled the problem of determining the widths $w_1, w_2, w_3, \dots, w_n$ of n interconnect wire segments in a R - $2R$ Ladder D/A Converter Circuit inside a mixed-signal integrated circuit chip. A simple π -model for each wire segment is shown in Fig. 1. The wire resistance and capacitances are given by,

$$R_i = \alpha \frac{l_i}{w_i} \quad \& \quad C_i = \beta l_i w_i \tag{4}$$

Where l_i and w_i are the length and width of the i^{th} wire segment respectively and α and β are positive constants depending on the physical properties of the material of the wire segments and the oxide layers respectively. To make the design and fabrication process easier, authors have considered fixed-length and uniform width wire segments. Thus, both wire segment resistance and capacitance are posynomial functions of the wire widths w_i ; w_i be our design variables.

A 4-bit R - $2R$ Ladder D/A Converter Circuit as shown in Fig. 2, is considered for demonstration. The interconnect wire segments are also shown in Fig. 2. The entire circuit becomes a resistor-capacitor (RC) tree by substituting the π -model for each of the wire segments (Fig. 1).

For an RC tree circuit, the Elmore delay δ_m to capacitor m is given by [1],

$$\delta_m = \sum_{i=1}^n \bar{C}_i \left(\sum R' \text{ s upstream from capacitors } m \text{ and } i \right) \tag{5}$$

The Elmore delay is a sum of products of \bar{C}_i and R_i 's, thus it is a posynomial function of the wire widths w_i . The critical delay of the circuit is the largest Elmore delay to any capacitor in the circuit:

$$\delta_c = \max \left\{ \delta_1, \delta_2, \dots, \delta_n \right\} \tag{6}$$

The Elmore delay to the load capacitance C_L , when the S_0 (LSB) switches from either low to high or high to low (keeping all other bits (S_3, S_2 & S_1) grounded) can be calculated from Fig. 3. Each branch of the RC tree circuit (Fig. 3) either has the associated wire resistance (R_i) or has circuit component resistance (R or $2R$). Each node has either one or several capacitances (capacitance contributed by the upstream and downstream wire segments). The resulting RC tree has resistances

and capacitances which are actually posynomial functions of the wire segment widths w_i . For the RC tree circuit shown is Fig. 3,

$$\left. \begin{aligned} \bar{C}_0 &= C_1, \quad \bar{C}_1 = C_1, \quad \bar{C}_2 = C_2, \\ \bar{C}_3 &= C_2 + C_3 + C_4, \\ \bar{C}_4 &= C_3, \quad \bar{C}_5 = C_4, \quad \bar{C}_6 = C_5, \\ \bar{C}_7 &= C_5 + C_6 + C_7, \\ \bar{C}_8 &= C_6, \quad \bar{C}_9 = C_7, \quad \bar{C}_{10} = C_8, \\ \bar{C}_{11} &= C_8 + C_9 + C_{10}, \\ \bar{C}_{12} &= C_9, \quad \bar{C}_{13} = C_{10}, \quad \bar{C}_{14} = C_{11}, \\ \bar{C}_{15} &= C_{11} + C_{12} + C_{13}, \\ \bar{C}_{16} &= C_{13}, \\ \bar{C}_L &= C_{13} + C_L \end{aligned} \right\} \tag{7}$$

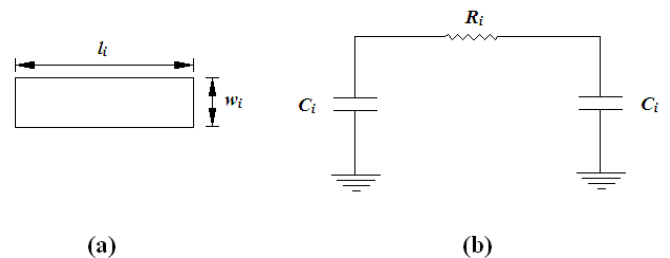


Fig. 1. (a) Interconnect wire segment with length l_i and width w_i , (b) RC π -model of the interconnect wire segment.

The Elmore delay to (leaf) capacitor \bar{C}_L for voltage switch at S_0 and keeping $S_1 = S_2 = S_3 = 0$, in the RC tree given by δ_{L0} can be calculated very easily from equation (5). Similarly the Elmore delays δ_{L1}, δ_{L2} & δ_{L3} to \bar{C}_L , when $S_1 \rightarrow$ voltage switch and $S_0 = S_2 = S_3 = 0$, $S_2 \rightarrow$ voltage switch and $S_0 = S_1 = S_3 = 0$ and $S_3 \rightarrow$ voltage switch and $S_0 = S_1 = S_2 = 0$ respectively can be determined from equation (5). Therefore, the critical delay to \bar{C}_L is the largest of the $\delta_{L0}, \delta_{L1}, \delta_{L2}$ & δ_{L3} , i.e.,

$$\delta_c = \max \left\{ \delta_{L0}, \delta_{L1}, \delta_{L2}, \delta_{L3} \right\} \tag{8}$$

Obviously the critical delay δ_c is a generalized posynomial of the wire widths w_i , because δ_c is a maximum of a set of posynomials.

Now the wire sizing problem for 4-bit R - $2R$ Ladder D/A converter can be formulated as the constrained optimization problem as,

$$\left. \begin{aligned} \text{Minimize} \quad & \delta_c \\ \text{Subject to} \quad & w_i^{\min} \leq w_i \leq w_i^{\max}, \quad i=1, 2, 3, \dots, n, \\ & \sum_{i=1}^n l_i w_i \leq A^{\max}, \end{aligned} \right\} \tag{9}$$

With variables w_1, w_2, \dots, w_n , where w_i^{\min} & w_i^{\max} are the lower and upper bounds on the wire widths w_i ; and A^{\max} is the limit on the total wire area. This is clearly a Generalized Geometric Programming (GGP) problem.

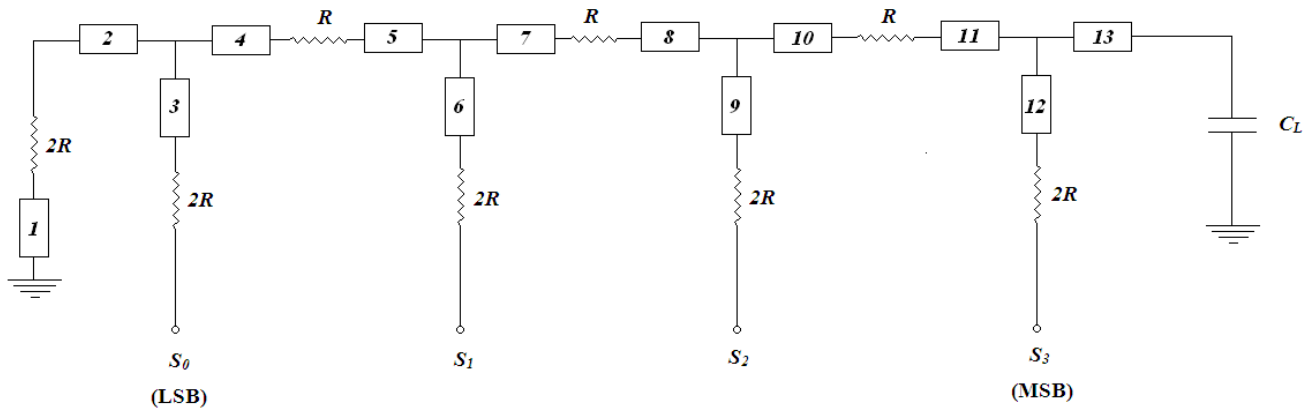


Fig. 2. 4-bit R-2R Ladder D/A Converter Circuit with load capacitance C_L , showing different interconnect wire segments.

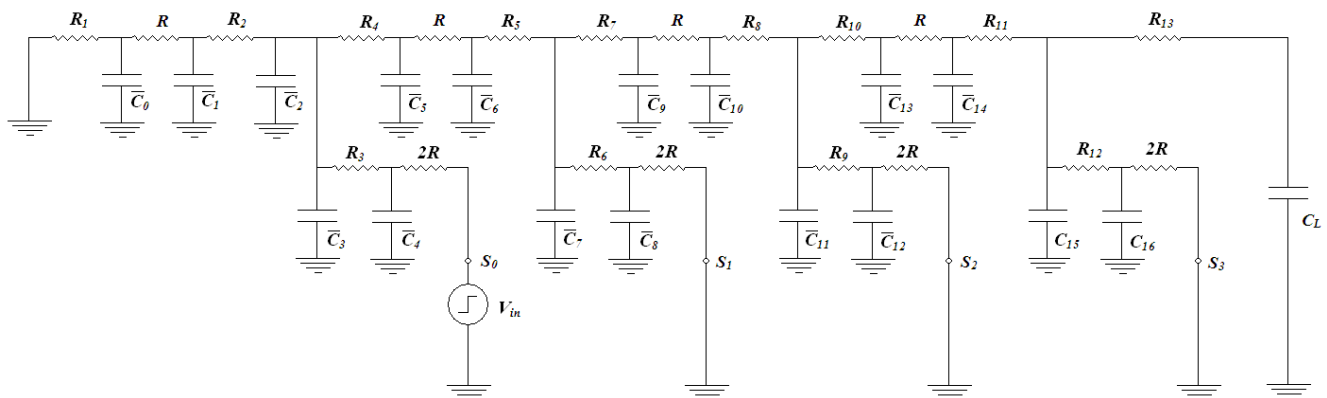


Fig. 3. RC tree model of the 4-bit R-2R Ladder D/A converter circuit in Figure 3 using the π -model of the interconnect wire segment.

4 EXPERIMENTAL RESULTS

Numerical experiment is carried out to solve the wire sizing problem formulated as GGP problem described in equation (10) to minimize the critical delay δ_c of the 4-bit R-2R Ladder D/A Converter Circuit. The GGP problem is implemented in MATLAB [15]; using *cvx-solver* tool [16] in MATLAB software, it is solved to obtain optimal wire sizes for which the critical delay associated with circuit is minimum. The experimental results are summarized in Table 1. From Table 1 it can be observed that critical delay δ_c associated with the 4-bit R-2R ladder D/A converter circuit can be reduced by 26.59 % by sizing the interconnect wire widths using GGP approach. Further circuit is tested for different initial guesses of unsized wires widths at the starting point. But for all those cases the solution converges to the same final wire sizes, which strongly establishes the globally optimal solution of the problem. Here the lower and upper bounds of the wire widths are taken as $w_i^{min} = 0.300 \mu m$ and $w_i^{max} = 0.500 \mu m$ and the upper limit of the total wire area is taken as $A^{max} = 30 \times 10^{-12} m^2$. The passive resistance of the circuit is taken as $R = 100 \Omega$ ($2R = 200 \Omega$) and the load capacitance is taken a $C_L = 1.0 pF$.

The same approach is used to minimized the critical delay in k -bit R-2R ladder D/A converters (where $k = 2, 4, 6, 8, 10,$

$12, 14, 16$) to investigate the performance of this approach under increased complexity of the circuit, thus under the increased number of optimization variables. Fig. 4 shows the variations of CPU time (time require for CPU to size the circuit), number of interconnect wires (n) against number of bits ($k = \text{order of the circuit}$) in R-2R ladder D/A converter circuit. It can be observed from Fig. 4 that, both CPU time and number of interconnect wires increases almost linearly with number of bits (k) in R-2R ladder D/A converter circuit. Fig. 5 shows the variation of critical delay of both sized and unsized R-2R ladder D/A converter circuits against order of the circuit (k). Fig. 6 also shows the variation of percentage of reduction in critical delay of the R-2R ladder D/A converter circuit due to sizing against k . It is interesting to observe from Fig. 5 and Table 2 that, the percentage of reduction in critical delay (i.e. $\Delta \delta_c / \delta_c$ (Unsized) (%), where $\Delta \delta_c = \delta_c$ (Unsized) - δ_c (Sized)) and thereby improvement of the level of circuit performance is significant in lower order D/A converter circuits due sizing via GGP approach. But this level of improvement due to sizing decreases as the order of the circuit (k), i. e. the complexity of the circuit increases. For example, reduction of critical delay is 39.46 % for 2-bit R-2R ladder D/A converter, while the same reduction is much lesser, only 20.64 % for 16-bit R-2R ladder D/A converter.

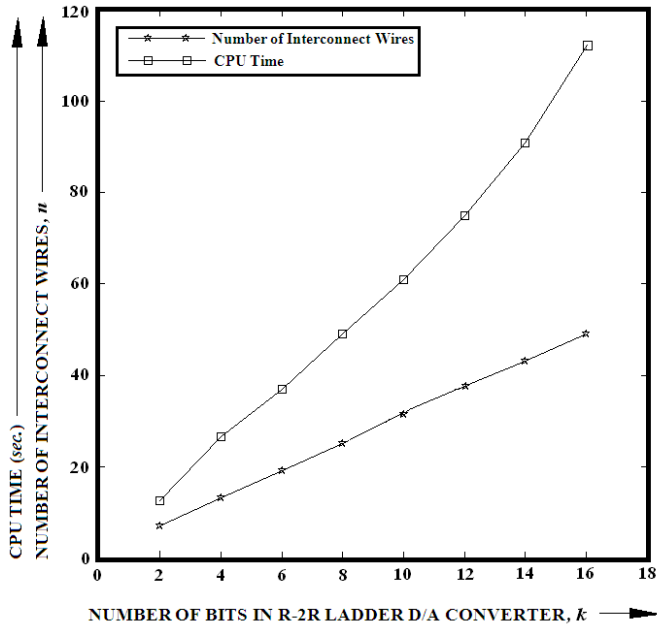


Fig. 4. CPU time and Number of Interconnect Wires versus Number of Bits in R-2R Ladder D/A Converter plots.

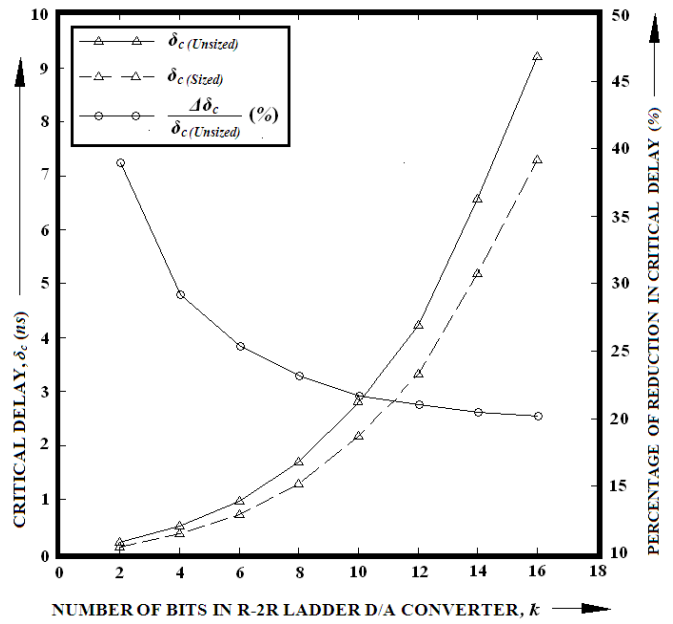


Fig. 5. Critical Delay and Percentage of Reduction in Critical Delay due to sizing versus Number of Bits in R-2R Ladder D/A Converter plots.

Table 1: Results of 4-bit R-2R Ladder D/A Converter Circuit.
 (Hardware environment: Intel® Core™ 2 Duo Processor T5750, 2 GB DDR2 RAM,
 Software environment: Microsoft Windows XP, SP-2)

Circuit	Interconnect wire number, i	l_i (μm)	Unsize			Sized			
			w_i (μm)	A (μm^2)	δ_c (Unsize) (ns)	w_i (μm)	A (μm^2)	δ_c (Sized) (ns)	CPU (sec.)
4-bit R-2R Ladder D/A Converter	1	5	0.4000	25.9999	0.5069	0.3015	27.2568	0.3563	26.59
	2	5	0.4000						
	3	5	0.4000						
	4	5	0.4000						
	5	5	0.4000						
	6	5	0.4000						
	7	5	0.4000						
	8	5	0.4000						
	9	5	0.4000						
	10	5	0.4000						
	11	5	0.4000						
	12	5	0.4000						
	13	5	0.4000						

Table 2: Results of k -bit R-2R Ladder D/A Converter Circuits ($k = 2, 4, 6, 8, 10, 12, 14, 16$).
 (Hardware environment: Intel® Core™ 2 Duo Processor T5750, 2 GB DDR2 RAM,
 Software environment: Microsoft Windows XP, SP-2)

Number of Bits in R-2R Ladder D/A Converter, k	Number of Interconnect Wires, n	Unsize	Sized		Percentage of Reduction in Critical Delay, $\Delta\delta_c / \delta_c$ (Unsize) (%)
		δ_c (Unsize) (ns)	δ_c (Sized) (ns)	CPU (sec.)	
2	7	0.2002	0.1212	12.43	39.46
4	13	0.5069	0.3563	26.59	29.71
6	19	0.9678	0.7178	37.16	25.83
8	25	1.6890	1.2890	49.05	23.68
10	31	2.7988	2.1788	61.19	22.15
12	37	4.2350	3.3235	75.91	21.52
14	43	6.5611	5.1861	91.13	20.96
16	49	9.2034	7.3034	112.44	20.64

5 CONCLUSION

In this paper, the wire sizing problem is formulated and solved to minimize the critical delay in R - $2R$ D/A converter circuits via Generalized Geometric Programming approach. Numerical experiments ensure that critical circuit delays associated with those circuits can be significantly reduced by sizing the widths of the interconnect wire segments using GGP. This sizing approach can be further extended to size different active (transistors) and passive components simultaneously in analog VLSI circuits, which might be extremely useful for realization of improved performance mixed-signal VLSI chips.

ACKNOWLEDGMENT

Aritra Acharyya would like to thank Dr. Pradip Mandal, Associate Professor, E & ECE Dept., IIT Kharagpur, India and Mr. Samiran Dam, Ph. D. student, E & ECE Dept., IIT Kharagpur, India for sharing their insights into geometric programming based device and circuit sizing problems in analog VLSI.

REFERENCES

- [1] W. C. Elmore, "The transient response of damped linear networks with particular regard to wide-band amplifiers", *J. Applied Physics*, vol. 19, no. 1, pp. 55-63, 1948.
- [2] J. Chong, K. S. Leung & D. Zhou, "Performance-driven interconnect designed based on distributed Remodel", in *Proceedings of the ACM/IEEE Design Automation Conference*, pp. 606-611, 1993.
- [3] J. Chong & K. S. Leung, "Optimal wire sizing under the distributed Elmore delay model", in *Proceedings of the IEEE International Conference on Computer-Aided Design*, pp. 634-639, 1993.
- [4] S. S. Sapatnekar, "RC interconnect optimization under Elmore delay model", *Tech. Rep. ISU-CPRE-94-SS03*, Iowa state university, Ames, IA, 1994.
- [5] C. P. Chen, C. C. N. Chu & D. F Wong, "Fast and exact simultaneous gate and wire sizing by Lagrangian relaxation", *IEEE Trans. Computer-aided design*, vol. 18, no. 7, pp. 1014-1025, 1999.
- [6] C. P. Chen, Y. W Chung and D. F Wong, "Fast performance-driven optimization for buffered clock trees based on Lagrangian relaxation", in *Proceeding of ACM/IEEE Design Automation Conf.*, pp. 405-408, 1996.
- [7] C. P. Chen, H. Zhou & D. F Wong, "Optimal Nonuniform wire sizing under the Elmore delay model", in *Proceedings of IEEE international Conf. on Computer-Aided design*, pp. 38-43, 1996.
- [8] S. Boyd, S. J. Kim, L. Vandanberghe & A. Hassibi, "A Tutorial on Geometric Programming", Springer Science + Business Media, LLC 2007.
- [9] R. A. Jabr, "Application of geometric programming to transformer design", *IEEE Trans. on Magnetics*, vol. 41, issue 11, pp. 4261-4269, 2005.
- [10] S. Kandukuri and S. Boyd, "Optimal power control in interface limited fading wireless channels with outage-probability specifications", *IEEE Trans, on Wireless Communication*, vol. 1, no. 1, pp. 46-55, 2002.
- [11] S. Joshi, S. Boyd and R. W. Dutlon, "Optimal Doping profiles via Geometric Programming", *IEEE Trans. on Electron Devices*, vol. 52, no. 12, pp. 2660-2675, 2005.
- [12] P. Mandal and V. Viswanathan, "CMOS op-amp sizing using a Geometric Programming Formulation", *IEEE Trans. on Computer-*

- aided design of Integrated Circuits and Systems, vol. 20, no. 1, pp. 22-38, 2001.
- [13] Maria Del Mar Herhenson, "CMOS analog circuit design via Geometric Programming", in *Proceedings of the American Control Conference*, Boston, Massachusetts, 2004.
- [14] A. Acharyya, A. Khandelwal and J. P. Banerjee, "Optimal Heat Sink Design for Terahertz IMPATT source via Geometric Programming", in *Proceedings of E2NC*, Mankundu, Hooghly, W.B., India, 2012.
- [15] A. Grace, "Optimization Toolbar User's Guide", The Math Works Inc., 1992.
- [16] S. Boyd and M. Grant, "cvx Users Guide for cvx Version 1.21", 2010.