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Low Cost Design of Sequential Reversible Counters

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Abstract - Reversible computing has attracted the attention of researchers due to its low power consumption and less heat dissipation. A number of reversible gates have been proposed by different researchers and various combinational circuits based on reversible gates have been proposed. Sequential circuits were not available because of feedback was not allowed in reversible circuit. However allowing feedback in space (not in time), some sequential reversible gates and circuits have been reported in the literature.
In this work, we propose a novel reversible gate and low cost T flip-flop by using our proposed gate. The proposed gate has significant improvement over earlier design in terms of garbage outputs, constant inputs and number of reversible gates. The design of efficient asynchronous and synchronous reversible counters has also been proposed. We hope this work will strengthen the development in the field of reversible sequential circuit.

Index Terms - Low-power VLSI, Reversible logic, Reversible counters, Reversible flip-flop, Sequential circuits

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1 INTRODUCTION

WITH increasing complexity of digital circuits, the heat dissipation is becoming a major issue to continue growth momentum. In early 1960's R. Landauer [1] showed that reversible hardware computation results in energy dissipation because of information loss. It has been proved that each bit of lost information will lead to dissipation of at least KTln2 joule of energy, where K=1.3806505 x 10^{-23} $m^2kg^{-2}K^{-1}$ is the Boltzmann's constant and T is the absolute temperature at which computation is performed [2],[4].

It is well known that irreversible gate erase at least one bit of information in every operation. Hence these gates will always produce some heat energy. C.H. Bennet [3], [4] proved that KTln2 joule of energy would not be dissipated if the computation is carried out by a reversible gates. The applications of reversible logic are quantum computation, optical computing, ultra low power CMOS design, DNA computing and nanotechnology etc.

In 1980, Toffoli [5] has proposed a well known Toffoli Gate and other reversible gates followed by Fredkin Gate [7] in year 1982 that has begun an era of reversible computing. Since then the development of reversible circuits is growing as an alternative of conventional irreversible computing.

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In reversible circuits feedback & fan-out are not allowed [8] and number of inputs and outputs must be equal. Like irreversible computing, the work is in progress of reversible computing for development of various circuits representation formats, hardware description languages, circuit synthesis and optimization algorithms, fault tolerance and design of sequential circuits etc.

Reversible circuit representation format like Reed-Muller expansion, PPRM etc. explained by Mehdi Saeedi and Igor L. Markov [9]. Syrec language for reversible hardware description was proposed by Robert Wille et al. [10]. Circuit synthesis and optimization algorithms such as Transformation-based methods [11], Search-based methods [12], Cycle-based methods [13] and BDD [14] were proposed by different researchers. In order to incorporate fault tolerance in reversible circuits a number of fault tolerant techniques and synthesis have been reported [15]. Anugrah Jain et al. [16] have exploited the parity preserving fault tolerance characteristics of PPTG Gate in year 2013.

Due to limitation of feedback and fan-out in reversible computing, the development of sequential circuits has not been significant. Recently, A. Banerjee et al. [17] have redefined that feedback in space is allowed but not in time. Hence, the development of reversible sequential circuits has begun.

In year 2005, H. Thapiyal et al. [18] have constructed T flip-flop using basic reversible gates. SKS Hari et al. [19] have improved this design of reversible T flip-flop in year 2006. In 2008, Min-Lun Chuang et al. [21] have reported T flip-flop by using D and T latches, which an improvement design over the one proposed by H. Thapiyal [18]. In year 2010, Sayem Gate was proposed by Abu Sadat, Md. Sayem [22] and D, J-K latches were designed using Sayem Gate and basic reversible gates. In 2011, V. Rajmohan et al. [23] have proposed T flip-flop using Sayem Gate and basic reversible gates. In this work, we are proposing a new

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reversible gate which will be used in the construction of T flip-flop.

This paper proposes a novel concept on efficient and optimized reversible sequential circuit design of asynchronous and synchronous counters.

The next sections of this paper are as follows. Section 2 explains the basic definition of reversible logic gates and necessary reversible gates used in this work. Section 3 provides the related work in the past. Section 4 provides the details about the proposed reversible gate and T flip-flop. Section 5 provides the conventional asynchronous circuit design and its reversible design. The conventional synchronous circuit design and its reversible design have been described in section 6. Section 7 concludes the work.

2 BASIC DEFINITIONS OF REVERSIBLE LOGIC GATES

2.1 Definition 1. Reversible Gate is a circuit in which the number of outputs is equal to the number of inputs and there is a one to one correspondence between the input and output vectors [24].

Example. Let the input vector be I_V, output vector be O_V and they are defined as follows, IV = (I_i, I_{i+1}, I_{i+2} .... I_{k-1}, I_k,) and O_V = (O_i, O_{i+1}, O_{i+2} .... O_{k-1}, O_k). For each particular i, there exits the relationship $I_V \leftrightarrow O_V$.

Conventional logic gates are almost all irreversible. Among the commonly used gates, only the NOT gate is reversible. The AND gate is irreversible because it violate the requirements of reversible functions as shown in Fig. 1. One way to make the AND function reversible is to add one input and two outputs as shown in Fig. 2(a). The AND function can be obtained in the third output column AB⊕C of Fig. 2(b), when setting C = 0[5].

A	B	P=(A.B)
0	0	0
0	1	0
1	0	0
1	1	1

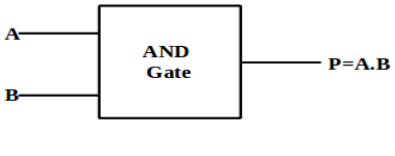

Fig.1. 2-bit AND gate (a) Truth Table; (b) Block Diagram

2.2 Definition 2. Unwanted or unused output of a reversible gate (or circuit) is known as Garbage Output.

In the reversible AND function shown in Fig. 2(a), the outputs A and B are garbage outputs which are used to make the function reversible. A set of reversible gates is needed to synthesize reversible circuits.
By using both the definitions, we can conclude that it is possible to obtain reversible logic gates and circuits from conventional irreversible gates.

A	B	C	A	B	AB⊕C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

(a)

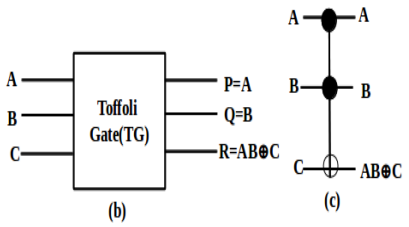

Fig.2. 3-bit Toffoli gate (a) Truth Table; (b) Block Diagram; (c) Symbol

Several reversible gates have been proposed in the past. Here we introduce the Toffoli and Feynman gate, which will be used in our work.

Toffoli Gate. The truth table of a 3-bit Toffoli Gate (TG) is shown in Fig. 2(a), and its block diagram is shown in Fig. 2(b) [5]. The function of the third column is AB⊕C. That means when A = B = 1, the output is inverted C; otherwise the output is C. This gate can be used to realize a 2-input reversible AND function by setting C as a constant 0 as mentioned [5].

Feynman Gate. The truth table of a 2-bit Feynman gate is shown in Fig. 3(a), and its block diagram is shown in Fig. 3(b) [6]. Feynman Gate (FG) can be used as a copying gate. Since a

A	B	A	A⊕B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(a)

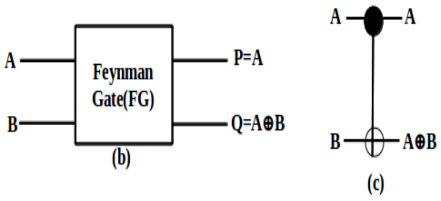

Fig.3. 2-bit Feynman gate (a) Truth Table; (b) Block Diagram ;(c) Symbol

fan-out is not allowed in reversible logic, this gate can be used for duplication of the input to two outputs.

Two restrictions on reversible logic synthesis must be followed [5]:

i. The fan-out count of a signal net must equal one. If two copies of one signal are needed, duplication is necessary.
ii. A combinational reversible network has to be loop-free. It cannot contain a cyclic path.

The first restriction is in place because a fan-out structure is not reversible. For fan-out, the input signal number is one, but there are two or more output signals. Therefore, for the first restriction, we use a 2-bit Feynman Gate to duplicate a signal.

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The truth table of a 2-bit Feynman Gate and its symbol are shown in Figure 3(a) and 3(c), respectively. The function of the second output column is A⊕B. If B is set as a constant 0, a copy of input variable A will be obtained at first output P=A as well as on second output Q= A⊕B = A⊕0=A. Hence this gate enables us to obtain fan-out like duplication of n input bit [21].

The second restriction is required because a reversible combinational function is necessarily a finite one-to-one function. It is customary to express this function in graphical form as a causality network. By construction, causality networks are "loop-free". Therefore, a combinational reversible network is loop-free [21].

These two restrictions have to be met in reversible sequential circuits as well. According to Toffoli [5], a sequential circuit is reversible if its transition function is constructed by reversible logic. The structure of transition function in Fig. 4 acts as a combinational network. Therefore, the synthesis of this transition function has to conform to the restrictions mentioned above.

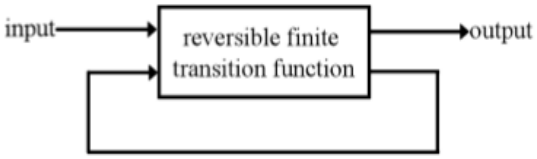

Fig.4. The structure of a Reversible Sequential Circuit

There are two objectives in the reversible circuit synthesis [21].

i. Minimize the number of gates. The number of gates gives a simple estimate of the implementation cost of a reversible circuit.
ii. Minimize the number of garbage outputs. Minimizing the number of garbage outputs leads to minimized area and power.

3 RELATED WORK

The following attempts have been made recently to design reversible T flip-flop and construct sequential circuits using them.

i. Min-Lun Chaung et al. have proposed new gates by allowing feedback for D & T latches in 2008 [21].These latches have been used D & T flip-flops. Both the flip-flops have 5 gates, 3 garbage outputs and 2 constant inputs.
ii. V. Rajmohan et al. [23] have proposed T flip-flop by two Sayem Gates and one Feynman Gate in 2011. Hence 3 gates, 3 garbage outputs and 2 constant inputs have been used in constructing T flip-flop.

We observed that the gate, garbage output and constant input counts can further be reduced and it is possible to construct a T flip-flop using only one gate proposed in this paper. Accordingly low cost asynchronous and synchronous counters can be designed using proposed T flip-flop.

4 PROPOSED REVERSIBLE GATE AND T FLIP-FLOP

The section describes our proposed gate name "SVS" gate and T flip-flop constructed using SVS gate.

4.1 PROPOSED REVERSIBLE SVS GATE

We propose a new 4*4 reversible SVS gate. The block diagram of the proposed gate is shown in Fig.5. Its corresponding truth table is shown in table I.

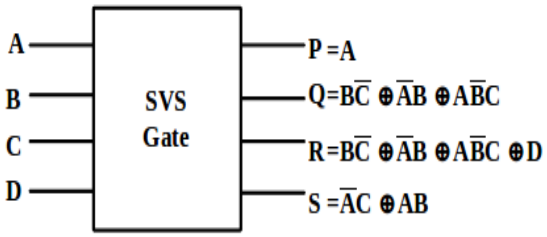

Fig.5. Proposed "SVS" Gate

Table I Truth Table of the Proposed Reversible Gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	0	1	1	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	1

4.2 PROPOSED REVERSIBLE POSITIVE EDGE TRIGGERED T-FLIPFLOP

A flip-flop is a bi-stable multivibrator. A flip-flop has only two

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stable states. In this section we propose the realization of T Flip-flop using our proposed reversible gate. The truth table of the T Flip- flop is given in Table II. The reversible design is shown in Fig. 6 and the corresponding block diagram is shown in Fig.7. The reversible realization of T Flip-flop has one constant input and it produces two garbage outputs. The comparison of the proposed design of T flip-flop with the existing designs is given in Table III based on three parameters namely number of gate counts, garbage outputs and constant inputs.

Table II Positive Edge Triggered T Flip-Flop

CLK	T	Q_{N-1}	Q
0	0	0	0
1	0	0	0
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	1
0	1	1	1
1	1	1	0

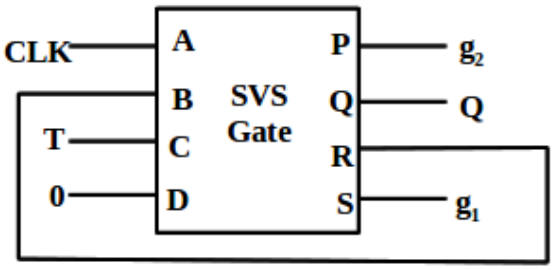

Fig.6. Reversible Positive Edge Triggered T Flip-Flop

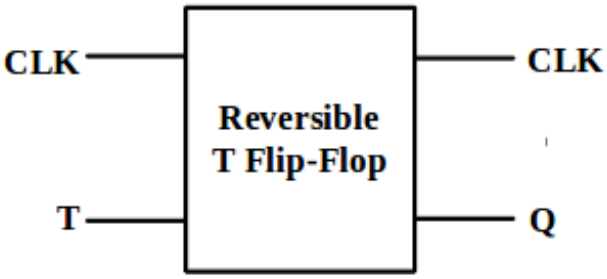

Fig.7. Block Diagram of Proposed T Flip-Flop

Table III Comparison of Different T Flip-Flops with Only Q Output

	No. of Gates	Garbage Outputs	Constant Inputs
Existing[18]	10	12	10
Existing[19]	5	3	2
Existing[20]	10	10	10
Existing[21]	5	3	2
Existing[23]	3	3	2
Proposed Design	**1**	**2**	**1**
Improvement Factor w.r.t[18]	10	6	10
Improvement Factor w.r.t[19]	5	1.5	2
Improvement Factor w.r.t[20]	10	5	10
Improvement Factor w.r.t[21]	5	1.5	2
Improvement Factor w.r.t[23]	3	1.5	2

5 DESIGN OF ASYNCHRONOUS REVERSIBLE COUNTERS

A counter, by function, is a sequential circuit consisting a set of flip-flops connected in a suitable manner to count the sequence of the input pulses presented to it in digital form. In a asynchronous counters, the output transition of one flip-flop serves as a source for triggering other flip-flops.

5.1 Proposed 4-bit Asynchronous Up-Counter

The conventional circuit diagram of a 4-bit binary asynchronous up-counter is shown in Fig. 8 [25].

The reversible design of the 4-bit asynchronous UP-Counter is shown in Fig. 9. At the output of each reversible T Flip-flop, the Feynman Gate is used for the complemented Q output with the input B=1. These complemented Q outputs of each T Flip-flop trigger the subsequent T Flip-flops and the reversible design performs the Up-Counter operation. The comparison of the proposed design with the existing is shown in Table IV.

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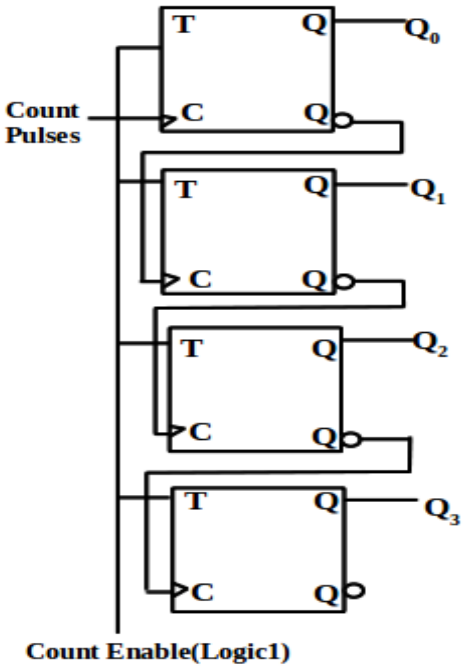

Fig.8. A Conventional 4-bit Asynchronous Up-Counter

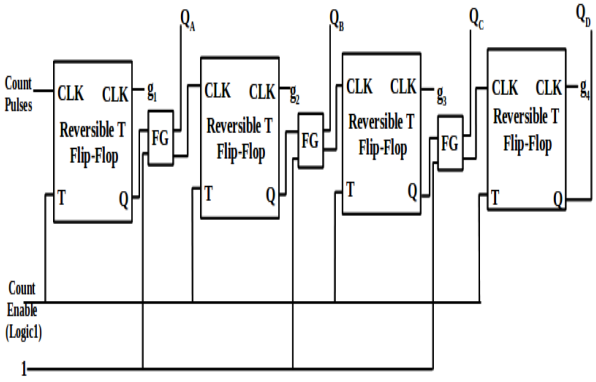

Fig.9. Proposed 4-bit Reversible Asynchronous Up-Counter

Table IV Comparison Between Existing and Proposed Reversible Asynchronous UP Counter Design

	No. of Gates	Garbage Outputs	Constant Inputs
Existing[23]	15	12	11
Proposed Design	7	8	7
Improvement Factor w.r.t[23]	2.14	1.5	1.57

5.2 Proposed 4-bit Asynchronous Down-Counter

The reversible design of the above 4-bit asynchronous Down-Counter is shown in Fig. 10. At the output of each reversible T Flip-flop, the Feynman Gate is used for fan-out of Q output with the input B=0. These Q outputs of each T Flip-flop trigger the subsequent T Flip-flops and the reversible design performs the Down-Counter operation. The comparison of the proposed design with the existing is shown in Table V.

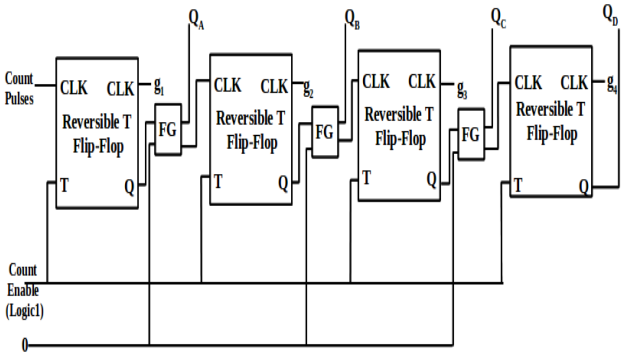

Fig.10. Proposed 4-bit Reversible Asynchronous Down-Counter

Table V Comparison Between Existing and Proposed Reversible Asynchronous Down Counter Design

	No. of Gates	Garbage Outputs	Constant Inputs
Existing[23]	15	12	11
Proposed Design	7	8	7
Improvement Factor w.r.t[23]	2.14	1.5	1.57

Similarly, the reversible design of the 4 -bit asynchronous Up/Down counter can be proposed by reversible T flip-flop.

6 DESIGN OF SYNCHRONOUS REVERSIBLE COUNTERS

The asynchronous counters above are simple but not very fast. If a counter with a larger number of bits is constructed in this manner, then the delays caused by the cascaded clocking scheme may become too long to meet the desired performance requirements. We can build a faster counter by clocking all flip-flops at the same time as presented below. Synchronous counters have regular pattern and can be constructed using flip-flops and gates.

6.1 Proposed 4-bit Synchronous Up-Counter

A conventional 4-bit Up Synchronous Counter can be realized as shown in Fig.11 [26]. In Fig. 11, instead of using AND gates of

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increased size for each stage, we use a factored arrangement. This arrangement does not slow down the response of the counter, because all flip-flops change their states after a propagation delay from the positive edge of the clock .Note that a change in the value of Q_0 may have to propagate through several AND gates to reach the flip-flops in the higher stages of the counter, which requires a certain amount of time [26]. This time must not exceed the clock period. Actually, it must be less than the clock period minus the setup time of the flip-flops.

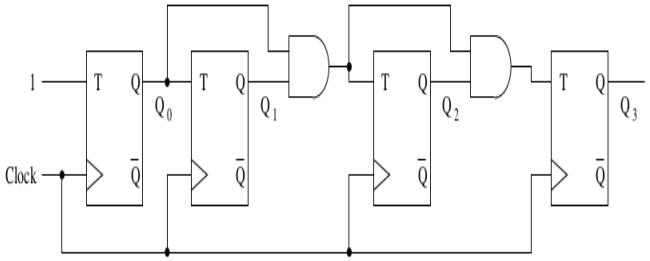

Fig.11. A Conventional 4–bit Synchronous Up–Counter

The reversible design of the 4-bit Synchronous UP-Counter is shown in Fig. 12. The Toffoli gate is used to realize the AND function. Feynman Gate is used for the fan-out of Q output with the input B=0. The comparison of the proposed design with the existing is shown in Table VI.

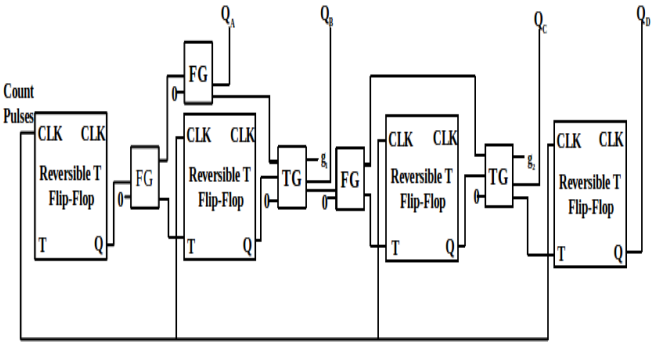

Fig.12. Proposed 4-bit Reversible Synchronous UP Counter

Table VI Comparison Between Existing and Proposed Reversible Synchronous Up Counter Design

	No. of Gates	Garbage Outputs	Constant Inputs
Existing[23]	15	12	13
Proposed Design	9	10	9
Improvement Factor w.r.t[23]	1.66	1.2	1.44

Similarly, the reversible design of the 4 -bit synchronous down and Up/Down counter can be proposed by reversible T flip-flop.

7 CONCLUSION

In this work, we propose a novel reversible gate which has shown the significant improvement for realizing and optimizing T flip-flop. We also propose the designs of reversible asynchronous and synchronous counter using reversible T flip-flop, Feynman Gate and Toffoli Gate. The designs of the counters are compared with existing counter design for three parameters namely gate count, garbage output, constant inputs and found improvement by a factor of 1 to 3. The proposed asynchronous and synchronous counter designs have the applications in building reversible Jonshan counter, Ring Counter, ASM charts and reversible processor etc. This work will provide a new face in designing of large and complex reversible sequential circuits for quantum computers. The design can further be extended to develop efficient reversible counters and reversible sequential circuits as a further work.

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