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Current Mode Comparator Design for Biomedical Applications

Apurva Gupta and R. S. Gamad

Abstract— In this paper, a new current mode low power comparator design is presented. In analog to digital conversion process, comparator is an important device widely used in the converting signals from analog to digital. Design is specially concentrated for biomedical device applications. The circuit includes two cascaded CMOS inverter with one diode connected transistors and another transistor (M_1) used as a reference current. Due to this changing design has reduced power dissipation, increase gain and speed. The circuit is simulated in a 0.18 µm CMOS technology with supply voltage 1.8 volt. Comparator was implemented for biomedical application in 0.18 µm technology with 1.8 volt supply. A primary advantage of building this design is the case of scaling with technology, and the power and area reduction. The total power is consumed 45.42 µW.

Index Terms— Analog to digital converter, biomedical application, Current mode, CMOS comparator, cadence, high gain, low power

1 INTRODUCTION

IN the communication process, analog to digital converter (ADC) is an important device. It is necessary to first sample the input. This sample signal is applied to the comparator for determining the digital equivalent output of the analog signal [1]. The information carried out by any electrical network is represented by nodal voltages and branch currents, former referred to "voltage domain circuits" whereas the latter are knows as a "current domain circuits" [2]. Due to increase market for portable equipment, for example, personal communication, computers and consumers, the interest toward low power and low voltage integrated circuit has grown. The voltage supply has gone down from 1.8 volt to 0.7 volt or less. Demand for low power consumption also has increased. These trends affect the fundamental limits architectures and innovative circuit design will be required. One possible solution is current mode [3]. Reducing the power consumption of the comparator benefits low power SAR ADC design and prolongs the device battery life in wearable biomedical electronics. The triode operation consumes large amount of current that is not suitable for ultra low power application [4]. A high-speed, low offset, low power consumption comparators are very important for many applications, such as memory sensing circuits, data receiver and ADC [5].

- *Apurva Gupta, Pursuing Master of Technology in Microelectronics and VLSI design in Electronics and Instrumentation Department from shri G. S. Institute of Science and Technology, Indore, India, MOBILE NO.-09826961836, E-mail: guptaapurva1607@gmail.com*
- *Dr. R. S. Gamad, Associate Professor in Electronics and Instrumentation Department in shri G. S. Institute of Science and Technology, Indore, India, MOBILE NO -09424584695. E-mail: rsgamad@gmail.com*

2 DETERMINATION SOME IMPORTANT PARAMETERS

Following parameters are given:

2.1 Power Dissipation

Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by [6]:

$$p = fCV_{dd}^2 \tag{1}$$

Where,

f = Output frequency.
C = Output capacitance.
V_{dd} = Power supply.

2.2 Sampling Frequency

The sampling frequency is defined as the reciprocal of the time T as [7]:

$$f_{sampling} = 1/T \tag{2}$$

The sampling frequency has to be equal or greater than twice of the frequency bandwidth of the analog signal.

2.3 Propagation Delay

The most important dynamic parameters that determine the speed of the comparator are the propagation delay and the settling time. If the propagation delay time is determine by the slew rate of the comparator, and then this time can be calculated as [8]:

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2SR} \tag{3}$$

Where,

ΔT = Propagation delay.
ΔV= Change of the output voltage of the comparator.
SR = Slew rate.
V_{OH}= Upper limit of the comparator.
V_{OL}= Lower limit of the comparator.

3 DESIGN OF A CURRENT MODE CMOS COMPARATOR

Current based comparators are basic blocks for non-linear current mode signal processing and ADC. In this paper the current comparator circuit utilizes two cascade inverter with one diode connected transistor PMOS (M_3) to limit the current and another transistor NMOS (M_1) used as a reference current. The advantage of this circuit in comparison with other circuits is lower power consumption and better accuracy [9]. The schematic view of the design is shown in figure 1. In this circuit the input current is integrated in the first inverter by gate source capacitor. The output voltage is dependent on difference of I_{in} and I_{ref}. The next inverter produces the logical level that uses in the register circuit.

The special attention was dedicated to make the comparator work in high speed and low power dissipation because it has been used in the current mode SAR ADC converter designs. Figure 1 shows the schematic view of the proposed current mode comparator.

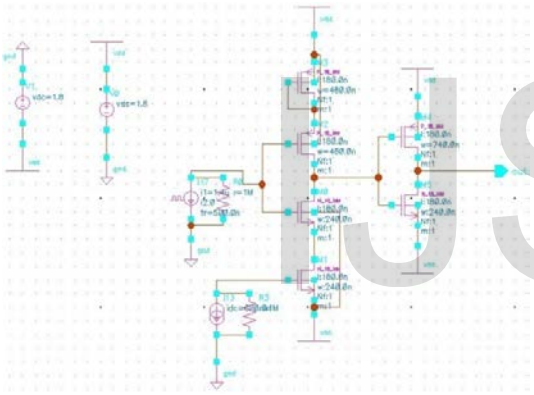

Fig.1. Schematic view of the current mode comparator

4 SIMULATION RESULTS

Simulation of the reported design is done by Cadence spectra in 0.18 µm CMOS technology with 1.8 V supply. Best simulation results are obtained and compare with earlier reported results as given in Table 1. It is observed that the performance parameters of this design are improved as compared to the earlier reported voltage mode comparator. This designed circuit is suitable for moderate speed, low power and better accuracy. The transient and DC transfer characteristics of this design is shown in figure 2 & 3. In addition authors have also determined some important parameters those are also useful for young researcher, designer and manufacturer as given in table-2.

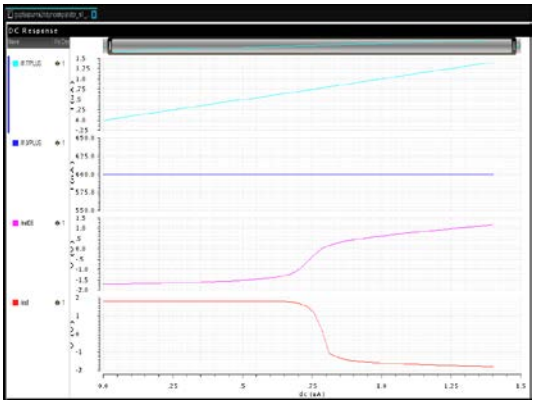

Fig.2. DC response

Fig.3. Transient response

In figure 3 – the input pulse i.e. i17 is compared with the reference current i.e. i13.

When i17 < i13 => out = i.e. 1.8 V

And i17 > i13 => out = i.e. -1.8 V is obtained.

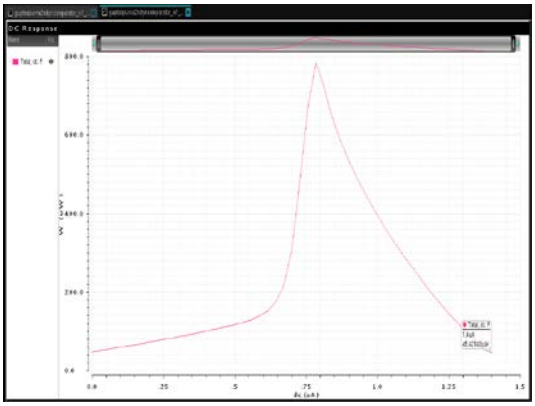

Fig.4.Total Power dissipation

TABLE 1
PERFORMANCE COMPARISON WITH EARLIER SIMILAR REPORTED WORKS

Parameters	Ref [5]	Ref [15]	Ref [16]	This work
Technology	0.18µm	0.18µm	0.18µm	0.18 µm
Power supply (V_{dd})	2 V	1.8 V	3 V	1.8 V
Mode	Voltage	Voltage	Current	Current
Power dissipation	0.27 m W	102 µW	2.3 m W	45.42 µW

TABLE 2
OTHER PARAMETERS WITH THIS WORK

Time period	Frequency	Propagation delay(t_p)	Output		Slew rate (V / µsec.)
			V_{OH}	V_{OL}	
40 μs	25 KHz	10.36 μs	1.8 v	-1.78 v	0.172
20 μs	50 KHz	5.38 μs	1.8 v	-1.78 v	0.332
10 μs	100 KHz	2.67 μs	1.8 v	-1.78 v	0.607

5 CONCLUSIONS

Present design is based on current mode CMOS comparator. This comparator is designed for Successive approximation ADCs applications. Simulation results are obtained with ±1.8 V power supply. Authors have achieved result on high sampling frequency of 100 KHz that is low power consumption about 45.42 µW as compare to earlier reported work. Presented results are compared and improvement is observed as shown in Table 1.

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