International Journal of Scientific & Engineering Research, Volume 5, Issue 6, June-2014
ISSN 2229-5518

Calculation of Performance Parameters and Reliability Aspects of Phase Shifted Semi Bridgeless Interleaved Boost Converter

V.Nithin vommi.nithin@gmail.com
Dr.R.Seyezhai seyezhair@ssn.edu.in
P.Siva Priya sivapriya.pitchuka@gmail.com
K.Vigneshwar vigneshwarkalaiazhagan@gmail.com
Department of Electrical and Electronics Engineering
S.S.N College of Engineering, Chennai, India

***Abstract*— Hybrid Electric Vehicles (HEVs) require a power modulator like an AC-DC converter at the charging end of the vehicle. The converter induces harmonics and distortion in the supply current due to the presence of nonlinear devices in its topology. This results in reduction of Power Factor (PF) and Efficiency. Hence, there is a need for implementation of a Power Factor Correction (PFC) circuit along with a rectifier to improve the performance of the charger. Among the various topologies mentioned in the literature, Bridgeless Interleaved and Phase Shifted Semi Bridgeless Interleaved PFC topologies are optimal solutions for the problem. This paper mainly focuses on the Performance Parameters and Reliability aspects of both the topologies operating in Continuous Conduction Mode (CCM). The Reliability aspects are based upon MILHDBK–217F standards. The topologies are simulated using MATLAB and the results are recorded. This paper is an effort to grade both the converters on the basis of reliability and other performance parameters.**

***Index Terms*— AC – DC Converters, Hybrid Electric Vehicles, PSIBC, Reliability, Power loss.**

I. Introduction

The main purpose of an AC - DC converter in the charging system of HEVs is to rectify the given AC supply and generate a constant DC supply. But the waveform is distorted due to the induced harmonics [1]. Thereby the power factor is also compromised. Therefore there is a need for a highly efficient converter which eliminates these drawbacks [2]. The topologies basically consist of a rectification part which converts the AC supply to a pulsating DC followed by a boost converter to enhance the output voltage. They are also provided with a bypass capacitor to filter the output ripple. Bridgeless Interleaved PFC and Phase Shifted Semi-Bridgeless Interleaved Boost PFC topologies are proposed for improving the performance of the charger in HEVs [3, 4].

In Bridgeless Interleaved (BLIL) boost topology, the diode bridge rectifier is eliminated so that the diode bridge losses [5], which are very significant at higher power levels, are minimized and thus higher efficiency is achieved. By employing the interleaving technique in the topology, effective ripple cancellation can also be achieved [6]. As a result, the Total Harmonic Distortion (THD) is reduced in this topology [7].

In Phase Shifted Semi-Bridgeless Interleaved Boost Converter (PSIBC) [8], four slow diodes are added to the bridgeless configuration to link the ground of the circuit to the input line. It employs the phase shifting technique to achieve EMI cancellation and interleaving operation to reduce the ripple content. The Electro Magnetic Interference (EMI), which is a hidden problem in BLIL, is reduced in this converter [9, 10].

The above mentioned topologies are also analyzed from the reliability point of view as reliability plays an important role in estimating the rate of system failures, warranty and the probability of functionality of a product for a defined period of time under specific conditions without any failure.

II. Phase Shifted Semi Bridgeless IBC

A. Circuit Diagram

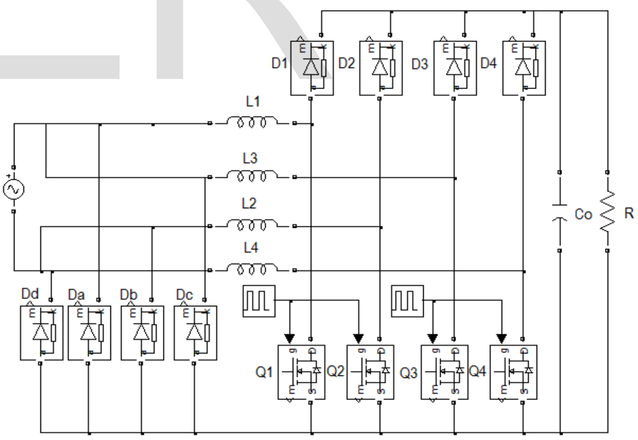

Fig. 1. Circuit diagram of PSIBC topology

B. Operation

During the positive half cycle of the supply, switches Q1 and Q2 are turned on. Thus the current flows along the path L1 - Q1 - Q2 and returns to the mains via L2. Thus the inductors L1 and L2 are charged up during this interval. When Q1 – Q2 are turned off, due to large rate of change of current flow, the voltage across the inductor reverses its polarity to oppose the large change in di/dt and tries to maintain current in the same direction. Thus inductors L1 and L2 starts discharging through D1 - load and returns to the mains through the body diode of Q2 and partially through Db.

In the interleaved converter, switches Q3 and Q4 are turned on after a phase delay of 180 degrees. The current flows along the path L3 - Q3 - Q4 returns to the mains via L4. Thus the inductors L3 and L4 are charged up during this interval. When Q3-Q4 are turned off , the inductors L3 and L4 starts discharging through D3 , load and returns to the mains through the body diode of Q4 and partially through Dd. The same can also be explained for the negative half cycle of the supply.

III. Performance Parameters

A. Total Harmonic Distortion

Total Harmonic Distortion of input current is defined as the measure of harmonic content present in the input current. It is the measure of distortion in the input current waveform when compared with the desired waveform. Mathematically it is defined as follows,

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I^2{}_{n,rms}}}{I_{1,rms}} \qquad (1)$$

where,
I_n rms = rms value of nth harmonic component of the input current, $2 < n < \infty$.
I_1 rms = rms value of the fundamental component of the input current.

B. Supply Power Factor

Power Factor (PF) is defined as the product of displacement factor and purity factor.

$$PF = K_d \times K_p \qquad (2)$$

$$K_d = \cos\theta \qquad (3)$$

where,
Θ = angular displacement between input voltage and current waveforms
K_d = Displacement Factor
K_p = Purity Factor

C. Efficiency

Efficiency can be defined as the ratio of the output power delivered to the input power supplied to the converter. Mathematically, it is represented as follows,

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \times 100 \qquad (4)$$

D. Component Losses

1) MOSFET (Switch)

The power loss of a MOSFET comprises of the loss due to frequent switching of the device ($P_{SW(MOSFET)}$) and the losses due to conduction ($P_{COND\ (MOSFET)}$) [11].

$$P_{COND\ (MOSFET)} = I^2{}_{drain\ (rms)} \times R_{DS\ (on)} \qquad (5)$$

$$P_{SW\ (MOSFET)} = 0.5 \times V_{DS} \times I_{drain\ (rms)} \times f_{sw} \times (t_{on}+t_{off}) \qquad (6)$$

Where,
$I_{drain\ (rms)}$ - RMS current through the MOSFET
$R_{DS\ (on)}$ - On state Drain – Source resistance
V_{DS} - Drain – Source forward voltage
f_{sw} - Switching frequency
t_{on} - Turn on time of MOSFET
t_{off} - Turn off time of MOSFET

2) Fast Diode

The power loss of a diode (P_{DIODE}) is due to the reverse recovery loss ($P_{rr(DIODE)}$), diode conduction loss ($P_{COND\ (DIODE)}$) and diode switching loss($P_{SW\ (DIODE)}$).

$$P_{DIODE} = P_{rr\ (DIODE)} + P_{COND\ (DIODE)} + P_{SW\ (DIODE)} \qquad (7)$$

E. Reliability Aspects

1) Reliability Function

The probability of a component operating under specified conditions for a defined period of time can be estimated mathematically as

$$R\ (t) = e^{-\lambda t} \qquad (8)$$

where,
λ is the failure rate constant during the useful life period of the device.

2) Failure Rates

Table 1: Mathematical equations for calculation of Failure rate

Device	**Mathematical Equation for Failure rate λ_p (Failures/10^6Hours)** [12]
MOSFET	$\lambda_b \times \pi_A \times \pi_T \times \pi_Q \times \pi_E$
Fast Diode	$\lambda_b \times \pi_S \times \pi_C \times \pi_T \times \pi_Q \times \pi_E$
Inductor	$\lambda_b \times \pi_Q \times \pi_E$
Capacitor	$\lambda_b \times \pi_Q \times \pi_E \times \pi_{CV}$
Resistor	$\lambda_b \times \pi_Q \times \pi_E \times \pi_T \times \pi_P \times \pi_S$

where,
λ_b - Base failure rate of the device
π_A – Application factor
π_T – Temperature factor
π_Q – Quality factor
π_E – Environment factor
π_S – Voltage stress factor
π_C – Contact construction factor

IV. Results

The following are the results obtained on simulation of BLIL and PSIBC topologies [13, 14]:

Table 2: Design parameters for PSIBC and BLIL topologies

Design Parameters for PSIBC and BLIL	
Input supply	230 V
Supply frequency	50 Hz
L1,L2,L3,L4	667 µH
R (load)	50 Ω
C	150 µF
Switching frequency	25 kHz
Duty Ratio	0.5

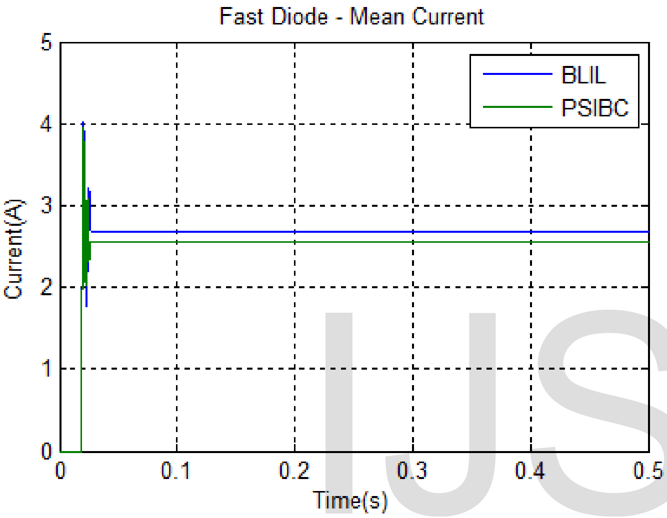

Fig. 2. Fast Diode Mean Currents for BLIL and PSIBC

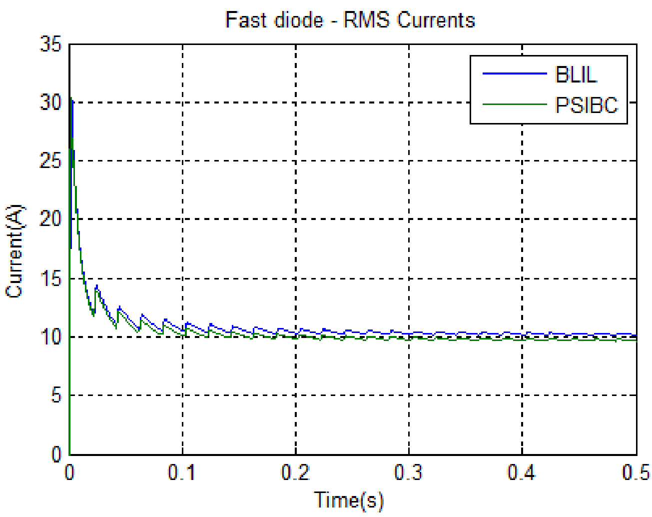

Fig. 3. Fast Diode RMS Currents for BLIL and PSIBC

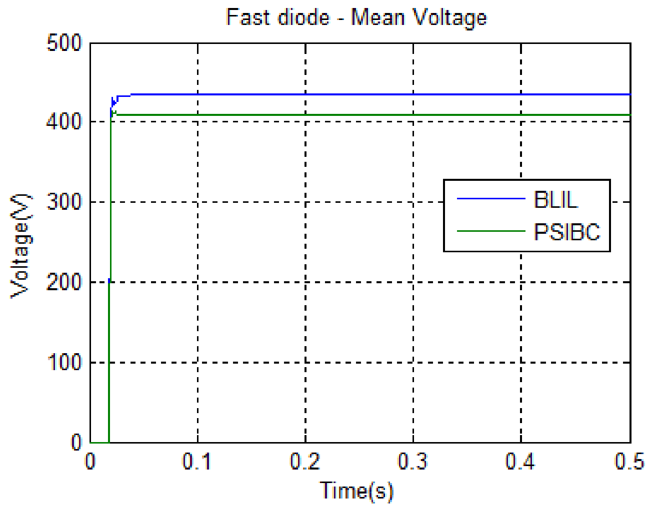

Fig.4. Fast Diode Mean Voltage for BLIL and PSIBC

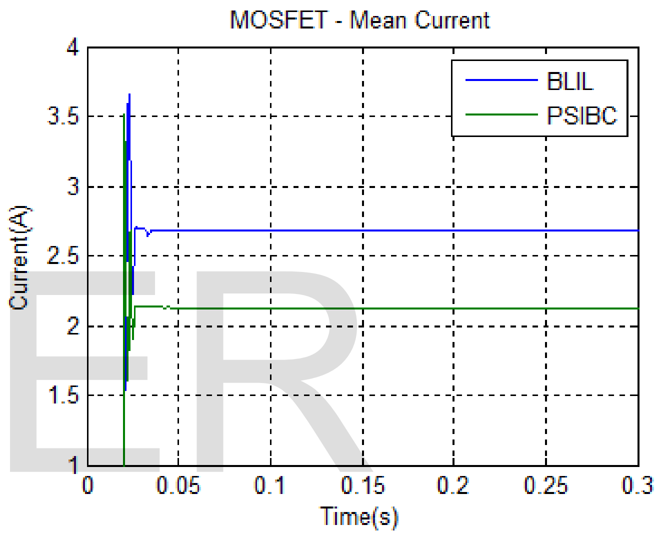

Fig.5. MOSFET Mean Current for BLIL and PSIBC

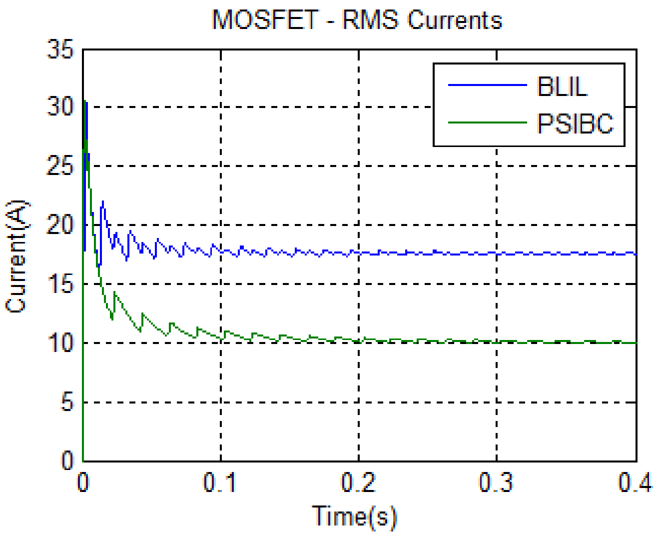

Fig.6. MOSFET RMS Currents for BLIL and PSIBC

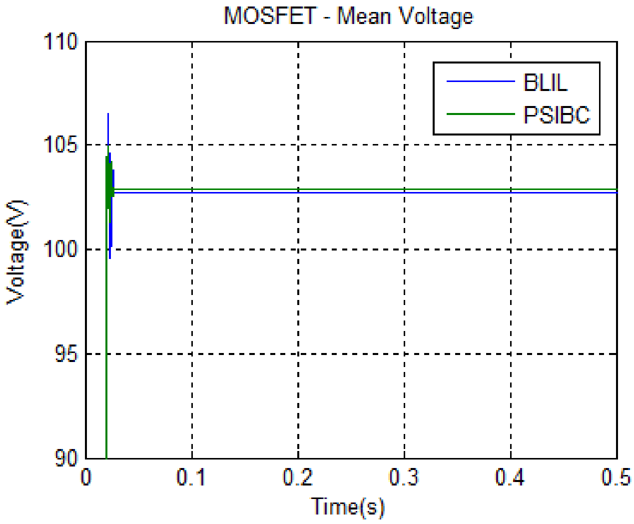

Fig.7. MOSFET Mean Voltages for BLIL and PSIBC

On examining the graphical results, it can be inferred that the current and voltage levels in the components are higher in the case of BLIL topology than PSIBC. This is the foremost cause of high power loss in BLIL topology.

Table 3: Performance Parameters of PSIBC

Performance Parameters - PSIBC	
Supply power factor	0.86432734
Total Harmonic Distortion (%)	58.18
Supply voltage peak (V)	325
Supply power (W)	7140.7267
Mean output voltage (V)	570.4076
Mean load current (A)	11.592
Output power (W)	6612.1648
Efficiency (%)	92.5979

Hence, the performance parameters of a 6.6kW Charger for HEVs with Phase Shifted Semi Bridgeless Interleaved Boost AC – DC Converter are tabulated in table 3.

V. Analysis and Comparison of Power Loss and Reliability Aspects of PSIBC and BLIL Topologies

The following devices manufactured by the leading manufacturers are selected to estimate the reliability and power loss of BLIL and PSIBC topologies. All the selected devices are RoHS (Restriction of Hazardous Substances Directive) compliant and qualified by AEC (Automotive Electronics Council) and JEDEC (Joint Electron Device Engineering Council) .

Table 4: Components for estimating the Reliability and Power loss of BLIL and PSIBC

Component	**Specification**
Switch (MOSFET)	IPB60R099CP
Fast Diode	IDB06S60C
Inductor	Kool mu 77071 core type
Capacitor	EKXJ451ELL820

Table 5: MOSFET Specifications

IPB60R099CP – Infineon MOSFET – Low Frequency (Less than 400MHz) – Specifications		
Parameter	**Value**	**Remark**
R_{DS} ON	0.09 Ω	
$T_{ON} + T_{OFF}$	80 ns	
λ_b (Base Failure Rate)	0.012	MOSFET
Π_A (Application Factor)	10	Rated Power ≥ 250W
Π_Q (Quality Factor)	5.5	Assuming the worst case – Lower Quality
Π_E (Environment Factor)	6	G_F
Π_T(Temperature Factor)	BLIL – 245.9066 PSIBC – 68.01547	
T_a (Ambient Temperature)	27˚C	

Table 6: Specifications of Fast Diode

IDB06S60C – Infineon Diode – Low Frequency (Less than 400MHz) – Specifications [15]		
Parameter	**Value**	**Remark**
$T_{ON} + T_{OFF}$	10 ns	
Forward Voltage drop	1.5 V	
λ_b (Base Failure Rate)	0.025	Fast Recovery type
Π_S (Electrical Stress Factor)	0.09729	
Π_Q (Quality Factor)	5.5	Assuming the worst case – Lower Quality
Π_E (Environment Factor)	6	G_F
Π_T(Temperature Factor)	BLIL – 163.52246 PSIBC – 143.0755	Fast Recovery type
T_a (Ambient Temperature)	27˚C	

Table 7: Specifications of Capacitor

EKXJ451ELL820 – Capacitor – Specifications		
Parameter	**Value**	**Remark**
Type	CQ,CQR	Capacitor, Fixed Plastic Dielectric (Hermetically sealed in metal, ceramic or glass cases)
λ_b (Base Failure Rate)	0.00051	CQ,CQR
Π_Q (Quality Factor)	10	Unknown/Commercial Purposes
Π_E (Environment Factor)	6	G_F
Π_{CV}	0.06969	$(0.34*C^{0.18})$
T_a (Ambient Temperature)	27˚C	

Table 8: Specifications of Inductor

Kool mu 77071 – Inductor – Specifications		
Parameter	**Value**	**Remark**
λ_b (Base Failure Rate)	0.049	High Power, High Pulse
Π_Q (Quality Factor)	3.0	Lower Quality
Π_E (Environment Factor)	6	G_F
T_a (Ambient Temperature)	27˚C	

The power loss calculations, power factor and efficiency of BLIL and PSIBC are recorded as follows:

Table 9: Comparison of Power loss, Power factor, Efficiency of BLIL and PSIBC

Feature	BLIL	PS IBC
Switch Losses (MOSFET * 4)	110.7208 W	36.089 W
Fast Diode Losses (Diode * 4)	18.44596 W	17.512 W
Power Factor	0.90200	0.86432734
Efficiency	91.752%	92.5979%

Hence, it is mathematically justified that BLIL topology suffers due to high power loss and reduced efficiency when compared with PSIBC.

Table 10: Comparison of Reliability and Failure rates of BLIL and PSIBC

Feature	PSIBC	BLIL
λ_p MOSFET	269.3412648	973.7904207
λ_p Diode	11.483864	13.12500806
λ_p Inductor	1.00128	1.00128
λ_p Capacitor	3.55E-3	3.55E-3
λ_p Resistor	0.0297	0.0297
λ_p System	1127.338885	3951.700085
MTBF (Hours)	887.0447	253.0556415

The base failure rates of individual components and of the whole system are calculated and tabulated in table 10 along with the Mean Time between Failures (MTBF). From the table it is mathematically justified that the overall failure rate of the system is less in the case of PSIBC. Hence, It is highly reliable for the specified applications.

VI. Conclusion

On comparison of both the topologies, it is inferred that though there is a marginal decrease in power factor in PSIBC due to the harmonics induced by the slow diodes, its major features such as reduced EMI noise, high reliability and improved efficiency proves it to be an optimal topology for implementation in HEV chargers than BLIL. Performance parameters and reliability aspects based on MILHDBK-217F standards are calculated and also mathematical justification for the low power loss and high reliability in the case of PSIBC topology is also provided in this paper. Hence it is mathematically proved that Phase Shifted Semi Bridgeless Interleaved Boost AC – DC converter is a highly reliable topology for use in the charging system of HEVs.

VII. References

[1] Yun-Sung Kim, Won-Yong Sung and Byoung-Kuk Lee, “Comparative Performance Analysis of High Density and Efficiency PFC Topologies”, IEEE Transactions on Power Electronics, Vol.29, No.6, June 2014

[2] Fariborz Musavi, Murray Edington, Wilson Eberle and William G. Dunford, “Energy Efficiency in Plug-in Hybrid Electric Vehicle Chargers: Evaluation and Comparison of Front End AC-DC Topologies”, supported by Delta-Q Technologies Corporation.

[3] Fariborz Musavi, Murray Edington, Wilson Eberle and William G. Dunford, "Evaluation and Efficiency Comparison of Front End AC-DC Plug-in Hybrid Charger Topologies”, IEEE Transactions on Smart Grid, Vol. 3, No. 1, March 2012

[4] Fariborz Musavi, “A High-Performance Single-Phase AC-DC Power Factor Corrected Boost Converter for plug in Hybrid Electric Vehicle Battery Chargers”, ISBN: 978-1-4244-5287-3

[5] Luciano S. C e Silva, Falcondes J.M. de Seixas, Priscila da S. Oliveira, “Experimental Evaluation of the Bridgeless Interleaved Boost PFC Converter”, Industry Applications (INDUSCON), 2012 10th IEEE/IAS International Conference

[6] Chuanyun Wang: "Investigation on Interleaved Boost Converters and Applications", Faculty of the Virginia Polytechnic Institute and State University, pp.1-128, (2012).

[7] John Karatzaferis, Nick Papanikolaou, Emmanuel Tatakis, Michael Loupis: "Comparison and Evaluation of Power Factor Correction Topologies for Industrial Applications", Laboratory of

Electromechanical Energy Conversion (LEMEC), pp.401-410, (2013).

[8] Mehdi Narimani, "A New Interleaved Three-Phase Single-Stage PFC AC–DC Converter", IEEE Transaction on Industrial Electronic, Vol. 61, No. 2, February 2014

[9] Cheng Deng, Dehong Xu, Pingping Chen, Changsheng Hu, Wenping Zhang, Zhiwei Wen and Xiaofeng Wu "Integration of Both EMI Filter and Boost Inductor for 1kW PFC Converter", DOI 10.1109/TPEL.2013.2295391, IEEE Transactions on Power Electronics

[10] Cheng Deng, Min Chen, Pingping Chen, Changsheng Hu, Wenping Zhang and Dehong Xu, "PFC Converter with Novel Integration of both EMI Filter and Boost Inductor", Energy Conversion Congress and Exposition (ECCE), 2013 IEEE

[11] Dr.R.Seyezhai, S.Mahalakshmi, M.Bhavani and R.Anitha "Analysis of Power Loss Calculation for Interleaved Converter using Switched Capacitors", International Journal of Advances in Electrical and Electronics Engineering, ISSN: 2319-1112

[12] Gulam Amer Sandepudi, Srinivasa Rao, "Estimation of Reliability of a Interleaving PFC Boost Converter", Serbian Journal of Electrical Engineering, Vol. 7, No. 2, November 2010, 205-216

[13] V.Nithin, P.Siva Priya, N.Siva Sumanth, Dr.R.Seyezhai and K.Vigneshwar, "Investigation of Two Phase Bridgeless Interleaved Boost Converter for Power Factor Correction", ISSN (online) 2347-2812 Volume-1, Issue-3, 2013

[14] Keun-Wan Koo, Dong-Hee Kim, Dong-Gyun Woo and Byoung-Kuk Lee, "Topology comparison for 6.6 kW On Board Charger: Performance, Efficiency, and Selection Guideline", 2012 IEEE Vehicle Power and Propulsion Conference, Oct. 9-12,2012, Seoul, Korea

[15] "Military Hand Book - Reliability Prediction of Electronic Equipment", MIL-HDBK-217F