ISSN 2229-5518

A Survey on FFT Processors

T.Angeline, D.Narain Ponraj

Abstract—This paper describes about the Fast Fourier Transform (FFT) processors which play a vital role in Digital Signal Processing, Wireless Communications and Medical electronics. First the evolution and various application areas of FFT are explored. Then the different processor architectures are outlined and the algorithm and technique involved in each architecture is explored.

Index Terms— Commutator, Discrete Fourier Transform (DFT),Fast Fourier Transform(FFT) ,Memory, Pipelining, Multipath, Singlepath.

1 INTRODUCTION

Fast Fourier Transform(FFT) is an efficient algorithm in calculating Discrete Fourier Transform. John Tukey a mathematician explained a fast method for computing Fourier Transform in 1963.Later Cooley joined with Tukey and presented Fast Fourier Transform.FFT is based on two concepts Divide and Conquer method and recursion method.Divide and conquer is the approach in which the larger problem is decomposed into smaller ones. A fast algorithm derived based on divide and conquer method and recursion is called Fast Fourier Transform. To reduce the computational complexity various algorithms were developed and from these algorithms Cooley-Tukey's radix-2[1] FFT algorithm is simple and widely used. Apart from this there are several FFT algorithms which include radix-4,split radix [2],radix-2^2 [3], radix-2^3 [4], radix-2^4 [5],radix-2^5 [6], radix-2^k [7], radix-r^k[8], prime factor algorithms [9], Winograd Fourier transform algorithms [10].

Discrete Fourier Transform is playing a vital role in speech, image and seismic processing.DFT helps in analysing spectrum and in correlation analysis [11].Spectral analysis is used in speech bandwidth reduction systems, in radar systems for obtaining the target velocity and for surface vessels and submarines. It also plays an important role in digital video broadcasting and in Orthogonal Frequency Division Multiplexing systems. In OFDM it plays a wide role in Ultra Wide Band,Very High Bitrate DSL and in Worldwide Interoperability for Microwave Access (WiMAX). The performance of FFT processors increase steadily with the advances in semiconductor processing technology.In ultra wideband applications FFT processor is the module with high computational complexity. As it is a key component in most of the digital systems it should be designed properly in achieving high speed, low power, low area etc.,

The paper is organized as follows. FFT algorithm is given in chapter 2.In Chapter 3 different FFT architectures are discussed. In Chapter 4 the results are discussed. Chapter 5 gives the conclusion.

- *T,Angeline, M.Tech student, Department of ECE Karunya University, Coimbatore.*
- *D.Narain Ponraj,Assistant Professor,Department of ECE Karunya University, Coimbatore.*

2 FFT ALGORITHM

The Discrete Fourier Transform (DFT) [11],[12] for an *N*-point input signal *x*(*n*) is given by

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}$$

Where k=0, 1,…..N-1 and the twiddle or rotation or phase factor is given by $W_N^{kn} = e^{-j2\pi kn/N}$

Here *X(k)* represents the frequency domain values obtained from the Fourier transform on *x(n)*.DFT computes X(K) from x(n).The direct computation of DFT is very complex and because of this FFT algorithm is used. To reduce the number of computations FFT algorithm uses a divide-and-conquer approach[12] recursively.Radix-2 is an FFT algorithm in which divide by 2 approach is recursively used. Apart from radix-2 algorithm there are other algorithms like radix-4[12], radix-8 and other higher radix algorithms where there are only less intermediate stages when compared to radix-2 algorithm. Radix-4[12] is an FFT algorithm which is used when N in DFT is a power of 4.This algorithm helps in reducing the number of multiplications but increases the number of additions. Lesser number of intermediate stages does not always lead to the design of faster processor. But when the techniques involved and the hardware used for the design of substructures in processor are accurate and simple then it will lead to the design of a better processor.

3 FFT ARCHITECTURES

3.1 Single Memory

Bevan M. Baas described about single, dual, array and cached memory architectures in his paper [13]. Single-memory architecture consists of a memory and a processor. A bidirectional data bus runs between the memory and the processor through which data exchange takes place between them. Data are read from memory and written back to the memory using bidirectional bus.

3.2 Dual Memory

In dual-memory architecture [13] two memories are used. A processor is present in between the two memories. Bus connects the memory 1 and memory 2 to the processor. Data input from one memory will pass through the processor to the second memory during processing of data. This process is done until the transform has been calculated..

3.3 Array Memory

Array architecture [13] consists of a number of independent processing elements with local buffers and they are connected through a network.

3.4 Cached Memory

The cached-memory [13] architecture consists of a cache memory inaddition to the single memory architecture. Cache memory is present in between the processor and main memory and it makes the process faster.

3.5 Pipelined Architectures

In pipelined architectures continuous processing of data is done through a series of processing elements. Pipelined architectures have high throughput rate when compared to the other architectures. For real-time applications pipelined architectures are more suitable.

3.5.1 Single path Architectures

3.5.1.1 R2SDF

S.He and M.Torkelson [3] described that in Radix-2 single-path delay feedback (R2SDF) [14] architecture data is processed in a feedback manner. Every stage of this architecture has a data path that goes through the multiplier. The number of processing elements (PEs) and multipliers used for radix-2 multi-path delay commutator architecture and this architecture are same, but the delay elements required for this architecture is only N-1[3].

In a single-path delay feedback FFT processor several long and wide delay lines are used. Delay lines are designed using shift registers which is nothing but the cascading of D flipflops. For each clock edge, data movement is in a forward direction in a lock-step fashion. Due to this half of the registers change states resulting in the wastage of power. For achieving low power and low area a R2SDF architecture [16] has been proposed with SRAM replacing the shift registers. To perform read and write operations in one clock cycle a dual port memory is required. But it can be replaced by two single port SRAMs[17] which can save area upto 33%.The read operation is performed during the first half cycle and the write operation in the next half cycle. Current mode SRAMs [18] are used which helps in power reduction. Two registers, one before the PE and the other after, are inserted to prevent the data access of the SRAM becoming critical paths. To access data from SRAM a ring counter is used instead of address decoder and true-single-phase-clock flipflops are used in the ring counters to reduce power consumption.

3.5.1.2 R4SDC

S.He and M.Torkelson [3] described that in Radix-4 Single-path Delay Commutator [19] a modified radix-4 algorithm is used.In this architecture the multipliers are utilized upto 75% using the programmable butterflies. The memory requirement can be reduced to 2N-2 using combined delay-commutator[3]. The most complicated parts in this architecture are butterfly and delay-commutator. For low power applications a new commutator is introduced [20].This commutator is termed as IDR architecture which is far superior than single port, Dual port and Triple port RAM architectures interms of power and area for two stages. For the third stage single port RAM is the good choice. The RAM blocks in this IDR architecture are enabled only if the outputs are needed which helps in reducing switching activity which inturn reduces the power consumption.

3.5.2 Multi path Architectures

3.5.2.1 R4MDC

Multipath Delay Commutator processes data in parallel. In R2MDC [11] two parallel data paths are present and two data are processed parallel in butterfly units i.e., in this architecture both pipelining and parallel processing are used. The two data which are to be processed are fed correctly to the butterfly units with the help of delay elements and multiplexer. This architecture requires ($\log_2 N$-2) multipliers, and 3N/2-2 delay elements[3].Radix-4 Multipath Delay Commutator [11] is same as R2MDC but here radix-4 algorithm is used and so four parallel data paths are present.In this architecture the components are utilized only upto 25% and this is because they are active once during the four cycle. This architecture requires $3\log_4 N$ complex multipliers and 5N/2-4 registers [3].The main drawbacks are high hardware cost and low utilization. However, if the four inputs are fed at the same time, computational elements are utilized perfectly which inturn reduce memory requirements.

Energy optimised high performance FFT processor [23] is designed to overcome the difficulties in conventional R4MDC architecture. In this architecture the input reordering requires only less hardware.ROM is used for storing the twiddlefactors. Thus this modified architecture requires only 7N/4-4 memory cells. As the reordering of the input data requires only small buffers for reordering this architecture helps in reducing hardware cost as well as energy

consumption to some extent. This modified architecture achieves improvement in memory utilization and reduction in memory leakage energy.

The two pipeline architectures i.e., single path delay feedback [24] and multi-path delay commutator have both advantages and disadvantages. The advantage of multipath delay commutator is that the throughput rate is much higher when compared to the single path feedback scheme. But, the disadvantages of this architecture are the number of data path required is large, the size of the FFT is large. The requirement of the memory cells and complex multiplier in the Multipath Delay Commutator architecture is comparatively higher than that of the Singlepath Delay Feedback structure. The MDC scheme helps in achieving higher throughput rate,on the otherside the SDF scheme needs lesser memory and hardware cost. In UWB applications MDC architecture is preferred due to its high-throughput-rate. But in the conventional Radix-2 MDC architecture frequency has to be raised to maintain the required throughput rate [25].

The Radix-4 MDC architecture and the Split-Radix MDC architecture have their limitation on FFT size and higher hardware cost [3] respectively. In addition, the higher radix FFT algorithm is difficult to be implemented in the traditional MDC architecture. By increasing the number of data paths in the MDC architecture the higher throughput rate can be achieved. As this architecture helps multiple data to operate at the same time it requires more memory and complex multipliers which inturn increases the hardware cost. Inorder to handle the above difficulties the features of the SDF and MDC architectures are combined to produce a mixed-radix multipath delay feedback (MRMDF) architecture [26] which is a four-data-path pipelined FFT architecture. The proposed FFT / IFFT architecture is not only suitable for the proposed UWB physical layer but also provide the necessary throughput rate to meet the UWB specifications. This architecture has lower hardware cost compared with the conventional MDC architecture and also saves power dissipation by using the high-radix FFT algorithm.

3.5.2.2 MRMDF

The MRMDF architecture [26] has the following features. It uses both radix-2 and radix-8 algorithm. The four parallel data paths provide higher throughput rate. There are two places where we need to reorder the data and they are to reorder the input data and to reorder the results of each module. As single feedback design is used the memory required for the above two reordering gets reduced. In this architecture scheduling scheme and specified constant multipliers are used and this reduces the number of complex multipliers. This architecture helps in achieving throughput of 1Gsamples per second at the clock rate of only 250MHz.

Architectures R2^2MDF [27], R2^4MDF [28] are designed by combining the features of SDF and MDC architectures. In this architecture [28] canonic signed division multiplication is used which helps in achieving low area and less power consumption. This architecture is also a four parallel architecture with which the throughput rate can be increased. Further as this architecture uses radix-2^4 algorithm and the power dissipation is also reduced here.

3.5.2.3 SRMDC

Apart from these architectures there are also architectures based on split-radix FFT algorithm. They are Split radix Multi-path Delay Commutator and Split radix single path Delay Feedback structures. But due to the disadvantages in the single path structures,multipath split-radix commutator [29] is designed. This architecture is a four parallel path architecture in which the data arrive at the computing elements perfectly with the help of delay commutator. In this architecture a dual port memory is used. This processor will operate at a frequency of 350MHz.

The main area to be concentrated in a FFT processor is twiddle factor generation and multiplication. There are different multipliers including complex multipliers and COordinate Rotation DIgital Computer (CORDIC) [21],[22] based multipliers. The area required for storing the twiddle factors is large as it is stored in a ROM memory and used for further multiplications. Inorder to overcome this disadvantage a ROM-free twiddle factor generator is used in [30] in which simple accumulators, shifters, registers and adders are used and this architecture is also a reconfigurable architecture .Multiplication is another important area to be considered. A CORDIC based multiplier [31] is used to achieve hardware simplicity when compared to booth multipliers.

Apart from these architectures the architectures are now derived for simplifying the architecture. These architectures are derived using decomposition of algorithm. There are also FFT architectures when the inputs are only real. For real valued FFT architectures some of the outputs are repetitive in nature. Using this concept real valued FFT architectures are designed with hardware simplicity by removing the redundant outputs.

4 RESULTS AND DISCUSSION

We have discussed different architectures based on single path realization and multipath realization. These architectures can again be under the categories of feedforward and feedback architectures. The main advantages of single path architectures are they require less memory, simple to design, hardware simplicity and less cost. Their disadvantages include less throughput and high latency. When we analyze multipath architectures they have high throughput but they require more memory, structures are too complicated etc.,

TABLE 1
PERFORMANCE MEASURES OF VARIOUS ARCHITECTURES

	R4MDC [23]	MRMDF [26]	R2^{4}MDF [28]	SPLIT RADIX [30]
Technology	65nm	180nm	180nm	180nm
Point	1024	128	128	8192
Clock Rate (MHz)	19	110	450	200
Area(mm^2)	2.71×3.15	1.76×1.76	---	3.6

5 CONCLUSION

In this paper a survey on FFT processors is presented. As FFT plays an important role in many of the digital systems, design of such a processor also plays an important role. Many applications like UWB requires high throughput rate where we can go for Multipath structures as it processes data in parallel with a little penalty in area and memory when compared to the single path structures. The designs of such architectures are also slightly complicated in nature. The main area to be concentrated in FFT architectures is twiddle factor multiplication and when the multiplication is done with less memory requirement, less power consumption and with high accuracy then it will be the better suitable for today's applications.

REFERENCES

[1] J. W. Cooley and J. Tukey, "An algorithm for machine calculation of complex fourier series," *Math. Comput.*, vol. 19, pp. 297–301, Apr. 1965.

[2] P. Duhamel and H. Hollmann, "'Split radix' FFT algorithm," *Electron. Lett.*, vol. 20, no. 1, pp. 14–16, Jan. 1984.

[3] S.He and M.Torkelson,"A New approach to Pipeline FFT processor," In *Proc. Int.Parallel Processing Symp.,*1996,pp.766-770.

[4] S.He and M.Torkelson, "Designing pipeline FFT processor for OFDM (de)modulation," in *Proc. URSI Int. Symp. Signals Syst. Elect.*, 1998, pp. 257–262.

[5] Chih-Peng Fan1, Mau-Shih Lee, and Guo-An Su "A low multiplier and multiplication costs 256-point FFT implementation with simplified radix-2^4 SDF architecture" in IEEE Asia Pacific Conference on Circuits and Systems,Dec 2006.

[6] Taesang Cho,Hanho Lee, Jounsup Park, Chulgyun Park " A high speedlow-complexity modified radix-2^5 FFT processor for gigabit WPAN applications Circuits and Systems,2011 IEEE International Symposium.

[7] M. Garrido, J. Grajal, M. A. Sanchez, and O. Gustafsson, "Pipelined radix-2^k feedforward FFT architectures," *IEEE Trans. VLSI Syst.*, 2012.

[8] A. Cortes, I. Velez, and J. F. Sevillano, "Radix r^k FFTs: Matricial representation. and SDC/SDF pipeline implementation," *IEEE Trans. Signal Process,*vol. 57, no. 7, pp. 2824–2839, Jul. 2009.

[9] C. S. Burrus and P. Eschenbacher, "An in-place, in-order prime factor FFT algorithm," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 29, no. 4, pp, 806–817, Apr. 1981.

[10] A. V. Oppenheim and R. W. Schafer, *Dicrete-Time Signal Processing* Prentice Hall, 1989.

[11] L.R. Rabiner and B. Gold. *Theory and Application of Digital Signal Proc* essing Prentice-Hall, Inc., 1975.

[12] John G.Proakis,Dimitris G.Manolakis,*Digital Signal Processing* Prentice-Hall, Inc., 2007.

[13] Bevan M. Baas, "A low power,high performance 1024-point FFT Processor," in IEEE J. Solid-State Circuits, vol. 34, no. 3, pp. 380–387, Mar 1999.

[14] E.H. Wold and A.M. Despain, "Pipeline and parallel-pipeline FFT processors for VLSI implementation". *IEEE Trans. Comput.*, C33(5) :414–426,May1984.

[15] Groginsky, H.L., and Works, G.A "A pipeline fast Fourier trans form",IEEE Trans. Comput., 1970, 19, (11), pp. 1015–1019.

[16] Y.-T. Lin, P.-Y. Tsai and T.-D. Chiueh "Low-power variable-length fast Fourier transform processor" IEE Proc.-Comput. Digit. Tech., Vol. 152, No 4, July 2005.

[17] Li, W., and Wanhammer, L.: "A pipeline FFT processor" Proc. Work shop Signal Processing Systems Design and Implementatio 1999.

[18] Wang, J.-S., Tseng, W., and Li, H.-Y.: 'Low-power embedded SRAM With the current-mode write technique', IEEE J. Solid-State Circuits, 2000, pp. 119–124.

[19] G. Bi and E. V. Jones., "A pipelined FFT processor for word sequential data" *IEEE Trans. Acoust., Speech, Signal Processing*, 37(12):1982–1985, Dec. 1989.

[20] Wei Han, T. Arslan, A.T. Erdogan and M. Hasan, "Low-power Commutator for Pipelined FFT Processors," *IEEE International symposium on Circuits and Systems(ISCAS),*Vol.5,Kobe,Japan May 2005,PP. 5274-5277.

[21] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Transactions on Electronic Computers*, vol. EC-8, no. 3, pp. 330–334, Sep. 1959.

[22] M. Garrido and J. Grajal, "Efficient memoryless CORDIC for FFT computation," in *Proc. IEEE Int. Conf. Acoust. Speech Signal Process.*, vol. 2, 2007, pp. 113–116.

[23] Dongsuk Jeon1, Mingoo Seok, Chaitali Chakrabarti, David Blaauw, Dennis Sylvester "Energy-Optimized High Performance FFT processor" ICASSP 2011.

[24] A.M. Despain. "Fourier transform computer using CORDIC iterations" *IEEE Trans. Comput.*, C-23(10):993–1001, Oct. 1974.

[25] B. Zhai, et al., "Energy-Efficient Subthreshold Processor Design,"*IEEE Transactions on VLSI Systems* pp. 1127-1137, 2009.

[26] Y. W. Lin, H. Y. Liu, and C. Y. Lee, "A 1-GS/s FFT/IFFT processor for UWB applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1726–1735, Aug. 2005.

[27] J. Lee, H. Lee, S. I. Cho, and S. S. Choi, "A High-Speed two parallel radix- FFT/IFFT processor for MB-OFDM UWB systems," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 4719–4722.

[28] M. Shin and H. Lee, "A high-speed four parallel radix- FFT/IFFT

processor for UWB applications," in *Proc. IEEE ISCAS*, 2008, pp.960-963.

[29] Jesús García1, Juan A. Michell, Gustavo Ruiz, Angel M. Burón FPGA realization of a Split Radix FFT processor VLSI Circuits and Systems III, edited by Valentín de Armas Sosa, Kamran Eshraghian, Felix B. Tobajas, Proc. of SPIE Vol. 6590, 65900P, 2007.

[30] Tze-Yun Sung, Hsi-Chin Hsin, Lu-Ting Ko Reconfigurable VLSI Architecture for FFT Processor WSEAS Transactions on Circuits and Systems Issue 6, Volume 8, June 2009.

[31] M. D. Ercegovac, T. Lang, "CORDIC algorithm and implementtions." *DigitalArithmetic, Morgan Kaufmann Publishers*,2004.