A NOVEL DESIGN OF 9-BIT PIPELINE ADC

Manju Devi, Arunkumar P Chavan, Dr K.N. Muralidhara

Abstract— In this paper, design of low power, 9-bit pipeline ADC architecture is introduced .A pipeline ADC architecture has a 3-stage pipeline ADC with 3-bit flash ADC followed by a 3-bit DAC at each stage. A novel approach to design a 3-bit ADC is implemented; this design offers less number of comparator and low power consumption with less circuit complexity based on this idea a 9-bit ADC is simulated in cadence virtuoso in 90 nm technology the maximum sampling speed is achieved by 670 MS/s. The power consumption of pipeline ADC is 39mW.

Index Terms— Analog to digital converter, Digital to analog converter, Sample and Hold, Comparator,

1 INTRODUCTION

Over the past years, flash ADC architecture is used for all low resolution and high speed application. Low power and high performance analog to digital converter (ADC) are the key component in mixed signal CMOS design [1,2]. Amongst various architecture, the pipeline analog to digital converter are used for applications which require high resolution and high throughput requirement of low power is increasing day-by-day so that life span of battery can be prolonged in a portable device.

As pipeline analog to digital converter (ADC) is a promising topology for high speed data conversion with compact area and efficient power dissipation. Pipeline ADC's are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers; studio came as, ultrasound monitors and many other high speed applications.

In this paper section II defines proposed pipeline ADC architecture. Simulation results are shown in section III and the conclusion with section IV.

2 Proposed Pipeline ADC Architecture

A novel design of 9 bit pipeline architecture is shown in Fig.1. 9-bit pipeline ADC architecture is built using 3 stages. Each stage of the pipeline ADC Architecture Consists of Sample and hold block, Flash ADC, DAC and summer, which gives 3 bit output.

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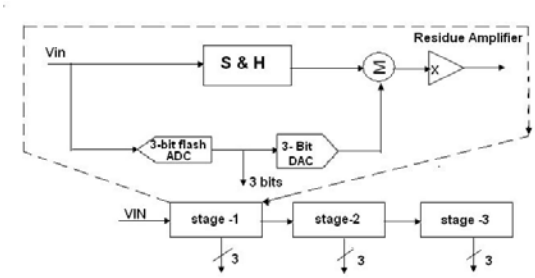

Fig.1 9 bit pipeline architecture

2.1 Sample and Hold circuit

The sample and hold circuit is a key aspect of the ADC [4], the circuit design of sample and hold is shown in Fig.2. Design of sample and hold circuit is done using a two stage op-amp.

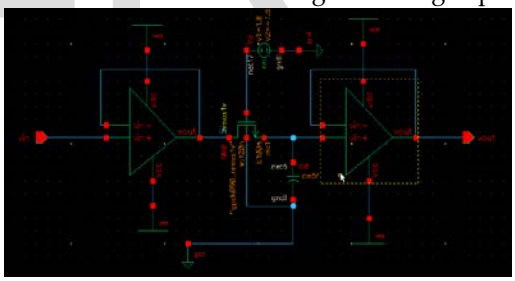

Fig. 2 Sample and Hold circuit

2.2 3-bit ADC

The basic blocks used to design a 3bit ADC are Comparator, Multiplexer, OR gate and inverter.

2.2.1 Comparator

The schematic view of pre-amplifier latch comparator is shown in Fig.3. The pre-amplifier stage consists of transistor from T0 to T4. The input differential pair NMOS transistor T0 and T1, where as the load resistor uses PMOS transistor T2 and T3. The latch is considered to be a sensitive part in the design of comparator. The schematic of latch has transistors from T5 to T13 which includes cross-coupled inverter pair T5-T6 and T7-T8 and charge imbalance circuitry T9-T11. Latch mainly consists of two inverters connected back to back with each other forming a differential comparator and NMOS transistor is connected between the differential modes of the latch. Transistor T5-T8 forms the main regenerative loop for the

latch. For minimum capacitance, width (W) and length (L) of transistor T5-T8 are kept minimum. Transistor T9-T10 is used to avoid the kick back effects from the latch to the input. When clock goes high, the amplifier is turned off and latch is used to amplify the difference obtained at input transistors T12-T13 to generate output logic levels. In this designed 4 transistors are present in the inverters combination, which reduces the parasitic capacitance and high speed can be achieved.

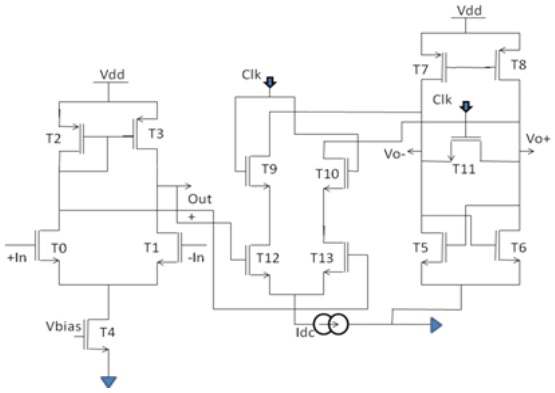

Fig.3 Pre-Amplifier Latch Comparator.

The individual blocks are designed and then integrated to build a 3-bit ADC. The proposed 3-bit ADC is a novel design which is a mixed approach of Flash and SAR type.

It mainly consist of 5 comparators, 2 OR gates, 2 MUX and an inverter. The comparator is a bottle neck of ADC which consumes maximum power dissipation among the entire block. Among the 5 comparators, the 3 comparators are effectively 'on' at a time and rest 2 will be in 'standby' mode which reduces power. This algorithm is derived from binary search algorithm [2] and it is used to calculate the digital code for the given analog voltage.

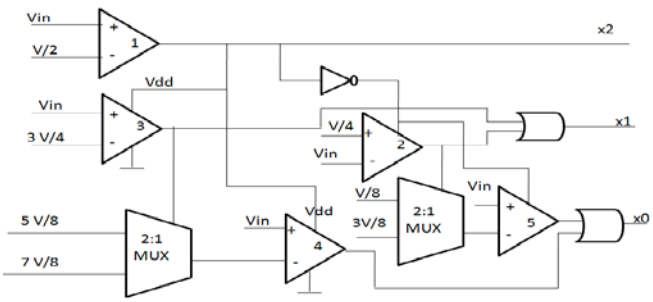

Fig.4 Proposed Model of 3 Bit Flash ADC

The algorithm steps are defined in the following ways.

1. Comparator 1, compares the Input with half of the given reference ($V_{ref}/2$), this produces the most significant bit if the digital code.
   If $V_{in} > V_{ref}/2$ Output => MSB =1, Else
   Output =>MSB=0
2. To calculate LSB bit -1:
   (i) If MSB=1 then comparator 3 compare input voltage with (3/4) of reference.
   (ii) If MSB =0 then comparator 2 compares input voltage with 1/4 of V_{ref}.

To get this, connect MSB bit to NOT gate, and connect VDD to comparator of 3/4 V_{ref} and 1/4 V_{ref} input to the inverter output.

3. Repeat the step for LSB.
4. Multiplexer is used to select comparing voltage for comparator based on previous MSB.

Algorithm

Step1: Begin

Initialize all the parameter, set value for analog input (V_{in})

If V_{in} >=V/2, set **X2=1**, else
Set **X2=0**

Step2: Set inverter input=X2 then
if X2=1, then comparator (4), comparator (2), comparator (5) = " stand by" mode and
Comparator (2), comparator (5) ="ON "mode

Step3: if X2=1 then
if V_{in} >= 3V/4 set comparator (3) output=1 else
set comparator (3) = 0
Set X1= output of comparator (3) "OR1" output of comparator (2)
Else
If B2=0, Then
If V_{in} >=V/4 set comparator output =1 else
set comparator (2) output =0.
Set X1 = output of comparator (3) OR1 output of comparator (2).

Setp4: if X2=1 then
If comparator (3) output is low and V_{in} >= 5V/8,
Set comparator (4) output=1 and
If comparator (3) output is high and V_{in} >= 7V/8,
Set comparator (4) output =1 else
Set comparator (4) output = 0.
Set X1= output of comparator (4) "OR2" output of comparator (5)
Else
If X2 =0 then
If comparator (2) output =0 and V_{in} >= V/8
Set comparator (5) output =1 and
If comparator (2) output =1 and V_{in} >=3V/8,
Set comparator (5) output =1 else
Set comparator (5) output = 0.
Set X0 = output of comparator (4) 'OR2' output of comparator (5).
end

The multiplexer is realizes using transmission gates the OR gate and inverter are realize using CMOS transistor.

2.2.2 Digital to Analog Converter (DAC)

DAC is used to produce analog signal for the given digital input. The block diagram of proposed 3-bit DAC is shown in Fig.5.

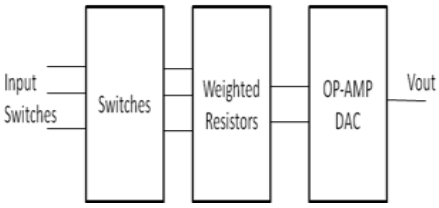

Fig.5 Block Diagram of 3-bit DAC

The weighted DAC requires switches, weighted resistors and OPAMP. The OPAMP is designed using two stages OPAMP for low power consumption [12]. The schematic representation for DAC is shown in Fig.6.

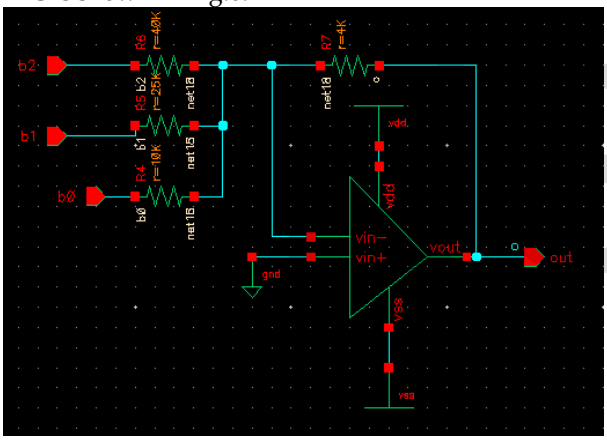

Fig.6 The schematic representation for DAC

3 Results and Discussions

Output of sample and hold circuit is shown in Fig.7

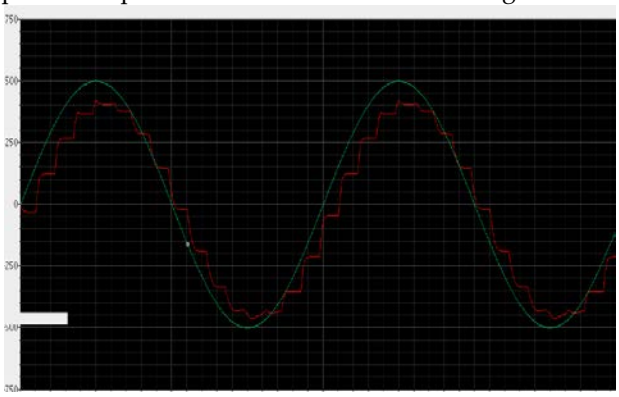

Fig.7 output waveform of sample and hold

The schematic diagram of a pre-amplifier latch comparator is shown in Fig. 8. In this design, we have used 1.8 V supply voltage for operation and clock period was 1.5ns. During the process, speed of the comparator was approximate to 670 MS/sec.

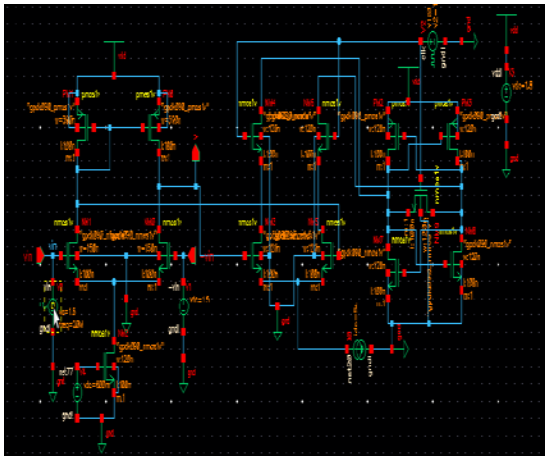

Fig.8 Schematic diagram of a comparator

The output waveforms are shown in Fig. 9 where the levels are compared.

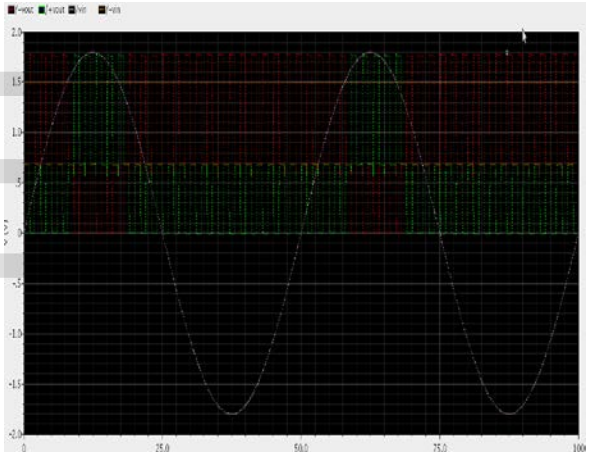

Fig. 9 Output waveform of a comparator

The Schematic view of XOR gate is shown in Fig.10. The XOR gate is designed using CMOS implementation technique.

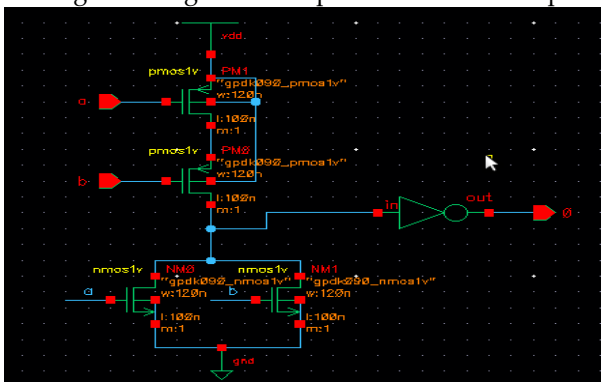

Fig.10 Schematic view of a XOR gate.

The multiplexer is design using a transmission gate technique. The Schematic diagram of 2:1 Mux design is shown in Fig.11.

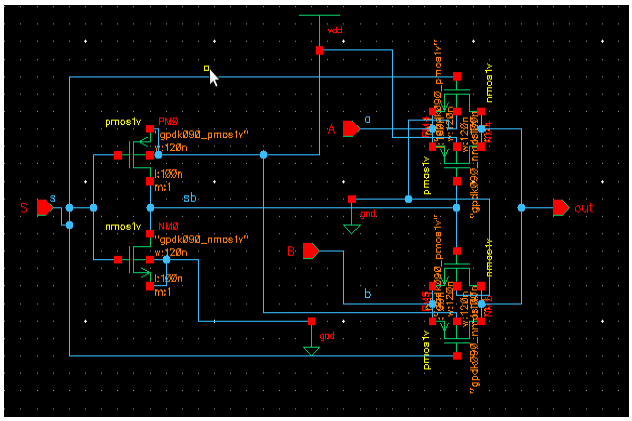

Fig.11 Schematic diagram of a 2:1 multiplexer

The schematic diagram of 3-bit flash ADC is shown in Fig.12. The reference voltages are generated using ladder circuit. The output of 3-bit ADC is given to 3-bit DAC.

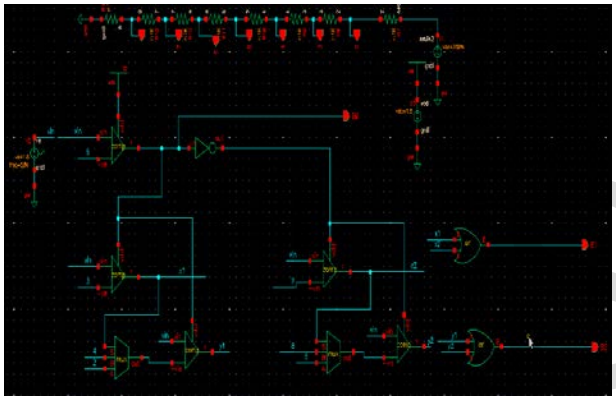

Fig.12 The schematic diagram of 3-bit flash ADC

The Output of 3 bit DAC is shown in Fig.13.

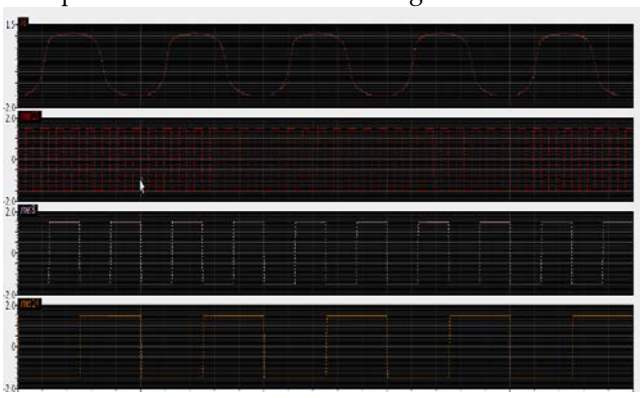

Fig.13 Output of a 3 Bit DAC

After designing all the independent blocks, these blocks are connected to form one stage ADC to give output of 3bits; this in turn is cascaded to two more stages as shown in Fig. 14 to form 9 bit pipeline ADC architecture.

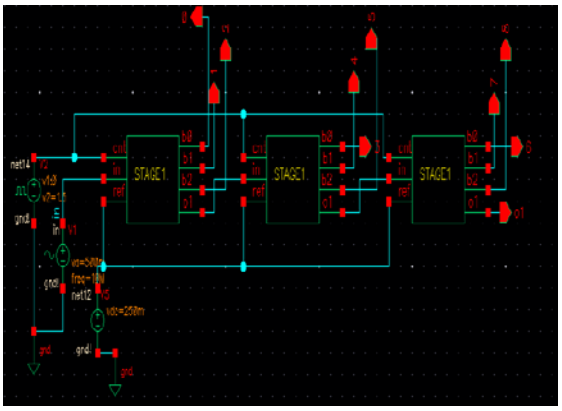

Fig. 14 schematic view of 9-bit ADC

The output Power dissipation is shown in Table.1

Table.1 power dissipation

Name	Power dissipated
Comparator	110µW
3 Bit –ADC	567µW
9 Bit pipeline ADC	39mW

4 Conclusion

In this paper a high speed and low power pipeline ADC is presented. The main bottleneck of the pipeline ADC is to design low power comparator and 3-bit ADC. The power dissipation of comparator and 3-bit ADC is 110uW and 567uW. Design and simulation is carried out using cadence 90nm technology. The maximum sampling frequency and power dissipation of 9-bit pipeline ADC is 670MS/s and 39mW.

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